EE 40 Syllabus -- Spring 2003

Date (Lecture #)	Topic	Text Covered
January 21 (1)	Introduction	
January 23 (2)	Circuit Elements and Quantities, Non-Ideal Elements	Sections 1.1, 1.2, 2.1, 2.2, 5.1
January 28 (3)	Kirchoff's Laws, RC Circuit	Sections 1.3, 8.1 (pp. 282-290)
January 30 (4)	RC Circuits, Time Constant	Section 8.1 (pp. 282-290)
February 4 (5)	Equivalent R and C, Voltage/Current Divider, Charging	Sections 2.2, 2.5, 2.6, 5.2
February 6 (6)	Nodal Analysis	Section 2.3
February 11 (7)	Dependent Sources	Section 4.1
February 13 (8)	Thevenin Equivalents	Section 3.1
February 18 (9)	Operational Amplifiers	Sections 4.2, 4.3, 4.4
February 20	**Midterm 1 (Lectures 2-8)**	
February 25 (10)	Differential Amplifiers/Comparator	Section 4.2
February 27 (11)	Digital Logic	Sections 11.1, 11.2
March 4 (12)	More Digital Logic	Sections 11.1, 11.2
March 6 (13)	Semiconductors, P/N Junction	Sections 13.1, 13.2
March 11 (14)	Load Line, Diode I-V	Sections 3.2, 13.2
March 13 (15)	Diode Circuits	Section 13.2
March 18 (16)	NMOS and PMOS Transistors, I-V	Section 13.4
March 20	**Midterm 2 (Lectures 9-15)**	
March 25 (17)	Spring Break	
March 27 (18)	Spring Break	
April 1 (19)	NMOS Circuits	
April 3 (20)	CMOS Inverter	Section 15.2
April 8 (21)	More CMOS Inverter	Section 15.2
April 10 (22)	Schmitt Trigger/Feedback	
April 15 (23)	CMOS NAND/NOR, Switch Model, Intermediate States	
April 17 (24)	Fabrication	Section 13.5
April 22 (25)	Layout	
April 24	**Midterm 3 (Lectures 16-23)**	
April 29 (26)	Computing Gate Delay	
May 1 (27)	Open Topic	
May 6 (28)	Open Topic	
May 8 (29)	Open Topic	
May 13 (30)	Open Topic	

Final Exam: Friday, May 23, 12:30-3:30 PM (Exam Group 19) Location: TBA

EE 40 Course Policies -- Spring 2003

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Course Description: This 4-unit EECS core course uses digital electronics topics to teach fundamental circuit analysis techniques. Topics include: (1) Essential quantities for circuit analysis, (2) Circuit laws and DC circuit analysis, (3) Transients and step response of RC circuits, (4) Digital logic and gates,
(5) Analog elements for digital circuits including transistors and operational amplifiers, (6) CMOS circuits and static logic gates, (7) Switch models and propagation delay for CMOS logic gates.

Textbook: *Electrical Engineering: An Introduction*, by Schwarz and Oldham, 2nd Edition, Oxford.

Class Notes: Notes will be handed out in lecture. The notes are designed to provide you with the main points and diagrams so that you can listen and think in lecture, and concentrate less on note-taking. Space will be provided for you to embellish the notes.

Class Website: http://inst.eecs.berkeley.edu/~ee40 . Class notes, homework, solutions, etc.

Class Newsgroup: ucb.class.ee40 . Check the newsgroup often for announcements.

Homework: Homework will be posted to the website when assigned, due at the beginning of class on the specified due date (at least one week later). You may discuss the homework with other students, but each student must write up the solutions independently. Turn in the homework either in class, or in the EE 40 drop box in the student lounge on the 2nd floor of Cory Hall. Late homework is not accepted, and the lowest HW score will be dropped.

Grading: There will be three midterms and one final exam. Your final score is computed as follows:

Final Score = [Midterm 1 + Midterm 2 + Midterm 3 + Homework + 2(Final Exam)] ÷ 6

The laboratory portion of the course is graded pass/fail. You must pass all the labs to pass the course.

Makeup Exams: Makeup exams will be given when there is a class conflict with the scheduled exam, a death of a close family member, or an illness with a doctor's excuse. The makeup exam may be oral or written, and might not have the same content or difficulty as the original exam.

Grading Scale: The grading scale is fixed, so your grade is determined by your performance, and is unaffected by the performance of other students. This is intended to eliminate competition.

A+ 97-100	A 89-96	A- 85-88	B+ 81-84	B 74-80	B- 70-73	C+ 66-69	C 59-65	C- 55-58	F below 55

Regrading Exams: Exams may be regraded if the grading error is pointed out when the exam is picked up. Once you take the graded exam away from the classroom/office, it cannot be regraded.

Laboratory: The lab is 3 hours per week and reinforces most of the basic concepts taught in this course. Students are responsible for downloading the lab and prelab each week, bringing the completed prelab to the laboratory, and finishing a lab report. The intent is a fun lab where students are encouraged to explore circuits and devices. It is OK to burn up transistors, though we want you to be kind to the expensive equipment. The last 5 weeks of the lab is spent on a project – a digitally controlled robot, the CalBot.

CalBot Contest: At the end of the semester, there will be a contest for you to show off your CalBot's abilities. The fastest CalBot and the CalBot with the most overall functionality will earn the winning lab team 100% on the final exam.

Felder, Richard, "Meet Your Students: 3. Michelle, Rob, and Art."
Chem. Engr. Education, 24(3), 130-131 (Summer 1990).

MEET YOUR STUDENTS

3. MICHELLE, ROB, AND ART

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The scene is the AIChE student chapter lounge at a large southeastern university. Three juniors---Michelle, Rob, and Art---are studying for the second quiz in the introductory transport course. Art got the high grade in the class on the first quiz, Michelle was close behind him, and Rob got 15 points below class average. They've been at it for over an hour.

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Michelle: "What about this stuff on non-Newtonian flow---I don't think I really get it."

Art: "I think we can forget it---I've got copies of Snavely's tests for the last five years and he's never asked about it."

M: "Maybe, but it's the real stuff...you want to analyze blood flow, for instance, Newtonian won't work."

A:"So what...the only blood flow we're going to have to worry about is ours on this test if we don't stick to the stuff Snavely *is* going to ask."

M: "Yeah, but if we don't..."

Rob: "Hey Art, is there going to be any of that Navier-Stokes trash on the quiz?"

A: "Yeah, there usually is, but no derivations---you just have to know how to simplify the equation."

R: "Rats---I hate that garbage."

M: "I've been looking through Bird, Stewart, and Lightfoot...there are all sorts of Navier-Stokes problems in there---we could try to set some of them up."

R: "Nah, too much grind---I just need to do enough to get my C, my degree, and my MG...Art my man, why don't you haul out those old tests and let's just memorize the solutions."

A: "Okay, but that may not...hey, look at this question---he's used it for three years in a row...Parts (a) and (b) are just plug-and-chug, but he throws a real curve ball here in Part (c)---I don't know how to do it."

R: "How much is Part (c) worth?"

M: "Never mind that---let me see it...okay, he's asking about velocity profile development---you just need to use the correlation for entrance length."

A: "What are you talking about---I never heard of that stuff."

M: "He never talked about it in class but it's in the reading---you need to calculate the Reynolds number and then substitute it in this dimensionless correlation, and that gives you..."

R: "I'm gonna grab a Coke from the machine, guys---when you get it all straight just tell me what formula I plug into, okay?"

A: "Yeah, sure. So it's just this correlation, huh Michelle---do I need to dig into where it comes from?"

M: "Probably not for the test, but I was trying to think why you would want to know the entrance length, and it seems to me that if you're designing a piping system that has a lot of short pipe segments it would be important to know how well your pressure drop formulas will work...blood flow again, in capillaries, or maybe lubricating oil in a car engine, or..."

A: "Forget it---that stuff's not going to be on this test...even Snavely wouldn't be that tricky...now look at this problem here..."

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These three students illustrate what Entwistle[1] calls *orientations to studying*. Michelle has a *meaning orientation*, Rob a *reproducing orientation*, and Art an *achieving orientation*. The characteristics of the orientations are as follows:

Meaning orientation. *Michelle tends to take a* deep approach *to learning, meaning that she tries not just to learn facts but to understand what they mean, how they are related, and what they have to do with her experience. Meaning-oriented learners are characterized by an* intrinsic motivation *to learn (I want to learn this material because it interests me and I find it relevant to my life) and a tendency to question conclusions offered in lectures and readings.*

Reproducing orientation. *Rob almost always takes a* surface approach *to learning---following routine solution procedures but not trying to understand where they come from, memorizing facts but not trying to fit them into a coherent body of knowledge. Reproducing learners are characterized by an* extrinsic motivation *to learn (I've got to learn this to pass the course, to graduate, to get a good job) and an unquestioning acceptance of everything in the book and in lectures. They often do poorly in school.*

Achieving orientation. *Art's primary goal is to get the highest grade in the class, whatever it takes. Achieving learners take a* strategic approach *to learning, which involves finding out what the instructor wants and delivering it---digging deep when they have to, staying superficial when they can get away with it.*

References

1. N. Entwistle, "Motivational Factors in Students' Approaches to Learning," in R.R. Schmeck, ed., *Learning Strategies and Learning Styles,* New York, Plenum Press (1988), Ch. 2.