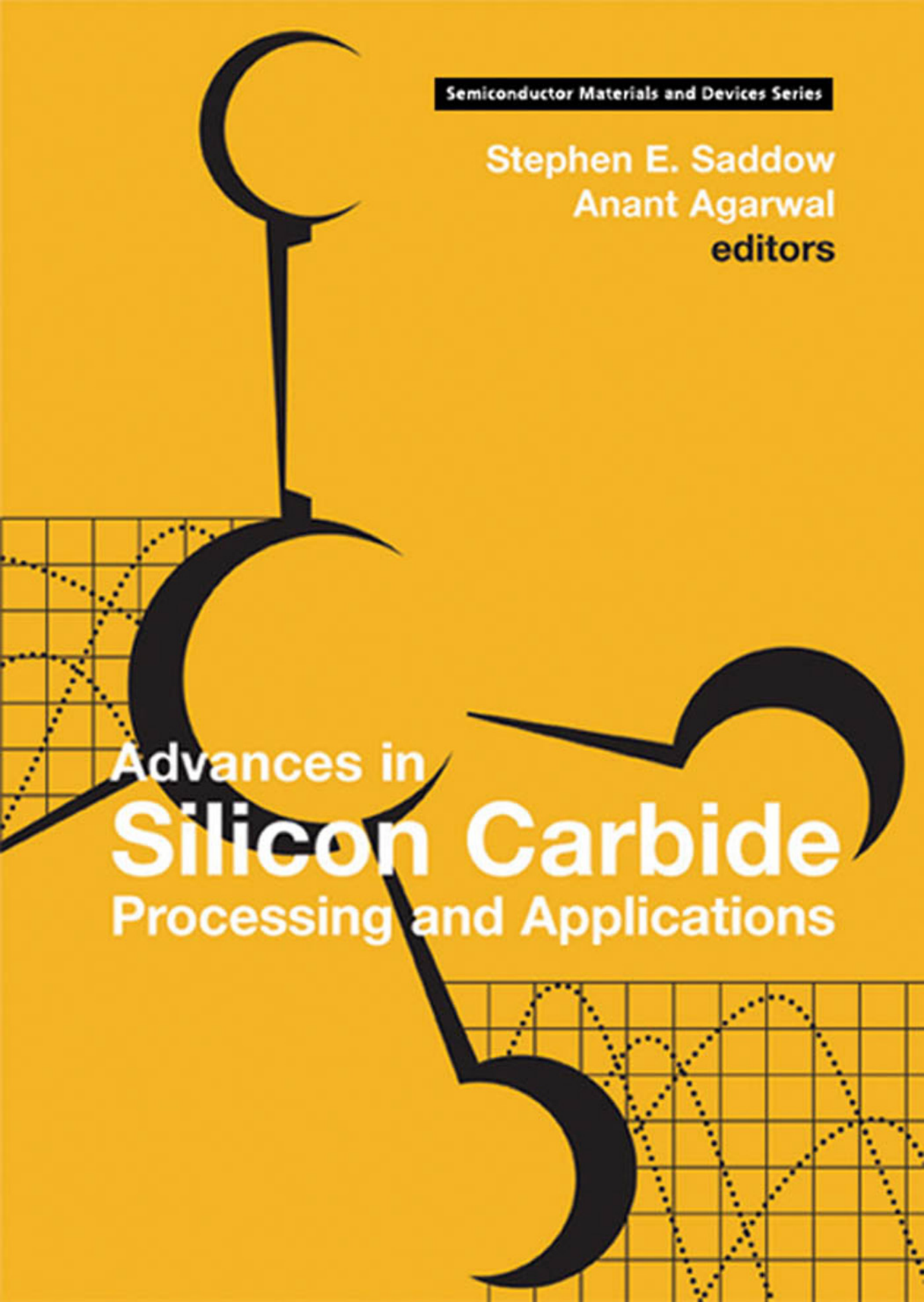

Semiconductor Materials and Devices Series
Stephen E. Saddow
Anant Agarwal
editors
Advances in
Silicon Carbide
Processing and Applications

Advances in Silicon Carbide Processing and Applications

For a listing of recent related titles, turn to the back of this book.

Advances in Silicon Carbide Processing and Applications

Stephen E. Saddow
Anant Agarwal

Editors

Artech House, Inc.
Boston • London
www.artechhouse.com

Library of Congress Cataloguing-in-Publication Data
A catalog record for this book is available from the Library of Congress.

British Library Cataloguing in Publication Data
Advances in silicon carbide processing and applications.—(Artech House semiconductor materials and devices library).
1. Silicon carbide 2. Silicon carbide—Industrial applications
I. Saddow, Stephen E. II. Agarwal, Anant
321.3'8152

ISBN 1-58053-740-5

Cover design by Igor Valdman

685 Canton Street
Norwood, MA 02062

International Standard Book Number: 1-58053-740-5

10 9 8 7 6 5 4 3 2 1

To our wives, Karen and Suman, for their love and patience

Contents

Preface

Recently there have been numerous books written on SiC, which is a testament to the importance of this technology and its potential impact on society. A majority of these books attempt to comprehensively cover a specific aspect of the technology and do this by a set of in-depth chapters on a particular research topic, concept, or result. While this is an excellent means to convey important aspects of the technology, the intent of *Advances in Silicon Carbide Processing and Applications* is to be less expansive and focus in on two of the most promising applications of SiC technology: gas and chemical sensing and electric vehicle motor drive and control. Having made this decision, we realized that the underlying device and processing issues that enable these application areas to be served by SiC technology should also be addressed. Hence a major portion of the book involves aspects of SiC technology in this key area, again with the intent (and hope) that the reader will be able to gain a broad and deep insight into the pacing issues of the technology as of this date. While there is no way to predict the wisdom of this strategy a priori, we have nonetheless tried to put ourselves into the shoes of potential readers of this book and carefully selected chapter topics that would best support this strategy.

We hope that all who read this book will benefit from the somewhat different approach we have taken. We begin with an overview of SiC as of 2003, with an attempt to provide some predictions as to the market for the technology. We then immediately jump into the application chapters, first on gas sensors, which is clearly an area where SiC can gain a significant market share compared with traditional Si technology, followed by advances in electric motor drive where, again, SiC clearly has an advantage over Si due to its robust material properties. We then step back and discuss the all-important area of SiC ion implantation technology—this is key since the properties of the SiC lattice precludes the use of thermal diffusion to achieve planar selective doping over the surface of single-crystal wafers. After discussing this topic, we then finish up with a discussion of recent advances in both SiC MOS and bipolar technology, both of which directly impact the sensor and motor drive applications. Attention was made to provide a large number references in the recognition that no single book can be fully exhaustive of such a broad subject such as SiC.

Acknowledgments

It is with the most sincere gratitude that the editors of this book thank all of the chapter authors for their dedication and hard work in bringing this idea to fruition. Just as a work of art can be immediately appreciated by the viewer, without any understanding of the efforts expended to bring it about, so too is a well-written book easy to appreciate by the reader without an appreciation of the long hours of hard work that is involved. Special thanks go to our colleagues who reviewed specific chapters of the book; their contribution has certainly improved the quality of each chapter. In particular, we thank John Wolan of the University of South Florida for his review of Chapter 2, Omar Manasreh for his review of Chapter 3, Nelson Saks of the Naval Research Laboratory for his review of Chapter 4, and Paul Chow of RPI for his review of Chapter 6. We wish to thank all of the SiC pioneers who have come before us and all of the present researchers in the field who have pushed the technology to the point where such a book project was warranted. Stephen E. Saddow would like to personally thank all of his current and former students, especially in the SiC Group at the University of South Florida, for all of their dedication and hard work that made this book possible.

Stephen E. Saddow
Tampa, Florida

Anant Agarwal
Durham, North Carolina
June 2004

CHAPTER 1

Silicon Carbide Overview

Olle Kordina and Stephen E. Saddow

1.1 General Properties

Silicon carbide (SiC) is a semiconductor material with highly suitable properties for high-power, high-frequency, and high-temperature applications. This almost worn-out opening statement may be found in many papers dealing with SiC. Yet, it cannot be left out because it really brings forward the essence of the material's potential. Silicon carbide is a wide bandgap semiconductor material with high breakdown electric field strength, high saturated drift velocity of electrons, and a high thermal conductivity. In combination with these properties, a native substrate of reasonable size exists, and one may readily grow the material and dope it both n- and p-types. In addition, SiC, like silicon (Si), has SiO_2 as its stable, native oxide. This fact is often overlooked but is key to any semiconductor technology, both from a processing perspective as well as opening up metal-oxide-semiconductor (MOS) device opportunities for SiC. Therefore, these properties make SiC ideally suited for a vast number of applications. In this chapter, we will discuss more details of these exciting properties and provide a realistic assessment of the material's challenges that are actively being studied to date. Indeed, one has to recognize that the unique properties of SiC—its robust structure, wide bandgap, high-temperature stability and so forth—also make it a challenge to manufacture and process into working devices. Although these challenges are not insurmountable, one needs to be aware of their implications before deciding to choose SiC as the technology for a particular application.

Therefore, the purpose of this book is to provide the reader with a realistic assessment of SiC as a technology one might select for a given application of interest. In this chapter, we will review material issues related to bulk and thin-film growth of SiC and then discuss some interesting applications of SiC. This will be followed by a discussion of one of the key process technologies that is absolutely essential to SiC—selective doping via ion implantation. We will then provide an update of several key device technologies ranging from power electronic switch development to MOS transistors and finally high-power radio frequency (RF) and bipolar devices.

The industrial application of SiC began with the blue light emitting diode (LED), which was very weak due to the indirect bandgap of SiC but was the only commercial blue electroluminescent light source at the time (the late 1980s). The SiC blue LED was soon surpassed in intensity by the gallium nitride (GaN)-based

LED due to the direct bandgap of the III-nitrides. However, due to the lack of a native substrate for GaN, sapphire or SiC substrates were and are still used. The biggest use of semiconductor-grade SiC is still for LEDs, but now it serves the role as the substrate for the active GaN layer rather than both the substrate and the active layer. Today there are high-frequency metal-semiconductor-field effect transistors (MESFETs) offered commercially, as well as an emerging market for Schottky diodes made from SiC. We are still at the beginning of the SiC revolution, however, and the material's full potential has yet to be realized.

1.1.1 Mechanical and Chemical Properties

Silicon carbide is a very hard substance with a Young's modulus of 424 GPa [1]. It is chemically inert and reacts poorly (if at all) with any known material at room temperature. The only known efficient etch at moderate temperatures is molten KOH at 400–600°C. It is practically impossible to diffuse anything into SiC. Dopants need to be implanted or grown into the material. Furthermore, it lacks a liquid phase and instead sublimes at temperatures above 1,800°C. The vapor constituents during sublimation are mainly Si, Si_2C, and SiC_2 in specific ratios, depending on the temperature.

1.1.2 Bandgap

The bandgap varies depending on the polytype between 2.39 eV for 3C-SiC to 3.33 eV for 2H-SiC [2]. The most commonly used polytype is 4H-SiC, which has a bandgap of 3.265 eV [2]. The wide bandgap makes it possible to use SiC for very high-temperature operation. Thermal ionization of electrons from the valence band to the conduction band, which is the primary limitation of Si-based devices during high-temperature operation, is not a problem for SiC-based devices because of this wide bandgap.

1.1.3 Critical Field

For power-device applications, perhaps the most notable and most frequently quoted property is the breakdown electric field strength, E_{max}. This property determines how high the largest field in the material may be before material breakdown occurs. This type of breakdown is obviously referred to as catastrophic breakdown. Curiously, the absolute value of E_{max} for SiC is frequently quoted as the relative strength of the E_{max} against that of Si. Most discussions on this subject note that E_{max} of SiC is 10 times that of Si. As with Si, there exists a dependence of E_{max} with doping concentration. Thus, for a doping of approximately 10^{16} cm^{-3}, E_{max} is 2.49 MV/cm, according to a study by Kostantinov et al. [3]. For Si, the value of E_{max} is about 0.401 MV/cm for the same doping [4]. As can be seen, the value for SiC is only about a factor of six higher than that of Si and not the often-claimed 10 times higher critical field strength. Why the discrepancy? It is more correct to compare the critical strengths between devices made for the same blocking voltage. Thus, an Si device constructed for a blocking voltage of 1 kV would have a critical field strength of

about 0.2 MV/cm, which should be compared with the 2.49 MV/cm of SiC. This is where the order of magnitude larger breakdown field spec comes from.

1.1.4 Saturated Drift Velocity

For high-frequency devices, the breakdown electric field strength is not as important as the saturated drift velocity. In SiC, this is 2×10^7 cm/sec [5, 6], which is twice that of Si. A high-saturated drift velocity is advantageous in order to obtain as high-channel currents as possible for microwave devices, and clearly SiC is an ideal material for high-gain solid-state devices.

1.1.5 Thermal Conductivity

The second most important parameter for power and high-frequency device applications is the material's thermal conductivity. An increase in temperature generally leads to a change in the physical properties of the device, which normally affects the device in a negative way. Most important is the carrier mobility, which decreases with increasing temperature. Heat generated through various resistive losses during operation must thus be conducted away from the device and into the package.

It is often quoted that the thermal conductivity of SiC is higher than that of copper at room temperature. There are even claims that it is better than any metal at room temperature [7]. The thermal conductivity of copper is 4.0 W/(cm-K) [8]. That of silver is 4.18 W/(cm-K) [8]. Values of the thermal conductivity as high as 5 W/(cm-K) have been measured by Slack [9] on highly perfect Lely platelets.

More detailed studies have been made where the thermal conductivity in the different crystal directions have been determined for SiC (see Table 1.1 [5]). As can be seen, there is a dependence on the purity of the crystal as well as on the crystal direction. At the time of this study, the material was not of the high quality we see today, and more sophisticated techniques have been developed to measure thermal conductivity. Thus, as higher-quality material has been grown, values close to the theoretical values have been measured using the laser flash technique [10].

High-purity semi-insulating (SI) SiC material has the highest reported thermal conductivity with a value of 4.9 W/(cm-K). Lower values are measured for the doped crystals but they are all above 4 W/(cm-K) at room temperature [10].

Table 1.1 The Thermal Conductivity of SiC

Sample Type	*Direction*	*Carrier Concentration (cm^{-3})*	*Thermal Conductivity (W/cm K)*	
			298K	*373K*
4H SI	// c	SI	3.3	2.6
4H n	// c	2.0 E18	3.3	2.5
4H n	⊥c	5 E15	4.8	2.9
6H n	// c	1.5 E18	3.0	2.3
6H n	// c	3.5 E17	3.2	2.3
6H n	⊥c	3.5 E17	3.8	2.8
6H p	⊥c	1.4 E16	4.0	3.2
Slack	⊥c	~ 1 E17	~ 5	~ 3

Source: [5].

1.1.6 Figures of Merit

There have been several attempts to summarize the importance of various material properties to enable comparisons between materials for high-frequency and high-power applications. Johnson suggested a figure of merit, the so-called Johnson Figure of Merit (JFOM), which considers the potential power handling and high-frequency capability of a device. The JFOM takes into account the critical field and saturated drift velocity, as shown in the following equation [11].

$$JFOM = \frac{E_B^2 v_{sat}^2}{4\pi^2} \tag{1.1}$$

where E_B and v_{sat} are the breakdown field and saturated drift velocity, respectively. Unsatisfied with the JFOM ability to take the material's thermal properties into account, which, as mentioned, are specifically apparent during high-frequency operation, Keyes proposed another figure of merit, the Keyes Figure of Merit (KFOM) [12]:

$$KFOM = \kappa\sqrt{\frac{cv_{sat}}{4\pi\varepsilon}} \tag{1.2}$$

where κ, c, and ε are the thermal conductivity, the speed of light in vacuum, and the dielectric constant, respectively.

Unfortunately, neither of these equations is particularly accurate for power devices and consequently Baliga proposed a figure of merit for low-frequency applications, called the Baliga Figure of Merit (BFOM) [13]:

$$BFOM = \varepsilon\mu E_B^3 \tag{1.3}$$

where μ is the carrier low-field mobility. In Table 1.2, the figures of merit for the two most common SiC polytypes are compared with Si and GaAs. All values are normalized to Si.

1.2 History

1.2.1 Berzelius and Acheson

Jöns Jacob Berzelius is mostly known for his discovery of Si; however, he was the first person who more than likely synthesized SiC. In 1824 he published a paper where he speculated that there was a chemical bond between Si and carbide (C) in

Table 1.2 Figures of Merit for Si, GaAs, and the Two Most Common SiC Polytypes (Values Are Normalized to Si)

Material	*JFOM*	*KFOM*	*BFOM*
Si	1	1	1
GaAs	9	0.41	22
6H-SiC	900	5.0	920
4H-SiC	1,640	5.9	1,840

one of the samples he had produced [14]. Berzelius was born just outside of Linköping in Sweden, which is interesting to point out because the center of SiC research in Sweden is at the University of Linköping.

Years later, two inventors, Eugene and Alfred Cowles, invented the electric smelting furnace in 1885 [15]. This furnace was adopted by Acheson to produce suitable minerals that could substitute diamond as an abrasive and cutting material [16]. Acheson mixed coke and silica in the furnace and found a crystalline product characterized by a great hardness, refractability, and infusibility, which was shown to be a compound of carbon and silicon. Acheson called his product "carborundum" and gave it the proper formula SiC. It is interesting to note that Acheson made the first SiC for abrasive applications near the city of Pittsburgh in Pennsylvania before he moved the operation to Niagara Falls due to the better availability of electric power. Today, Pittsburgh is another center for SiC research, with the University of Pittsburgh and Carnegie Mellon University spearheading the research in the United States.

The Acheson process sometimes also includes sawdust and salt in lesser amounts together with the coke and silica. The sawdust creates channels that help impurities escape and the salt creates free chorine, which reacts with metal impurities that become volatile. Thus, the means to purify synthetic SiC have been employed since the beginning.

In the reacted mass of SiC, there are also voids or pockets that are characterized by the fact that they are lined with hexagonal-looking crystals, as illustrated in Figure 1.1. These pockets have a uniform thermal environment but with a slight gradient toward the center of the void. The environment favors growth of crystals that is close to homogeneous. The crystals are only attached in one point to the sides of the void and grow toward the center. These crystal flakes are called platelets. We

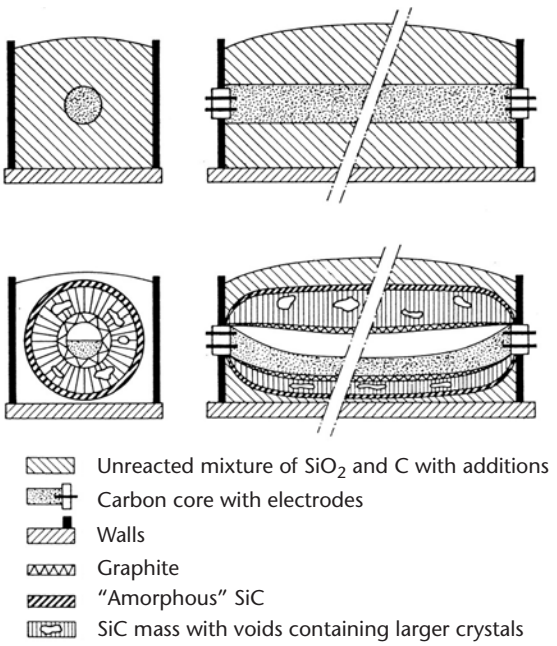


Figure 1.1 The Acheson process. The figure also shows the voids in which Acheson found the SiC crystals. (*From:* [17]. © 1963 Philips. Reprinted with permission.)

will discuss later the Lely process that produced the famous Lely Platelets, which represented the first wave of SiC technology development for electronic applications.

1.2.2 The Discovery of Polytypism

When Acheson found the hexagonal crystals in the voids, he sent some to B.W. Frazier, a professor at Lehigh University. Professor Frazier found that although the crystals were all silicon carbide, they differed in their crystalline structure. He had discovered the polytypism of SiC [18]. Polytypism will be explained in Section 1.3.2.

1.2.3 The First LED and the Lely Process

The electronic properties of SiC were investigated shortly afterward and in 1907 the first LED was produced from SiC [19]. However, the extraction of crystals was a cumbersome process that required patience, and the purity of the crystals was not controllable. As a consequence, in 1955 another crystal growth invention of significant proportions was made by J. A. Lely [20].

Lely created a mini-environment for the growth of crystals similar to the growth in the voids in the Acheson process (Figure 1.2). With Lely's method, the crystal purity and properties could, to some extent, be controlled. This created renewed interest in SiC and, at this time, SiC was even more popular than silicon and germanium. This would soon change, as we all know, mainly due to the difficulty at that time in processing high-purity SiC substrates. Until this substrate issue was solved, SiC was relegated to the arena of material scientists and physicists, who fortunately kept the science of SiC alive until technology could give it a push to commercial use.

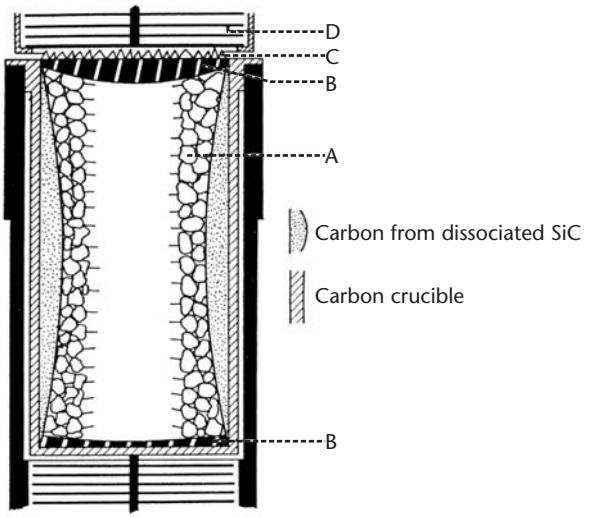


Figure 1.2 The Lely process simulates the voids in the Acheson process, yielding the hexagonal crystals called Lely Platelets. (*From:* [17]. © 1963 Philips. Reprinted with permission.)

1.2.4 The Lost Decades

In 1958, the first SiC conference was held in Boston, Massachusetts. However, after this, the interest in SiC rapidly declined and the 1960s and 1970s are characterized by a low interest in SiC. Research was still ongoing, mainly in the former Soviet Union. In the United States, the work done by Westinghouse and the University of Pittsburgh is primarily notable. Indeed, the photoluminescence studies made by Choyke, Patrick, and Hamilton are still very relevant and often cited [21].

1.2.5 The Second Wave

In the late 1970s, a very important invention—the seeded sublimation growth [22, 23]—was made in Russia by Tairov and Tsvetkov. Unlike the Lely process and the growth in the Acheson voids, where the growth is conducted under close-to-uniform thermal conditions, Tairov and Tsvetkov introduced a seed crystal and forced material transport from the source to the seed by a thermal gradient (Figure 1.3). The growth rates increased markedly and seeds of larger diameters and lengths could be made. The produced boules could be sliced and polished. The SiC wafer was born.

Another major invention that came only two years later was the ability to grow epitaxial SiC on Si substrates [24]. Research on SiC gained new speed, but it was a spark that never really caught on. However, there was generally a greater awareness of SiC and its potential, which was important for the years to come.

1.2.6 The Third Wave

In 1987, another milestone occurred when high-quality epitaxy could be made at low temperatures on off-axis substrates using "step-controlled epitaxy" [24]. Cree, Inc., was founded in 1989 as a result of this breakthrough. It manufactured the first commercial blue SiC LEDs and began to sell SiC wafers as well. At the same time, the company generated demonstrators for power devices and high-frequency devices. This was the beginning of the third and last wave of SiC. Along with improved epitaxy, continuous improvement of the diameter and quality of the wafers, and device milestones, this third wave has not died out but continues to grow in strength.

The commercial potential of SiC has to date mainly been in the materials arena. SiC is used as substrate for LEDs made from GaN, which is the largest market of semiconductor-grade SiC. Recently Infineon launched its Schottky diode product

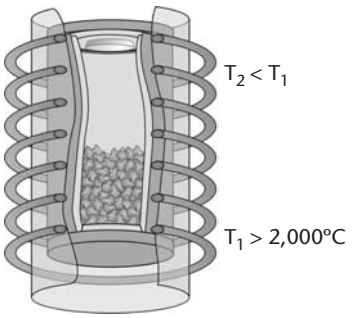


Figure 1.3 The seeded sublimation growth or modified Lely growth invented by Tairov and Tsvetkov.

line made from SiC and Cree has also come out with a Schottky diode as well as high-frequency MESFETs. The future for SiC looks very bright indeed now that commercial products have hit the marketplace!

1.3 Crystalline Structure

1.3.1 Basic Structure

The basic building block of a silicon carbide crystal is the tetrahedron of four carbon atoms with a silicon atom in the center (Figure 1.4). There also exists a second type rotated 180° with respect to the first. The distance between the carbon and silicon atom is 1.89Å and the distance between the carbon atoms is 3.08Å [6]. SiC crystals are constructed with these units joining at the corners.

1.3.2 Polytypism

Silicon carbide exhibits a two-dimensional polymorphism called polytypism. All polytypes have a hexagonal frame of SiC bilayers. The hexagonal frame should be viewed as sheets of spheres of the same radius and the radii touching, as illustrated in Figure 1.5. The sheets are the same for all lattice planes. However, the relative position of the plane directly above or below are shifted somewhat to fit in the "valleys" of the adjacent sheet in a close-packed arrangement. Hence, there are two inequivalent positions for the adjacent sheets.

By referencing the possible positions as A, B, and C, we can begin constructing polytypes by arranging the sheets in a specific repetitive order. Thus, the only cubic polytype in SiC is 3C-SiC, which has the stacking sequence ABCABC… The simplest hexagonal structure we can build is 2H, which has a stacking sequence ABAB… The two important polytypes, 6H-SiC and 4H-SiC, have stacking sequences ABCACBABCACB… and ABCBABCB…, respectively.

The number in the notation of the resulting crystal structure determines the number of layers before the sequence repeats itself, and the letter determines the resulting structure of the crystal: C for cubic, H for hexagonal, and R for rhomohedral.

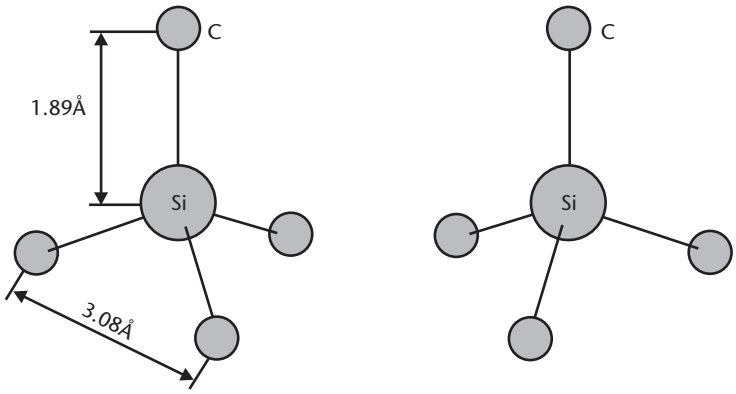


Figure 1.4 The characteristic tetrahedron building block of all SiC crystals. Four carbon atoms are covalently bonded with a silicon atom in the center. Two types exist. One is rotated 180° around the *c*-axis with respect to the other, as shown.

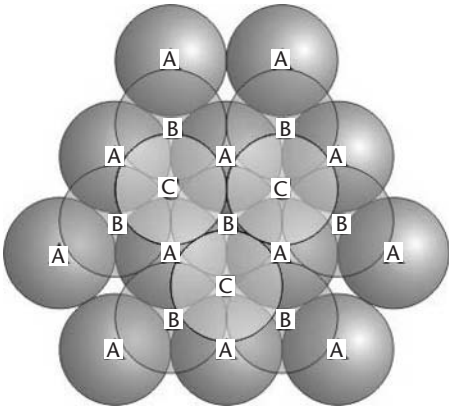


Figure 1.5 Illustration of three close-packed planes of spheres. The first layer is a layer of "A" atoms, followed by a layer of atoms on a "B" position, with a layer of atoms on "C" positions on top of that. The resulting structure in this example is 3C-SiC.

All polytypes are SiC of equal proportions of silicon and carbon atoms, but due to the fact that the stacking sequence between the planes differs, the electronic and optical properties differ. The bandgap is, for instance, 2.39 eV for 3C-SiC, 3.023 eV for 6H-SiC, and 3.265 eV for 4H-SiC [2].

The unit cell for the different polytypes will naturally vary, as will the number of atoms per unit cell. This will affect the number of electronic bands and the phonon branches for a given polytype.

1.3.3 Impurities in Different Polytypes

A very striking and beautiful feature of polytypism is the behavior of impurity atoms. In Figure 1.6, it may be seen that the sites are not equivalent in the hexagonal polytypes 6H-SiC and 4H-SiC. The difference is in the second-nearest neighbors.

A nitrogen atom substituting a carbon atom in the lattice can either occupy a "k" site or an "h" site in 4H-SiC. The k site is a lattice site that displays cubic symmetry, whereas the h site has hexagonal symmetry. The immediate vicinity of a nitrogen atom on either site is the same, but the second-nearest neighbors to the sites are different, which creates a slightly different core binding energy. Thus, 4H-SiC has two binding energies for the nitrogen donor, which has consequences when designing devices. 6H-SiC has three energy levels for nitrogen and 3C-SiC has only one. More complex polytypes such as rhombohedral (15R-SiC) has no less than five binding energies, although only four have been identified.

The photoluminescence (PL) spectrum in Figure 1.7 shows a number of lines related to nitrogen-bound excitons and free excitons. SiC has an indirect bandgap, thus the exciton-related luminescence is often assisted by a phonon. Bound exciton luminescence without phonon assistance can, however, occur because conservation in momentum can be accomplished with the help of the core or the nucleus of the nitrogen atom. That is why the zero phonon lines of the nitrogen atom are seen, denoted P_0 and Q_0, in the spectrum but not the zero phonon line of the free exciton.

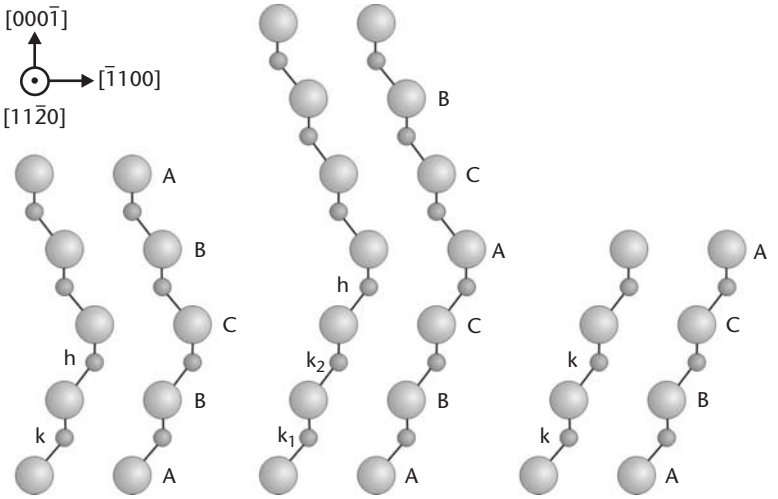


Figure 1.6 The three most common polytypes in SiC viewed in the [11$\bar{2}$0] plane. From left to right, 4H-SiC, 6H-SiC, and 3C-SiC; *k* and *h* denote crystal symmetry points that are cubic and hexagonal, respectively.

The binding energies for the hexagonal and cubic nitrogen impurities are 59 meV and 102 meV, respectively [2]. According to the effective mass approximation [25], the binding energy of an electron bound to a nitrogen atom in 4H-SiC would be:

$$E_D = 13.6\frac{Z^2 m^*}{n^2 \varepsilon_r^2 m_0}\,\text{eV} \approx 6.07\ \text{meV} \tag{1.4}$$

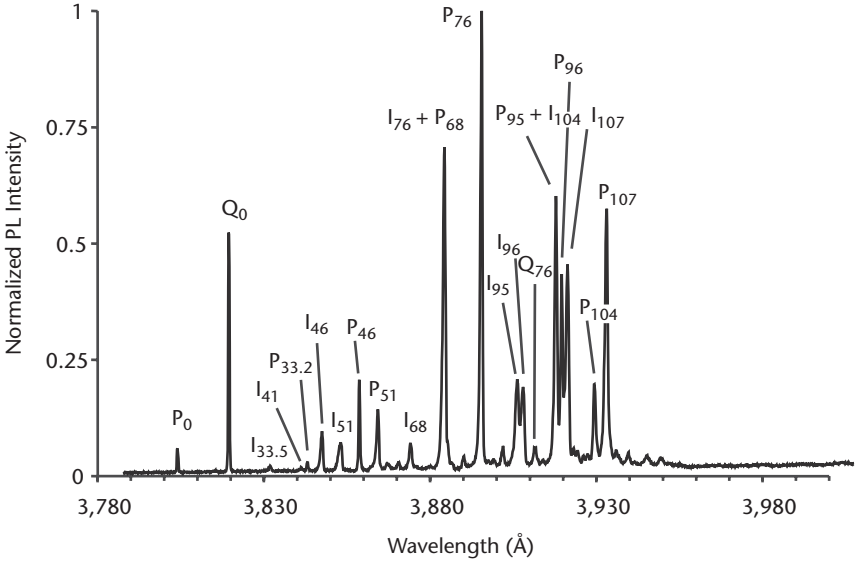


Figure 1.7 Near-band-edge photoluminescence spectrum of 4H-SiC showing the bound exciton-related luminescence denoted P_h and Q_h (where h is the energy in meV of the phonon involved in the transition) and free exciton-related luminescence denoted I_h. (Data provided by Docent Anne Henry at Linköping University.)

where m^* and ε_r are the effective mass and dielectric constant, respectively. Z is the charge that is equal to 1 in this example and n is an integer equal to 1 for the ground state. The discrepancy between the actual binding energy, 59 meV, and what the effective mass approximation predicts is taken up by the core and is referred to as the central cell correction. In this example, the central cell correction is about 53 meV.

Defects with large central cell correction have very localized wave functions. The larger the correction, the more localized the wave function and the higher the probability of interaction between the core (or central cell) and the electron and/or the exciton bound to the defect. Hence the reason why the P_0 line is so much smaller than the Q_0 line in the spectrum, as well as the reason why the phonon replicas to the Q-line, is simply a matter of probability, since the central cell correction is so much larger for a nitrogen defect on a cubic site than a hexagonal site.

A useful feature of photoluminescence that is not limited to but very apparent in SiC is the ratio between the free exciton and bound exciton luminescence, which can give an accurate determination of the level of doping once properly calibrated [26]. In a perfectly pure crystal, the electron-hole pairs created through the absorption of above bandgap photons would bind together to form free excitons. These would move freely in the crystal until they recombine and possibly generate some light in the recombination process. If we do the same in a crystal with a small amount of nitrogen in it, some of the free excitons will likely hit on a nitrogen defect, which will attract the free exciton. The free exciton will lose some of its energy and bind to the defect center into a four-particle complex called the bound exciton. The four particles are the electron-hole pair of the free exciton, the electron of the nitrogen defect, and the core of the nitrogen atom. The bound exciton will, of course, also recombine and emit some light. Thus, by comparing the ratio between the free exciton and bound exciton luminescence, the doping level can be determined.

The paper by Henry et al. [26] continues to describe how PL may be used at higher doping levels where the free exciton is no longer seen by comparing the Q_0 line and the P_{76} line. In the very high doping range, the authors correlated successfully the position of a broad nitrogen-related luminescence band with the doping concentration.

1.4 Crystal Growth

1.4.1 Seeded Sublimation Growth

1.4.1.1 General Principle

As previously mentioned in Section 1.2, Tairov and Tsvetkov [22] invented seeded sublimation growth in 1978. The technique is almost exclusively used today to manufacture SiC wafers.

The principle is simple. A graphite crucible is partially filled with SiC powder and a seed is attached on the lid of the crucible. The whole system is closed and heated up to temperatures above which SiC starts to sublime appreciably. A thermal gradient is applied such that the seed is slightly colder than the powder source. Material will thus transport from the source to the seed where it will condense. The principal constituents during sublimation are Si, Si_2C, and SiC_2 and the ratio between them is determined by the temperature.

The control of the process is complicated and much effort has been spent to optimize the process. The pressure is kept low to enhance the material transport, as is nicely illustrated by Maltsev et al. in Figure 1.8 [27]. Typically, the pressure is kept below 50 mbar. In a study by Barrett et al., the dependence of the growth rate on the system pressure was analyzed [28]. They could determine that convective effects were present at pressures above 20 Torr (approximately 26.7 mbar). Below 20 Torr the vapor transport is diffusive, according to their study.

The temperature and temperature gradient are naturally very important factors for the growth. The growth rate is exponentially increasing with increasing temperature. Typical trends are comprehensively illustrated by Vodakov et al. [29], Barrett et al. [28], and Maltsev et al. [27].

1.4.1.2 Substrate Diameter

Two major challenges for SiC bulk crystals are the manufacture of large-diameter, high-quality wafers and the manufacture of SI wafers. The diameter is rapidly increasing and 4-inch wafers have already been demonstrated. The increase in wafer diameter is significantly faster than that experienced for Si and GaAs, partly as a result of the knowledge base established for these technologies [30]. There is no doubt that SiC, with the same diameter as silicon wafers, will be available in the not-too-distant future.

1.4.1.3 Semi-Insulating Substrates

The second challenge in making SI SiC started initially by attempting to make the crystals as pure as possible to increase the resistivity, as was done by Barrett et al. [28]. It was later discovered that the introduction of specific deep-level dopants into the SiC lattice created deep traps that captures free carriers [31]. The dopant of choice for these compensated crystals was vanadium, which was found to compensate shallow acceptors. Therefore, during growth, the material needs to be doped p-type by the addition of boron or aluminum as well as introducing vanadium in larger amounts than the p-type dopant. Unfortunately, this created some problems with yield and defects due to the large amounts of impurities present in the crystal. Nevertheless, very high resistivities exceeding 10^{15} Ω-cm were obtained at room temperature. The activation energy of the vanadium trap was determined to be 1.18 eV.

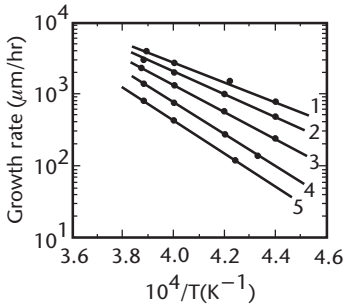


Figure 1.8 The temperature dependence on the growth rate is shown here for different Ar pressures. The residual pressures are for curve: 1–10, 2–35, 3–50, 4–75, and 5–100 Torr. (*From:* [27]. © 1996 Institue of Physics Publishing. Reprinted with permission.)

It is hard to understand the tremendous interest in the vanadium doped crystals since, in 1993, the Westinghouse Science and Technology Center was already producing 6H-SiC wafers with resistivities as high as 10^5 Ω-cm without the introduction of impurities by simply growing the crystals as purely as it could achieve [28]. It is particularly surprising in view of the fact that it was the same group that first introduced the vanadium doping. It is unfortunate that they did not realize that the most promising and much superior approach was to continue to improve the purity of the crystals as much as possible.

Other than poor crystalline quality and yield problems, there was one more problem with the vanadium doped SI SiC wafers; they did not work for high-frequency applications due to excessive trapping of electrons. A very elegant demonstration of this trapping can be seen in the publication by Sghaier et al., where the degradation in performance of the high-frequency device was clearly seen and it concluded that the cause for the trapping was the vanadium doped substrate [32].

Then, in 1999, the high-frequency community, in desperate need of better semi-insulating substrates, regained their confidence due to some interesting results where very pure, vanadium-free crystals had been grown that displayed SI behavior [33]. The authors found a deep level with an activation energy of 1.1 eV, though they had no clear identification of the identity of the defect. However, they speculated that it was intrinsic in nature. The resistivity was outstanding, demonstrating a resistivity in excess of 10^7 Ω-cm at 300°C, which is high enough for most power RF applications.

Another even more interesting development was occurring at the same time. This was the development of a new growth technique, called the High Temperature Chemical Vapor Deposition (HTCVD) technique [34], that produced crystals that were intrinsically semi-insulating. In a paper by Ellison et al. [34], the authors reported on a defect with an activation energy of 1.15 eV yielding an extrapolated room temperature resistivity in excess of 10^9 Ω-cm.

Further work showed that several intrinsic defects can contribute to the semi-insulating properties of the crystal, such as Si-vacancies, C-vacancies, and C-antisites. Typically, the resistivity of semi-insulating crystals containing predominately Si-vacancies is lower and the activation energy of the responsible defect is less than 1.1 eV, whereas crystals with predominately C-vacancies content have higher resistivities and the activation energy is around 1.4 eV [35]. Lately, photo-electron paramagnetic resonance (EPR) measurements revealed that the carbon vacancy acts as a deep donor with an activation energy of 1.47 eV [36]. This provides to date the strongest evidence that C-vacancies play a role in SiC similar to the well-known EL2 deep level in GaAs for producing high-purity semi-insulating wafers.

Now, 2-inch SI wafers without vanadium doping are sold commercially from several sources. Vanadium doped crystals will rapidly disappear and soon only be used as displays in museums or as book rests.

1.4.1.4 Prospect

A lot of research is being conducted on the seeded sublimation growth technique. The material properties are improving steadily and there should be no reason for worries. Yet, one worry is the need for off-axis substrates for high-quality epitaxial

growth. The current standard of 8° off-axis from the [0001] plane on the 4H-SiC wafers was introduced in 1995 by Cree, since it had seen an improvement in the epitaxy when the off-axis angle was increased from 3.5° (which is still the standard miscut for 6H-SiC). At that time, only 30-mm wafers were available commercially, and it was not a big problem to slice the wafers somewhat more off-axis. It was only a matter of 4-mm lost material in total from the grown boule. On a 100-mm wafer, the amount of lost material is no less than 14 mm. Considering that most boules in the world are grown on-axis parallel to the *c*-axis and that the length is limited to approximately 25–30 mm, it is going to cause significant heartache to slice the boule 8° off-axis and lose half of the material.

The trend must be to reduce the off-axis angle. Fortunately, if we peek at what has happened previously in the Si and GaAs worlds, the standard was to use off-axis substrates initially, but as the material quality improved, the need for off-axis substrates was reduced and on-axis substrates are now used for epitaxy. This is likely going to be the trend in SiC too. The need for better epitaxial procedures and higher-quality substrates than what is available today is important.

Boule lengths are also likely to increase. More powder may be introduced into the growth chamber, however, thermal considerations become an issue as the boules increase too much in length. Even if the surface is kept at constant distance in the chamber, the distance from the source will vary as the material is depleted and the growth conditions change.

The source material will release excess silicon in the beginning of the growth cycle and be more carbon-rich in the end due to preferential depletion of silicon. This is a known problem and it is a matter of detailed control and an understanding of the dynamic transport mechanisms in combination with thermodynamics. Nevertheless, the result is invariably that SiC boules grown by seeded sublimation growth are Si-rich in the beginning and C-rich near the end, which creates yield issues. Simulation of the process is necessary to improve the situation.

The turnaround time for a boule growth run is several days. It takes time to prepare the source, load the crucible, attach the seed, evacuate the system carefully, gradually heat up the crucible under controlled conditions, and finally grow the boule and then cool down. The turnaround time itself is not a problem, however, the cost of manufacturing a wafer needs to decrease so the price of the wafers can be reduced in order for SiC to gain acceptance in the market.

Seeded sublimation growth is a mature and needed tool for the SiC industry today. There are still major challenges. Specifically, boules will need to be grown on off-axis substrates, or the off-axis angle needs to be eliminated, which will only be possible if a combined effort of improving wafer quality, polishing procedures, and epitaxial procedures is pursued.

1.4.2 High Temperature Chemical Vapor Deposition

In 1995, a new technique, called HTCVD, was presented for the growth of SiC boules. This technique uses gases instead of a powder as source material. It was first presented at ICSCRM '95 in Kyoto, Japan, but the first publication of HTCVD in a journal was in 1996 [37]. More recent publications are available where the technique is better described [38].

1.4.2.1 General Principle

The HTCVD apparatus can be described as consisting of three separate zones: An entrance zone, a sublimation zone, and a growth (or condensation) zone. The gases used are mainly silane, ethylene, and a helium carrier. The carrier flow is very low. A schematic of the HTCVD system is shown in Figure 1.9.

Silane and ethylene are present at very high concentrations so that homogeneous nucleation dominates the process. As the gases enter into the hot part of the injector, the silane will decompose and form small Si liquid droplets or solid microcrystals, depending on the temperature. The ethylene will also take part in the reaction, forming microparticles of Si_xC_y. It has been noted [39] that even a small addition of hydrocarbons converts the Si droplets to stable particles of Si_xC_y (or nonstoichiometric SiC). The stability may, in a hand-waving circumstantial way, be intuitively understood from a solubility point of view. The solubility of carbon in silicon is very low, thus, when carbon is added to the Si droplets, the phase will be solid rather than liquid.

The process can work without additions of a hydrocarbon, in which case the carbon is supplied through a reaction between the hot silicon and the graphite walls. This is usually not the preferred growth mode and additions of hydrocarbons are needed to obtain a high growth rate.

The formed microparticles of Si_xC_y will move into the hot chamber or the sublimation zone with the aid of the inert helium carrier gas. Once in the sublimation zone, the microparticles will sublime to form Si, Si_2C, and SiC_2, as in the case of seeded sublimation growth. A thermal gradient is applied, as illustrated in Figure 1.9, so that the sublimed species will condense on the seed, as in the case of seeded sublimation growth.

There are similarities between seeded sublimation growth and HTCVD in that solid particles sublimate in the reactor and the vapor condenses on a seed crystal maintained at a lower temperature. However, the differences are quite dramatic and the outcome even more so. Take, for instance, the dynamics governing the growth

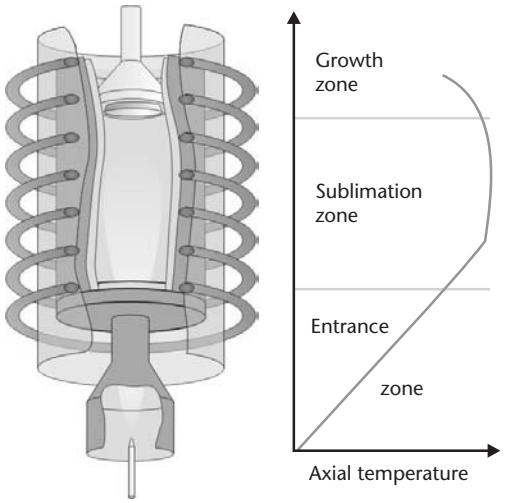


Figure 1.9 HTCVD process. Microparticles are formed in the inlet region of the system and transported to the sublimation zone, where the particles sublime to finally condense on the growth surface.

rate. The heating of the particles in the sublimation zone must be efficient so that they sublime properly. Insufficient sublimation results in particles appearing as "smoke" coming out from the crucible. This is obviously not a good scenario and material quality, as well as growth rate, will suffer.

The growth rate is naturally influenced by the amount of input precursors, however, too high concentrations will give rise to too large nuclei, which will be difficult to sublime. As may have been deduced, if the thermal gradient between the seed and the sublimation zone is increased, the potential for sublimation will increase so that larger microparticles may be sublimed, thus larger amounts of precursors may be introduced and the growth rate will increase.

The process is usually carried out at somewhat reduced pressures, though not at as low a pressure as seeded sublimation growth, where the pressure is greatly reduced to aid the material transport. HTCVD has its own material transport through the small but steady flow of helium, so reduced pressure is not needed to enhance growth species transport. However, the lower pressure will result in smaller particle sizes due to a suppression of homogeneous nucleation. Lowering the pressure will thus increase the maximum amount of precursors without observing "smoke" at the outlet.

Thus, there are several ways to improve the growth rate, as can be seen. But in the end it all comes down to the size of the particles that need to be sublimed in the sublimation zone. Typical maximum growth rates are in the order of 0.8 mm/hr–1 mm/hr.

What is also interesting about the HTCVD is the material transport. Why does the silane not decompose and grow directly on the walls of the inlet? There are two reasons for this. First, the injector is a coaxial injector, as illustrated in Figure 1.9 [40]. The silane and ethylene are transported in the inner tube, whereas there is only carrier gas in the outer tube. Thus the silane will not be in close proximity with a wall when it decomposes and will preferentially form nuclei through homogeneous nucleation. Second, the ethylene will make these particles very stable and hence they will not be prone to growth on the walls at all.

As is well known, when hydrocarbons transported in an inert gas such as helium are heated, carbon or pyrolytic graphite will deposit on the walls. In the HTCVD, the ethylene helps make the particles stable and, in doing so, carbon is transported into the chamber together with the silicon. It is a sort of symbiosis in the transport between the silicon and carbon.

1.4.2.2 Material Properties

One of the prime advantages of the HTCVD approach is the resulting crystal properties. Due to the high purity of the gases, the material comes out intrinsically semi-insulating. Also, since the source material is produced on demand, the stoichiometry can always be kept the same, unlike the case with seeded sublimation growth. This will improve the yield of the grown material.

It is also interesting to note that the technique is shown to reduce micropipes by 80% during each run [35]. The micropipes close at the interface by some type of hollow core-closing effect. Very low micropipe densities have been recorded using this technique, which is clearly much faster in improving material quality than seeded sublimation growth.

The resistivity of the SI wafers has been measured to be in excess of 10^{11} Ω-cm at room temperature [35]. As mentioned earlier, a deep level defect was found to have an activation energy of 1.4 eV. MESFETs manufactured on these wafers show an increased performance in the sense of reduced trapping, which the authors explain as being primarily due to a reduction of the shallow impurities in the material.

1.4.2.3 Challenges

Some of HTCVD's initial challenges have been solved. For example, using a coaxial injector solved the blocking of the inlet. Another issue is the purity of the graphite material, which may be overcome using properly coated graphite crucibles.

The outlet is a major problem because the material grows not only on the surface of the crystal but also around it and on the walls. When the outlet blocks, the growth must be interrupted and hence the length of the crystals is limited. Work is ongoing to solve this specific issue and it has, to some extent, been fruitful. Crystals with a length in excess of 15 mm have been grown [A. Ellison, private communication].

New problems will arise as the crystal increases. It will, for instance, be necessary to pull the crystal during growth so that the growth surface remains at the same position in the crucible. When the crystals become long the thermal profile may change and will need to be controlled. Fortunately these are all problems that can be easily managed with proper engineering design and process simulation. As a result, there appear to be no real limitations to this approach.

The growth rates today can be approximated to about 1 mm/hr, which means that roughly 20 mm of material may be grown each day, including 4 hours for the turnaround heat-up and cool-down time. Although this is better than what the seeded sublimation growth can achieve, growth rates will need to be increased further to drive wafer costs down.

The cost of manufacture is often used as an argument against HTCVD. The reactors are, as may be understood, significantly more complex and hence also more expensive, compared with seeded sublimation growth. Graphite materials are somewhat more expensive for HTCVD, whereas the gases are likely to be less expensive than high-purity powder material in bulk quantities. However, with a potentially higher throughput when using the HTCVD technique, and provided the volumes are high, it will actually be less expensive to use this technique than seeded sublimation growth since the cost will largely be driven by volumes. The cost comparison becomes even more favorable for HTCVD if the improved yields of low micropipe material, particular low micropipe SI material, are taken into account.

However, such comparison is a meaningless exercise. A comparison of silicon, sapphire, GaAs, or other established materials, rather than other SiC growth techniques, should occur instead. The blue and white LEDs can, for instance, be made on either sapphire or SiC substrates. From a performance point of view, there appear to be advantages with the SiC substrate but the substrate cost is lower on sapphire, therefore making it the most-used substrate. Granted, once larger substrates of SiC are made available, it is doubtful that the LED cost will be lower on sapphire.

Ultimately, SiC will not only be going up against sapphire but also against such giants as silicon and GaAs, which will require significant cost-reduction measures

in the materials growth for SiC to become a viable technology. HTCVD is clearly a step in the right direction, but the SiC community still has a long way to go in this regard.

1.5 Epitaxial Growth

Several techniques for epitaxial growth exist today and it is therefore beyond the scope of this chapter to explain all of them. Chemical vapor deposition (CVD) is the only technique that is used for commercial applications of SiC and the description of epitaxy will be limited to this technique.

Several different types of CVD reactors exist. The cold wall design, which used to be the most common type of reactor, is now less frequently used and the hot-wall reactor has filled its place. Some new and interesting concepts exist as well. These are referred to as chimney-type reactors. The main difference between the hot- or old-wall type reactors and the chimney-style reactor is the transport of materials, which will be explained in the following sections.

1.5.1 Chemical Vapor Deposition

CVD of SiC normally uses silane and a hydrocarbon as the precursor gases and a hydrogen carrier gas. The gases pass over a heated graphite susceptor that is coated by SiC or tantalum carbide (TaC).

The velocity of the gases is high but it is always laminar flow. Over the susceptor there will be a boundary, or stagnant, layer where the velocity gradient decreases to zero. As the gases are heated, the silane and hydrocarbon will decompose and the species will diffuse through the boundary layer to grow on the reactor walls or on the substrate. A comprehensive study of this may be found in a paper by M. Leys and H. Veenvliet [41].

The concentration of precursor gases will decrease with respect to the flow direction over the susceptor due to the consumption of growth species, which results in a tapered layer thickness. This effect is known as depletion. To compensate for the depletion it is common to taper the susceptor such that the velocity of the gases increases along the flow direction over the susceptor and thus the boundary layer will be pushed downward, resulting in a shorter diffusion for the active species to the substrate.

It is sometimes not enough to taper the susceptor to achieve good homogeneity of thickness and doping, hence other more complicated measures are applied, such as rotation of the substrate as described in the literature [42]. In this paper, the authors also use a blend of argon and hydrogen as carrier gas, which has been shown to be advantageous to achieve better homogeneity [43].

The flow of hydrogen is generally very high and the pressure is reduced. This is not so much on account of the flow dynamics but more due to reducing the homogeneous nucleation of Si, which is significant when silane is used. The silicon cluster formation was first noticed and studied in detail by Rupp et al. in a single wafer Emcore reactor with a very high thermal gradient [44].

1.5.1.1 Doping Control

This can be done by introducing nitrogen for n-type and trimethylaluminum (TMA) for p-type layers. To obtain a better range of doping, it has been elegantly demonstrated that by changing the C/Si ratio of the input gases the doping concentration will change without changing the flow of nitrogen or TMA. This effect is known as site competition [45]. Unfortunately, when changing the stoichiometry, the morphology is affected somewhat and it is therefore not always desirable to do this if thick layers are to be grown.

When doping is used and multiple layers are grown with different carrier type and conductivity, it is important that the doping level decreases rapidly after the source of the dopant is shut off. Otherwise one does not achieve abrupt junctions. This is known as the memory effect and it can be reduced by various tricks. For instance, one can vary the stoichiometry, provide a short purge without any dopant but continue to flow the normal precursor gases, or even perform an in-situ etch back before the next layer is grown. Although an Al memory effect was a concern in the early 1990s, this problem has been solved and it is no longer a concern.

1.5.1.2 Hot-Wall Reactor

Prior to the introduction of hot-wall reactors in 1993 [46], thick, low-doped layers for very high voltages had not been achieved. This type of reactor proved it possible to grow very thick, low-doped layers of good morphology and high quality, which are needed for high-voltage power devices [47].

Hot-wall CVD reactors have become increasingly popular due to the ease of obtaining high- quality layers. The stochiometry is usually selected with respect to optimum morphology and doping is varied by changing the partial pressures of the dopants.

The reactor also displays a remarkably high uniformity in both thickness and doping. Even without wafer rotation, uniformities as tight as 1% in thickness and 2% in doping have been reported [48]. More recently, rotation has been introduced, primarily to increase the capacity (i.e., to have the same high uniformity over several wafers [49]). The reproducibility was also reported to be very good, within ±10% in doping.

The behavior of the hot-wall reactor has been investigated thoroughly. A short but comprehensive study by Wagner and Irmscher captures the main points [50].

1.5.1.3 Multiwafer Reactors

Wafer rotation, as previously mentioned, has been introduced in the hot-wall reactor (see Figure 1.10), which gives it a capacity of 3×2-inch (that is, three 2-inch wafers can be run simultaneously to increase reactor throughput). The uniformity in this reactor is routinely 1–2% in thickness and 5–7% in doping [Rune Berge, Epigress, private communication].

Aixtron has manufactured both a cold-wall planetary reactor and a hot-wall planetary reactor for 7×2-inch wafer capacity or 5×3-inch. The cold-wall reactor has provided very good uniformities and its performance has been described in

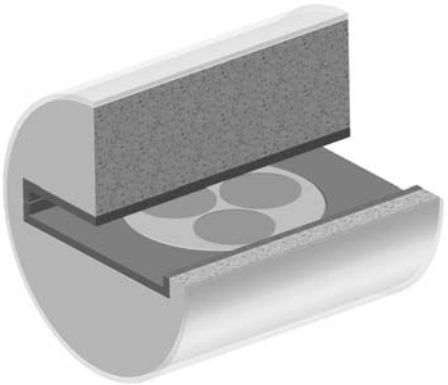


Figure 1.10 The hot-wall reactor with a 3 × 2-inch rotating platter. The mode of rotation is generally gas-foil rotation.

several papers [51]. For the 7 × 2-inch reactor, they report on thickness uniformities around 4% and doping uniformities of 5% and 7%, depending on the doping level.

The 7 × 2-inch hot-wall version has shown outstanding uniformities and high material quality [52]. Uniformities in thickness of 0.4%, and doping of 5–6% have been demonstrated. Wafer-to-wafer uniformities are 0.6% in thickness and 3.6% in doping, which are outstanding results. Results for the 5 × 3-inch version of the same reactor are meager but the hot-wall version of the 5 × 3-inch reactor behaves much the same as the 7 × 2-inch (i.e., approximately the same uniformities [Rune Berge, Epigress, private communication].

1.5.1.4 The Chimney Reactor

An elegant new reactor concept for the growth of SiC epitaxial layers was introduced by Ellison et al. [34, 53] and is called the chimney reactor. This technique is similar to the HTCVD technique in that it is a vertical system and the material transport is achieved by allowing large clusters of Si to form. This is achieved by reducing the carrier flow, which thereby increases the partial pressure of the precursors. Hydrogen is used as the carrier gas but, again, only very small flow rates are required.

The silicon clusters are formed in the inlet region at relatively low temperatures. As the temperature increases the formed Si clusters will thermally decompose and be available for growth. This is very similar to HTCVD; however, in this case there is no sublimation, only a decomposition of the Si clusters.

Very high growth rates and outstanding purity has been achieved using this technique. Growth rates between 15–50 μm/hr and background doping in the low 10^{13} cm^{-3} have been reported by Zhang et al. [54].

Typically, the temperatures used for growth are somewhat higher than those used in regular CVD, however, it need not be much higher. The high growth rates are obtained at higher temperatures as the dissociation of the Si clusters is more efficient.

Other groups have also worked on the same concept. Specifically, Tsuchida et al. have achieved very good results using this technique [55]. Their reactor is heated through radiation using a cylindrical heating element surrounding a wedge-shaped substrate holder. The substrate temperature is lower (around 1,600°C) than what is usually used for chimney reactors but the surrounding heating element is significantly hotter.

Kimoto et al. has also achieved high-quality results using the chimney technique. They report doping concentrations below 10^{13} cm^{-3} [56].

1.6 Defects

It is important to discuss the major defects present in SiC. The intent is not to create an encyclopedia of SiC defects but rather highlight two that have become the favorite lament of device researchers and which create significant heartache and debate.

1.6.1 Micropipes

In previous sections, micropipes have been discussed, and these are indeed the most important defect present in SiC. Micropipes may be caused by several screw dislocations bunching together to form a giant screw dislocation, making it energetically favorable to open up a hollow core in the center [57]. A different way of forming micropipes may be simply by system contamination, where particles are trapped in the growing crystal, thus forming a micropipe, as described by Augustine et al. [58]. The third way micropipes form, according to the same authors, is by vacancy condensation at a helical dislocation.

Micropipes are basically a hollow core penetrating the entire wafer along the *c*-axis direction. Placing any device directly on top of the micropipe is bound to cause failure. These defects are particularly disturbing for large-area devices such as high-power devices because the probability of placing your device on a micropipe increases, as shown in Figure 1.11. To obtain decent yields in excess of, say, 80% for a 10-A Schottky device, micropipe densities must be in the order of 8 mp/cm^2. For a 50-A Schottky one would need material with a micropipe density better than 2 mp/cm^2.

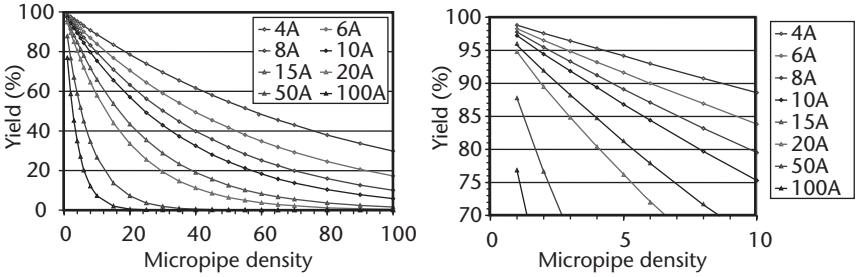


Figure 1.11 Simulation of the yield of various sizes of Schottky diodes versus micropipe density for randomly distributed micropipes. The right-hand figure is a detail of the left-hand figure. Micropipes located on the active area or JTE region render a failed device, however, micropipes located in between the devices are considered harmless.

Figure 1.11 is a simulation of randomly distributed micropipes, however, there is normally a tendency to cluster the micropipes, which would give somewhat better yields. Also, a significant amount of micropipes land in between the devices where the wafers are diced and these are considered harmless in the simulation.

There is interesting research going on with respect to minimizing the micropipes by growing boules on the [03$\bar{3}$8] plane [59]. The plan is to let the micropipes and stacking faults propagate diagonally to prevent them from reaching the top surface of the boule. The researchers did indeed find micropipe-free areas and it will be interesting to follow future work on this.

Similar research has been done on planes perpendicular to the [0001] basal plane. Micropipe-free material has been grown, however, new defects appear as reported by the authors [60].

1.6.2 Stacking Faults

The second defect that needs to be discussed does not have as grand a history as micropipes because it only recently became popular. This defect is the stacking fault, which creates degradation of bipolar devices. Reports by Lendenmann [61] and Bergman [62] reveal that a PiN diode operating under normal conditions begins to degrade. While the diode is operating, defects, which the authors interpret as stacking faults, evolve with an accompanying reduction in carrier lifetime. The defects thus act as recombination centers for the carriers.

Furthermore, the stacking order has been identified as that of the 3C-SiC polytype and, according to the study by Stahlbush, an explanation to the recombinative behavior of the stacking fault is that the 3C-SiC, having a lower bandgap than 4H-SiC, acts as a quantum well, thereby enhancing the recombination [63]. It is a very serious materials issue that must be solved prior to the realization of commercial bipolar devices.

Work is ongoing to reduce defects in SiC material. One of the more interesting concepts is the reduction of defects through epitaxial growth on porous SiC substrates [64]. This approach has clearly demonstrated a reduction in intrinsic defects, as evidenced by photoluminescence measurements. It is too early to tell whether this technique can provide a path forward for the bipolar devices but it will clearly find its applicability in several areas where SiC will have a market.

1.7 Commercial Outlook

Silicon carbide has a clear place in society today, yet it has only one major commercial application today, which basically is materials or, more specifically, substrates for LED applications. This is perhaps not such a glamorous place to be in the commercial market but it does represent a significant starting point for SiC.

The military has had SiC on its radar screen for many years for radar applications, electronic warfare, more electric airplanes, more electric ships, more electric combat vehicles, and rail guns (which, we suppose, are also of the “more electric” variety). These applications require high-quality materials and large wafer sizes. Thanks to the military and its requirements for large wafers of high quality, the

commercial SiC sector has started to wake up and aggressively pursue product development to meet these needs.

1.7.1 High-Frequency Applications

Cree is currently offering MESFET devices geared toward the cellular base station market. It is estimated by Rutberg and Co. that the RF transistor market will be as large as $1.9 billion by 2006. Cell-phone base stations are clearly the biggest market for high-frequency devices. It will not be meaningful to replace *all* the transistors in a base station with SiC MESFETs or GaN high-electron mobility transistors (HEMTs), but a conservative estimate is that SiC will capture about 20% of this market, which would be approximately $400 million. However, due to the advantages of using SiC (or GaN), a higher average selling price (ASP) will be accepted by customers and it is therefore more accurate to estimate the SiC and GaN high-frequency market to be in excess of $1 billion.

A recently published and interesting market study by Yole Développement estimates the high-frequency market for SiC MESFETs to be $400 million in 2007 [65]. This also takes into account a dramatic annual price reduction of the components.

The jury is still out whether it will be SiC MESFETs or GaN HEMTs that capture the bulk of this large market. Silicon carbide MESFETs have overcome their initial technological problems and have a clear potential to capture this market. However, GaN HEMTs show the highest power densities and highest frequency capabilities but are marred by an unfortunate instability caused by highly faulted materials.

A GaN substrate would be a help in this respect but it would need to be semi-insulating. In addition, GaN has a poor thermal conductivity and is not very suitable due to this negative material property. Aluminum nitride substrates may become the substrate of choice for GaN high-frequency applications. It has a reasonable thermal conductivity and is intrinsically semi-insulating but only time will tell.

Unlike SiC, GaN is still not mature for the market. There is no doubt that the technological issues will be overcome but it will take some time. And finally, since money rules in the ruthless commercial world, will the manufacturing cost of GaN HEMTs be low enough to capture a lion's share or just a niche portion of the market?

1.7.1.1 High-Power Applications

By far the biggest application for SiC technology is the high-power electronics market. It may not be as glamorous as the high-frequency or the optoelectronic markets but it is big. The current size of the power-device market is $16 billion [65] and it is growing at a rate of almost 10% per year [66]. The question on everyone's mind is how big will the SiC share be?

When determining where the power is used, it may come as a surprise that most power is used in a relatively narrow range between a couple of hundred volts to a couple of thousand volts and between an amp to several hundred amps, as can be seen in Figure 1.12. This range lies within the sweet spot for SiC unipolar devices.

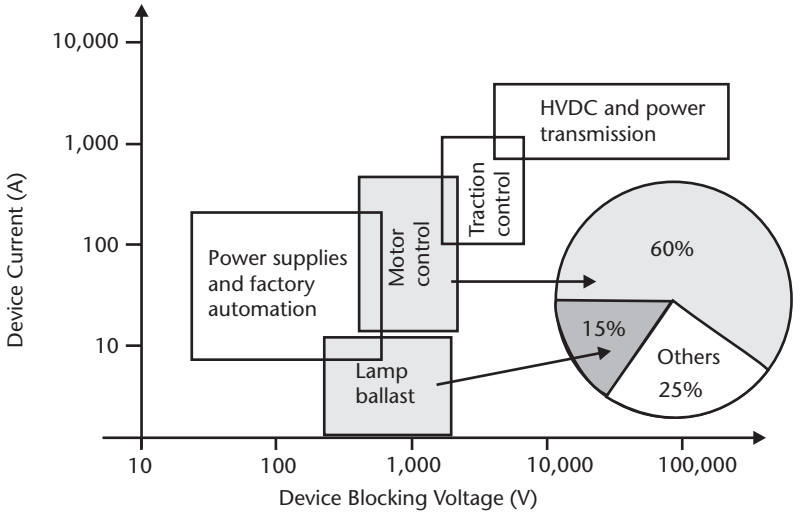


Figure 1.12 The application for power devices relative to their blocking voltage and current ratings. Most power is used in a comparatively narrow range of voltage (200–2,000V) and between 1A to several hundred amps. This lies within the sweet spot for SiC unipolar devices. (*After:* [67].)

Thus, if we begin substituting the old-fashioned Si devices with fresh new ultra-fast SiC unipolar devices, more than 75% of the power will go through an SiC device.

This will be a major deal for the power industry on account of the superior performance of the SiC devices. If we assume that we improve the efficiency of the Si circuits with another 5%, approximately $50 billion will be saved in power consumption annually in the United States as a result. On top of this are additional savings due to the fact that the air-conditioning needed to remove the heat that is no longer generated is dramatically reduced.

Unfortunately, where the power is used is not where the bulk of power devices are sold. Most devices that are sold are for low-voltage (below 300V) and low-current applications in markets where SiC is not competitive.

In the range between 300–600V, the picture is a little different, as can be seen in Figure 1.13. Approximately one-third of this market will be accessible for SiC (i.e., $1.32 billion of the Si share). Above 600V, it is estimated that SiC will capture 70% of the market (i.e., $1.68 billion of the Si share).

As with high-frequency applications, the power-device market can support the higher ASP of SiC power devices. A factor of approximately 3–5 times higher ASP is expected. Thus, the $3 billion Si share would convert into an approximately $10 billion SiC power-device share when the market is fully developed. A customer will be willing to pay a higher price for the SiC devices because there will be significantly larger savings on the passive components and on the cooling devices due to the higher switching frequency and increased efficiency.

The market study by Yole estimates the SiC power-device market to be close to $600 million in 2007 and growing rapidly. This also covers bipolar devices, which are at higher voltages.

Infineon, as well as Cree, has already launched its first power-device products—Schottky diodes. The SiC Schottky diode market alone is estimated to be around $250 million by 2007. An interesting observation with respect to SiC

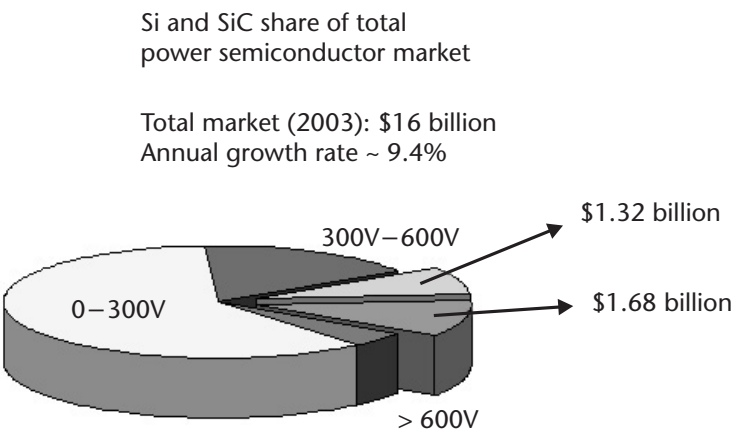


Figure 1.13 Distribution of the power-device market with respect to voltage. Below 300V, SiC will not play a major role. In the region of 300–600V, SiC is estimated to capture roughly one-third of the market. Above 600V, SiC is estimated to capture 70% of the market.

Schottky diodes is that the invention of the very fast Si CoolMOS transistor is helping the introduction of the SiC Schottky diode. The power transistors always have a freewheeling diode in antiparallel, however, there has been no diode fast enough to match these fine Si transistors until the introduction of the SiC Schottky diode.

In the higher voltage range, SiC transistors as well as Schottky diodes will be important. Specifically, motor drives will be the main application where SiC will become a major player, especially where power conservation is of prime concern; for instance, in the drives to the electric motors for fuel-cell vehicles. The future will be very interesting and very bright.

1.8 Summary

The purpose of this chapter was to briefly introduce the reader to the exciting world of SiC technology. An attempt has been made to both excite the audience with the impressive potential that SiC has, while painting a realistic picture of the challenges that exist that must be solved if SiC is to enter and remain in the modern marketplace. Indeed, the philosophy of this book is along these lines and the topics were carefully chosen with this in mind. Now that an overview of the SiC field has been provided, we will delve into two exciting applications of SiC where this material system clearly has an advantage over traditional solid-state technologies such as Si or GaAs. These are robust, high-temperature gas sensors (Chapter 2) and electric motor drive electronics (Chapter 3). Before reviewing some recent developments in the more traditional SiC electronic devices, Chapter 4 is devoted to one of the critical processing steps necessary for all SiC devices—selective doping via ion implantation. This is followed by an update on MOS transistors (Chapter 5), and power RF and bipolar devices (Chapter 6). Although no single book on SiC can completely tell the whole story, the reader is encouraged to review other texts on this subject to get a clearer impression of the technology and its uses.

References

[1] Matus, L. G., et al., *Inst. Phys. Conf. Ser.*, No 137, 1993, p. 185–188.

[2] Choyke, W. J., and G. Pensl, "Physical Properties of SiC," *MRS Bulletin*, March 1997, pp. 25–29.

[3] Konstantinov, A. O., et al., "Ionization Rates and Critical Fields in 4H SiC," *Appl. Phys. Lett.*, Vol. 71, No. 1, 1997, pp. 90–92.

[4] Baliga, B. J., *Power Semiconductor Devices*, Boston, MA: PWS Publishing Company, 1996, p. 74.

[5] Allen, S. T., et al., "Recent Progress in SiC Microwave MESFETs," *Mat. Res. Symp. Proc.*, Vol. 572, 1999, pp. 15–22.

[6] Järrendahl, K., and R. Davis, "Material Properties and Characterization of SiC, Semiconductors and Semimetals," *SiC Materials and Devices*, Vol. 52, Y. S. Park, (ed.), 1998.

[7] http://www.cree.com/Products/sic_silicarb.html.

[8] Nordling, C., and J. Österman, *Physics Handbook*, 5th ed., Lund, Sweden: Studentlitteratur, 2002, pp. 28–29.

[9] Slack, G. A., *J. Appl. Phys.*, Vol. 35, 1964, p. 3460.

[10] Müller, S. G., et al., *Mat. Sci. Forum*, Vols. 389–393, 2002, pp. 23–28.

[11] Johnson, E. O., *RCA Rv.*, Vol. 26, 1965, p. 163.

[12] Keyes, R. W., *Proc. IEEE*, Vol. 60, 1972, p. 225.

[13] Baliga, B. J., *J. Appl. Phys.*, Vol. 53, 1982, p. 1759.

[14] Berzelius, J. J., *Ann. Phys., Lpz.*, Vol. 1, 1824, p. 169.

[15] Cowles, A. H., and E. H. Cowles, U.S. Patent 319945, 1885.

[16] Acheson, A. G., Engl. Patent 17911, 1892.

[17] Knippenberg, W. F., *Philips Research Reports*, Vol. 18, No. 3, 1963, pp. 161–274.

[18] Frazier, B. W., *J. Franklin Inst.*, 1893, p. 287.

[19] Round, H. J., *Electrical World*, Vol. 19, 1907, p. 309.

[20] Lely, J. A., *Berichte der Deutschen Keramischen Gesellshaft* e.V, Vol. 32, 1955, p. 229.

[21] Patrick, L., W. J. Choyke, and D. R. Hamilton, *Phys. Rev. A*, Vol. 137, pp. A1515–A1520.

[22] Tairov, Y. M., and V. F. Tsvetkov, *J. Cryst. Growth*, Vol. 43, 1978, p. 209.

[23] Matsunami, H., S. Nishino, and H. Ono, *IEEE Trans. Electron Devices*, ED-28, 1981, p. 1235.

[24] Kuroda, N., et al., "Ext. Abstr.," *19th Conf. on Solid State Devices and Mater.*, 1987, p. 227.

[25] Wolfe, C. M., N. Holonyak, Jr., and G. E. Stillman, *Physical Properties of Semiconductors*, Upper Saddle River, NJ: Prentice Hall, 1989, p. 86.

[26] Henry, A., et al., *Mat. Sci. Forum*, Vols. 389–393, 2002, p. 593.

[27] Maltsev, A. A., A. Y. Maksimov, and N. K. Yushin, *Inst. Phys. Conf. Ser.*, No. 142, 1996, pp. 41–44.

[28] Barrett, D. L., *J. Cryst. Growth*, Vol. 128, 1993, pp. 358–362.

[29] Vodakov, Y. A., et al., *Phys. Stat. Sol. (b)*, Vol., 202, 1997, pp. 177–200.

[30] Powell, A. R., and L. B. Rowland, *Proc. IEEE*, Vol. 90, No. 6, June 2002.

[31] Augustine, G., et al., *Mat. Sci. Forum*, Vols. 264–268, 1998, pp. 9–12.

[32] Sghaier, N., et al., *Mat. Sci. Forum*, Vol. 389–393, 2002, p. 1363.

[33] Mitchel, W. C., et al., *Mat. Sci. Forum*, Vols. 338–342, 2000, pp. 21–24.

[34] Ellison, A., et al., *Mat. Sci. Forum*, Vols. 338–342, 2000, pp. 131– 136.

[35] Ellison, A., et al., *Mat. Sci. Forum,* Vols. 433–436, 2003, pp. 33–38.

[36] Son, N. T., et al., *Mat. Sci. Forum,* Vols. 433–436, 2003, pp. 45–50.

[37] Kordina, O., et al., *Appl. Phys. Lett.*, Vol. 69, 1996, pp. 1456–1458.

[38] Ellison, A., et al., *Mat. Re. Soc. Symp.*, Vol. 640, 2001.
[39] Ellison, A., et al., *Mat. Sci. Forum*, Vols. 264 –268, 1998, pp. 103–106.
[40] Ellison, A., et al., U.S. Patent 6,039,812, 2000.
[41] Leys, M. R., and H. Veenvliet, *J. Cryst. Growth*, Vol. 55, 1981, p. 145.
[42] Schöner, A. et al., *Mat. Sci. Forum*, Vols. 389–393, 2002, pp. 187–190.
[43] Kordina, O., K. Irvine, and M. Paisley, U.S. Patent 6,297,522, 2001.
[44] Rupp, R., et al., *Mat. Sci. Forum*, Vols. 264–268, 1998, pp. 89–96.
[45] Larkin, D. J., *Phys. Stat. Sol. (b)*, Vol. 202, 1997, p. 305.
[46] Kordina, O., et al., *Inst. Phys. Conf. Ser.*, No. 137, 1993, pp. 41–44.
[47] Kordina, O., et al., *Appl. Phys. Lett.*, 66, 1373, 1995.
[48] Paisley, M. J. et al., *Mat. Res. Soc. Symp. Proc.*, Vol. 572, 1999, p. 167.
[49] Zhang, J., et al., *J. Cryst. Growth*, Vol. 241, 2002, p. 431.
[50] Wagner, G., and K. Irmscher, *Mat. Sci. Forum*, Vols. 353–356, 2001, pp. 95–99.
[51] Nordby, H. D. Jr., et al., *Mat. Sci. Forum*, Vols. 338–342, 2000, pp. 173–176.
[52] http://www.epigress.com.
[53] Ellison, A., "Silicon Carbide Growth by High Temperature CVD Techniques," Ph.D. thesis, Linköping University, 1999.
[54] Zhang, J., A. Ellison, and E. Janzén, *Mat. Sci. Forum*, Vols. 338–342, 2000, pp. 137–140.
[55] Tsuchida, H., et al., *Mat. Sci. Forum*, Vols. 353–356, 2001, pp. 131–134.
[56] Kimoto, T., et al., *Mat. Sci. Forum*, Vols. 389–393, 2002, pp. 165–170.
[57] Frank, F. C., *Acta Crystal*, Vol. 4, 1951, pp. 497–501.
[58] Augustine, G., et al., *Phys. Stat. Sol. (b)*, Vol. 202, 1997, p. 137.
[59] Nakayama, K., et al., *Mat. Sci. Forum*, Vols. 389–393, 2002, pp. 123–126.
[60] Takahashi, J., M. Kanaya, and T. Hoshino, *Inst. Phys. Conf. Ser.*, No. 137, 1993, pp. 13–16.
[61] Lendenmann, H., et al., *Proceedings of the Ultra-Low-Loss Power Device Technology Workshop*, 2000, pp. 125–130.
[62] Bergman, J. P., et al., *Mat. Sci. Forum*, Vols. 353–356, 2001, pp. 299–302.
[63] Stahlbush, R. E., et al., *Mat. Sci. Forum*, Vols. 389–393, 2002, pp. 427–430.
[64] Saddow, S. E., et al., *Sci. Forum*, Vols. 353–356, 2001, pp. 115–118.
[65] Yole Développement, "Evaluation of the 2002–2007 SiC Market and Analysis of the Major Technology and Industrials Trend," market study, 2003.
[66] Frost and Sullivan, *North American Power Semiconductor Markets,* 7273-26, 2000.
[67] Baliga, B. J., *Power Semiconductor Devices*, Boston, MA: PWS Publishing Company, 1996, p. 2, Figure 1.2.

CHAPTER 2

High-Temperature SiC-FET Chemical Gas Sensors

Anita Lloyd Spetz, Shinji Nakagomi, and Susan Savage

2.1 Introduction

Chemical sensors are rapidly growing in importance in society because constraints around environmental issues continue to increase in severity. These constraints include a demand for increasing control of emissions and reduction of energy consumption in vehicles and in industry, which necessitates the development and production of faster and more efficient sensors for on-line control. Gas sensors that can function in extreme environments have the potential to provide this control. Those based on wide bandgap materials such as SiC, AlN, GaN, AlGaN, and diamond have the potential to function in extreme environments such as corrosive atmospheres and at high temperatures. Through the employment of a catalytic material on the device surface, chemical gas sensors based on a variety of field-effect devices have been developed. The capability to operate at elevated temperatures considerably increases the speed of response to a change in the gas atmosphere, providing the potential for the production of very fast sensors. The possibility to measure directly on-line at high temperatures and in corrosive atmospheres, for example, in car exhausts or flue gases, makes it possible to quickly detect unwanted emissions, allowing immediate adjustment of the system for maximum fuel efficiency and emission control.

The wide bandgap of silicon carbide, 3.2 eV for 4H-SiC, permits an operation temperature of up to 1,000°C [1], with time constants for the gas response of a few milliseconds [2]. An electronic device based on SiC can function as a chemical sensor by the deposition of a catalytic material on a thin insulating layer on its surface. For example, the catalytic material can be a metal such as platinum, iridium, palladium, or combinations of these. Metal oxides can also be used as catalytic layers on devices where the material does not need to conduct large currents. The technology lends itself to batch processing, which considerably reduces the price per chip of the sensors. Furthermore, arrays of sensors with different selectivity patterns can be processed on the same chip, which, together with data evaluation algorithms, enable several components to be identified and monitored in the gas mixtures. Several groups have contributed to the development of SiC sensor devices [1–9].

Other wide bandgap materials, such as GaN, AlN, and diamond, with bandgaps of 3.4, 6.3, and 5.5 eV, respectively, have also been explored by a number of

groups [10–15]. These have a higher bandgap than SiC, and therefore have the potential to function at even higher temperatures. Several groups have started to develop chemical gas sensors based on these materials. When film growth and process technology is mature enough, we can expect commercialization of devices based on these materials. The high-temperature operation of devices based on all these materials will encounter similar problems that will have to be addressed. One example, the diffusion of atomic hydrogen in the materials, is described in this chapter.

The high quality of the SiC material available today and the maturity of the processing technology has allowed commercialization of SiC devices to begin. This includes Schottky diodes manufactured by Infineon [16] and UV flame detectors made by General Electric [17]. It has also permitted the demonstration of high-quality prototypes of other devices, such as large-area SiC X-ray detectors based on Schottky diodes, which function at 100°C [18]. Therefore, if commercialization is to be realized in the near future, SiC is the preferred material for developing gas sensors that can function in extreme environments.

We recently published a chapter in the book *Silicon Carbide: Recent Major Advances* by Choyke et al. [19] that describes SiC gas sensor applications in detail. In this book, we emphasize device properties; applications are only briefly reviewed at the end. The device and gas sensing properties of various field-effect chemical gas sensing devices based on SiC are described, and other wide bandgap material devices are reviewed. The detection principle and gas response is explained, and the buried channel SiC-FET device is described in detail. Some special phenomena related to the high-temperature influence of hydrogen at high temperature are also reported.

2.2 Detection Mechanism of Field-Effect Gas Sensors

It is important to have a clear picture of the detection mechanism before we introduce the different types of field-effect transistor (FET) devices and their gas sensing properties. The sensing mechanism is largely independent of the device type, since the chemical reactions responsible for the gas response are defined by the type of catalytic material processed onto the device and the operation temperature [1, 2, 20, 21]. Even at a temperature of 600°C, chemical reactions occur on the catalytic metal surface at a rate of a few milliseconds, which is slower than the response time of the devices.

2.2.1 Gas Sensing Principle

The detection principle of field-effect sensors with catalytic metal contacts is based on the change of the electric charge at the insulator surface caused by dissociation of the gas molecules by the catalytic material. Adsorbed gas molecules and reaction products form a polarized layer at the metal-insulator interface (Figure 2.1). This gives rise to an electric field in the insulator, which causes the concentration of mobile carriers in the semiconductor underneath the insulator to change.

The gas response, ΔV, is a Langmuir response, which saturates at higher gas pressures, P [22]:

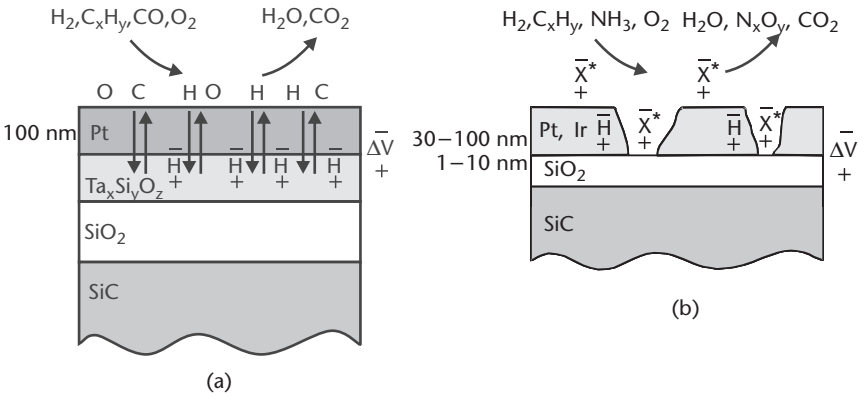


Figure 2.1 (a) Schematic picture of an MISiC device with a dense catalytic metal gate. (b) A porous catalytic metal gate. The total gas response is a combination of responses at the metal-insulator interface, metal in contact with the insulator, and exposed insulator surface.

$$\Delta V = \Delta V_{\max} P^{\beta} / \left(1 + P^{\beta}\right) \tag{2.1}$$

where $V_{\max}$ is normally 0.5-1 V and β depends on the reaction path. The polarization introduced by the gases at the insulator interface will change the current voltage (IV) characteristics of a Schottky diode, or a diode-coupled transistor, and will change the flat band voltage of a capacitor (Figure 2.2). A time-resolved gas response can therefore be measured as the voltage shift at a constant current or constant capacitance level (Figure 2.3).

Because chemical reactions on the catalytic metal surface are responsible for the detection of gases, the sensor response is highly temperature-dependent. In general, an increased temperature gives a faster gas response (see Section 2.5.1 and [2]). Thus, both the catalytic metal type and the temperature influence the gas response [23, 24].

2.2.2 Detection of Different Molecules

2.2.2.1 Detection of Hydrogen

In the case of thick, dense catalytic metals, hydrogen or hydrogen-containing molecules such as hydrocarbons dissociate on the surface of the metal, and the resulting hydrogen atoms diffuse through the metal within microseconds to the insulator surface [see Figure 2.1(a)]. This occurs at temperatures as low as 150°C, depending on the molecule and increases with temperature. Experimental results indicate that the polarized layer is indeed located on the insulator surface [22, 25], and this is further supported by results from ion-selective field-effect sensors (ISFETs), where it is shown that hydrogen introduces SiO^-, SiOH, and $SiOH_2^+$ groups on the SiO_2 surface in a liquid environment [26]. The maximum shift, $\Delta V_{\max}$, given by the polarized layer may be described as:

$$\Delta V_{\max} = pN/\varepsilon_0 \tag{2.2}$$

where p is the dipole moment of the charged complex, N is the number of sites for the complex, and ε_0 is the dielectric constant. Results from devices with different

insulator materials (Al_2O_3, Si_3N_4, Ta_2O_5, and SiO_2) show a strong correlation between the oxygen concentration on the insulator surface and the "inert hydrogen response." This indicates that absorption at the metal-insulator interface is indeed at these surface oxygen atom sites [27]. A similar model has also been suggested for the hydrogen response of thick Pt films in Pt/GaN Schottky diodes [14]. This is supported by results from elastic-recoil detection (ERD) experiments, which lead to a model where the hydrogen-induced polarized layer is formed at an oxidic interfacial layer [11]. It has also been shown that GaN Schottky diodes produce a similar gas response to their SiC counterparts, and this is irrespective of whether the Schottky contact is formed on the Ga or N surface. This indicates that the interface properties that are responsible for the gas response are similar for SiC and GaN and on both faces of the GaN [28, 29]. Another strong support for the model in which charges on the insulator surface are responsible for the gas response is provided from experiments with AlGaN/GaN HEMT that do not include metal on the gate region. These devices have also shown similar modulation of the channel current for Ga or N face surfaces due to fluxes of negative or positive ions generated by an ion spray technique [28]. The channel current was amplified by as much as 1,000.

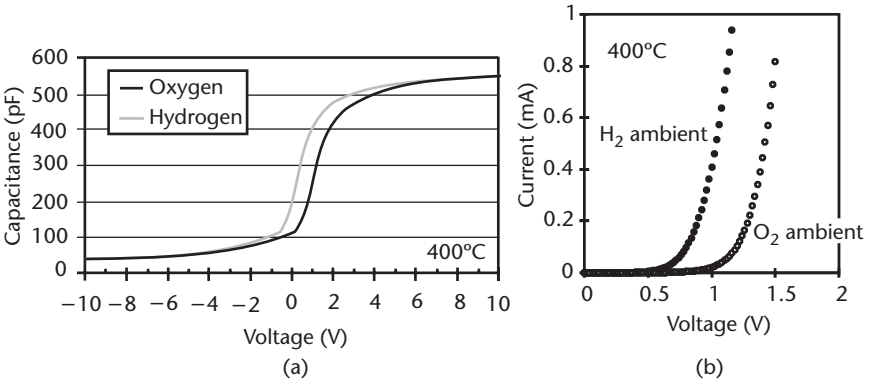


Figure 2.2 (a) Capacitance voltage characteristics of an n-type SiC-based capacitor at 400°C with a gate of sputtered Pt. (b) Current voltage characteristics of a Schottky diode at 400°C with a porous Pt gate electrode.

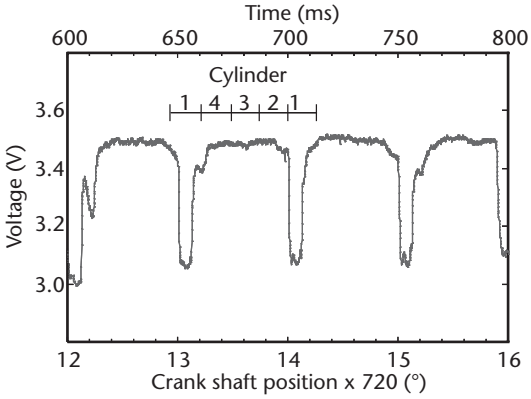


Figure 2.3 The sensor signal (the voltage at a constant current) in a cylinder-specific measurement, when one cylinder is driven under excess fuel (rich) conditions. When cylinder 1 ignites, the sensor signal changes to a lower voltage.

2.2.2.2 Detection of Ammonia

The detection of other molecules, such as ammonia, requires the use of a porous catalytic metal. To obtain a gas response from the NH_3 molecule, it is believed that active sites of "triple points" are required where the molecules are in contact with the metal, insulator, and ambient [30, 31]. It has been shown that gas species such as hydrogen atoms or protons also diffuse out onto the exposed oxide surface in between the metal grains [Figure 2.1(b)] [32, 33]. Furthermore, Löfdahl et al. have performed experiments that provide clear evidence that hydrogen atoms or protons also diffuse under the metal from the triple point [34]. The hollow structure of the metal surface facing the insulator has been revealed by Åbom et al. [35].

The detection mechanism can now be summarized in the following [36]:

$$\Delta V = \gamma_i \Delta V_i + \gamma_m \Delta V_m + \gamma_s \Delta V_s \tag{2.3}$$

Thus the total gas response is a combination of the response at the metal-insulator interface (*i*), metal in contact with the insulator (*m*), and exposed insulator surface (*s*) [Figure 2.1(b)]. The constant γ is a function of several parameters, for example metal coverage and temperature.

2.2.2.3 Detection of Hydrocarbons

The field-effect devices with catalytic metal contacts respond to hydrogen as well as other hydrogen-containing molecules such as hydrocarbons through the delivery of hydrogen atoms or ions to the metal-oxide interface when the molecules are dissociated on the metal surface [37, 38]. However, oxygen molecules also dissociate on the catalytic metal surface (Figure 2.1) and react with the dissociation products from the hydrocarbons to produce water and carbon dioxide, which leave the surface. This process consumes hydrogen and thus decreases the sensor signal, providing the opportunity to indirectly detect the presence of oxygen.

2.2.2.4 Detection of Carbon Monoxide

The response to hydrocarbons can be explained by the dissociated hydrogen atoms forming a polarized layer at the insulator surface. However, an observed response to carbon monoxide cannot be explained so readily. A careful investigation has been carried out into the response to CO at 600°C by Nakagomi et al. [20]. It was observed that the response to hydrogen and CO showed an additive effect. It was also observed that the gas response to both CO and H_2 was considerably lowered by the presence of water vapor in the atmosphere. Nakagomi suggests three possibilities for the CO response.

1. The response to CO in argon may actually be a response to background hydrogen, since the sensor is observed to become extremely sensitive to hydrogen once the CO has consumed all the oxygen atoms on the sensor surface [39].
2. In argon, the CO molecules may simply reduce the oxide layer on the Pt surface, which gives rise to an increased response due to the difference in

work function between the clean Pt surface and that with adsorbed oxygen [20, 40]. (It has been shown that the Pt surface can be reversibly oxidized at these temperatures [41].)

3. In an oxygen atmosphere CO sometimes gives a direct gas response for a porous metal film. This indicates that the CO molecule may be detected when adsorbed at a site where the dipole moment of CO is able to influence the mobile carriers in the semiconductor.

Samman et al. have characterized propane, propylene, and CO response up to 640°C in laser-ablated Pt MOSiC capacitor devices [5]. They deduced that the strong response they found to CO at temperatures greater than 490°C is actually caused by a response to oxygen, for example in the form of charged oxygen vacancies within the oxide. They also suggested that contamination by Na and K in the oxide can play a role, which has previously been suggested by Nylander et al. in 1984 [42]. High concentrations of Na or K ions in the oxide may form complexes with gas-introduced species in the oxide. Schalwig et al. also point out that the removal of oxygen by CO might be detected as a shift in the same direction as that caused by the addition of hydrogen [5, 40].

The details in the CO response continue to be the subject of many discussions and a full explanation will need further studies. These can include spectroscopy studies such as diffuse reflectance transform infrared spectroscopy (DRIFT), which can be performed under realistic conditions [43, 44], and theoretical modeling [45]. However it seems likely that not only hydrogen gives rise to charged or polarized complexes on the insulator surface. Equation (2.3) may now be written as

$$\Delta V_{\max} = \sum_{i=1}^{n} p_i N_i / \varepsilon_0 \tag{2.4}$$

where p_i is the dipole moment for the complex i and N_i is the number of sites for the complex i. The same site (e.g., oxygen atoms on the insulator surface) may be occupied by different complexes. From available activation energies and adsorption and desorption energies, it may be possible to calculate the equilibrium distribution of different complexes at a certain temperature.

2.2.3 Influence of Oxygen

It has been suggested by several groups that oxygen may be involved in the detection mechanism [20, 40, 46]. For example, the removal of adsorbed negative oxygen ions will give the same electrical effect as adsorption of positive hydrogen ions, protons. There is also evidence of a direct response to oxygen, which is larger from an Ir gate sensor, compared with a Pt gate sensor.

Nakagomi et al. have shown that the hydrogen response in an atmosphere containing excess oxygen has a square- and quarter-root dependence, respectively, on the hydrogen and oxygen pressure at 300°C, compared with the square-root dependence for both the hydrogen and oxygen pressure at 150°C [3]. The correlation between the coverage of active sites for the gas response Θ and the hydrogen and oxygen pressure can be described by [3, 47]:

$$\frac{\Theta}{1-\Theta} = k\frac{\sqrt{P_{H_2}}}{\sqrt[4]{p_{O_2}}} \tag{2.5}$$

For an Si-based Pd MOS device, it has experimentally been shown by Hua et al. [48] that the quarter-root dependence in (2.5) was valid at 50°C, and Hughes et al. [49] showed the same behavior at 30°C, whereas at 75°C the square-root dependence applies. This indicates that different chemical reactions are rate-limiting at different temperatures. The quarter-root dependence has been interpreted by Lundström [47] as the formation of water from a reaction between hydroxyl (OH^-) groups on the surface, whereas adsorbed hydrogen atoms form water with OH^- groups very slowly. The adsorbed oxygen atoms block only the dissociation of hydrogen.

2.2.4 Influence of Different Metals

The response to hydrogen is considerably lower for Pt, compared with Pd, and this has been explained as a difference in the reaction barrier for OH^- formation (between adsorbed atomic hydrogen and oxygen). This barrier is higher on Pd than on Pt, which leads to a higher surface coverage on Pd and therefore a higher hydrogen response at a given gas concentration [50].

Kim et al. have compared the hydrogen and methane sensitivity at 400–600°C of Pt and Pd-SiC Schottky diodes fabricated on n-type 6H-SiC. The Pd or Pt (<80 nm) was sputter deposited in 1-mm dots [8]. The sensitivity was measured as the change in current at a constant forward bias of 3V. The Pd-SiC Schottky diodes showed a higher sensitivity, as well as faster speed of response to both hydrogen and methane. The stability of the hydrogen response was tested for 30 days at 500°C and showed excellent results for both types of sensors.

In Figure 2.4 the response to NH_3 versus temperature shows characteristic differences for the two different catalytic metals, Ir and Pt [51, 52]. The NH_3 response is larger over a wider temperature range for Ir compared with Pt. Also, the increase in temperature at which maximum sensitivity occurs as a function of NH_3 concentration is more pronounced for Ir than for Pt. The difference in catalytic activity between Pt and Ir has been confirmed previously [53, 54]. Literature reports differences in the oxygen adsorption on these two metals, which may be one reason for the differences seen here [55, 56].

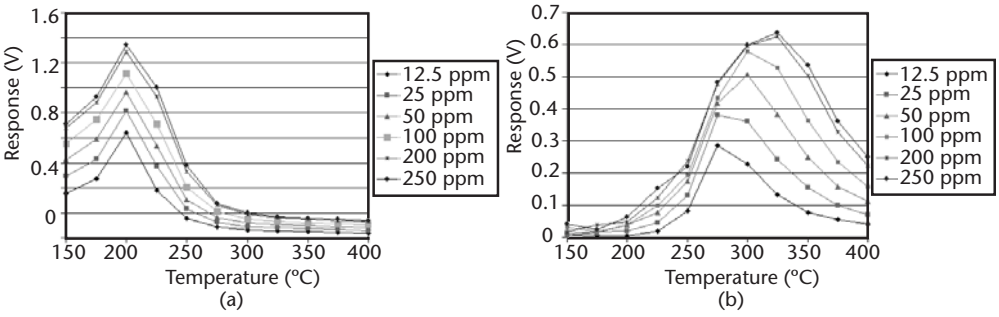


Figure 2.4 The ammonia response versus temperature for an MISiC-FET sensor with (a) 25-nm Pt and (b) 60-nm Ir as the gate contact metal. NH_3 concentration: 12.5, 25, 50, 100, 200, and 250 ppm in 10% O_2/N_2. (*From:* [23]. © 2003 IEEE. Reprinted with permission.)

2.2.5 Influence of Temperature

The metal-insulator-silicon carbide MISiC sensors function over a large temperature range, 100–700°C. Their gas response can be divided into two different temperature regimes with the break-over point around 600°C.

Above 600°C the gas response of MISiC sensors, for example, to hydrocarbons, shows a binary behavior. This means that the signal has basically only two voltage levels and changes rapidly from a low level in excess hydrocarbons to a high level in excess oxygen (Figure 2.5).

Due to the large reaction rates that occur at temperatures around and above 600°C, exposure to hydrogen or hydrocarbon gas mixtures causes the platinum surface to go rapidly through a transition from a surface covered with adsorbed oxygen atoms to a surface covered with adsorbed hydrogen and hydrocarbon species [57]. In excess oxygen, total combustion of the hydrocarbon molecules on the metal surface probably occurs, causing the hydrocarbons to convert to water, nitrogen, and carbon dioxide, which leave the surface. For the sensor devices this means that the gas response quickly changes from the base line level in oxygen to the saturated hydrogen response level. A model for this binary response has been suggested by Baranzahi et al., based on kinetic phase transitions [58]. This explains that the signal depends on the total ratio, α defined in (2.6), of oxidizing and reducing species, but is largely independent of the gas composition.

$$\alpha = \sum_{i=1}^{n} \frac{\left(2x + \frac{y}{2}\right)\left[C_x H_y\right]_i}{2\left[O_2\right]} \tag{2.6}$$

In the temperature regime below 600°C, a more linear response is obtained. This is demonstrated in the response to hydrogen at 300°C compared with that at $T > 600$°C in Figure 2.5(b). In the lower temperature regime it is postulated that only partial combustion of the gas molecules occurs on the metal surface. This also means that at these lower temperatures, the various hydrocarbons are dissociated to different degrees and give substantially different responses at critical temperatures.

The reactivity of other gas molecules such as ammonia and CO also shows a strong temperature dependence [24]. The response to ammonia as a function of temperature is shown in Figure 2.4 for the case of two different catalytic metals, as previously described. It is seen that the temperature profile of the response is also dependent on the type of catalytic metal and the concentration of NH_3. This provides the opportunity to tailor-make the sensor to fit the application by choosing appropriate catalytic metals and measurement temperatures.

2.2.6 Sensor Arrays

The fact that the sensing of different gases can be controlled by the correct choice of catalytic metal and operating temperature opens the possibility to use arrays of these sensors together with pattern recognition techniques to provide detailed information about the composition of ambient gases. This has been tested in flue

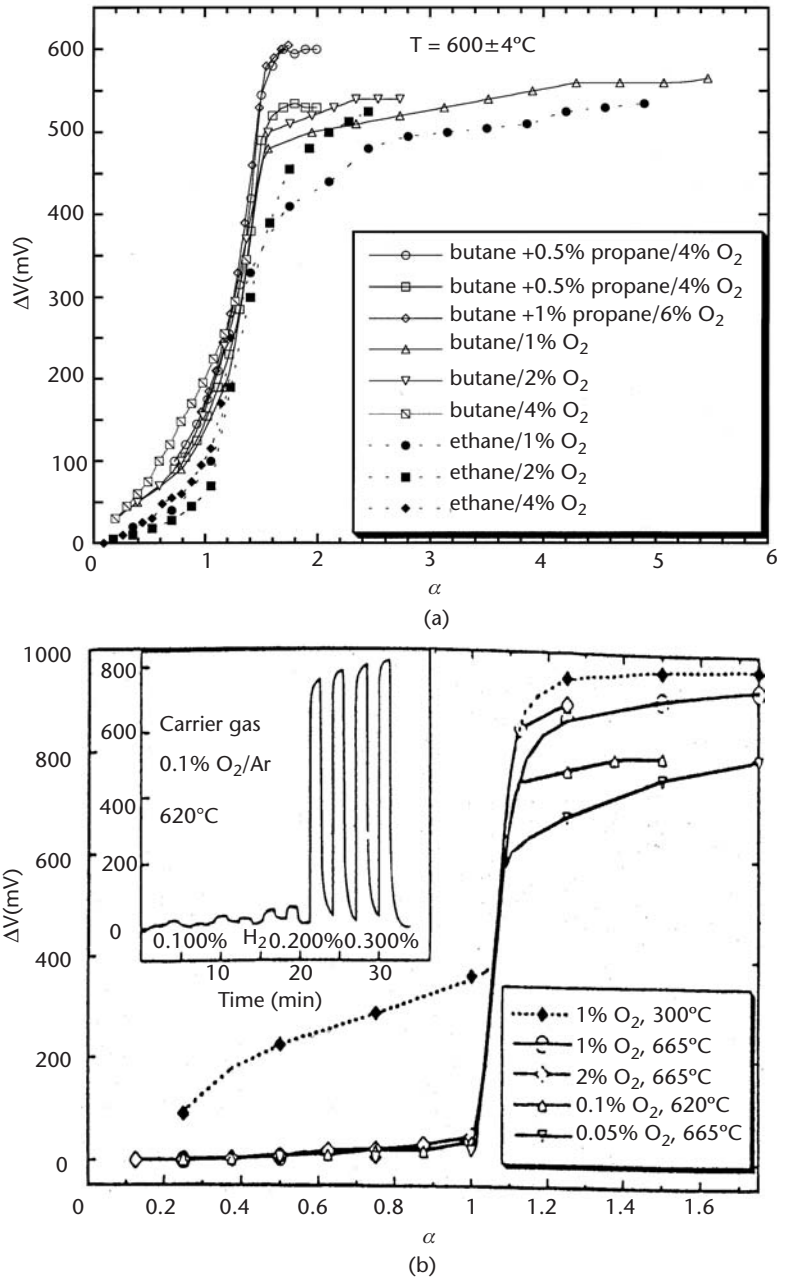


Figure 2.5 The response of an MISiC sensor. (a) At 600°C to gas mixtures containing different hydrocarbons (butane, propene, ethane) and concentrations. (*From:* [56]. © 1997 Elsevier B.V. Reprinted with permission.) (b) To hydrogen in different oxygen concentrations at 300°C and at $T >$ 600°C plotted versus the ratio of reducing to oxidizing species, α, as defined in (2.6). Inset: the pulse response at 620°C to 0.1, 0.2, and 0.3% H_2 in 0.1% O_2/Ar. (*From:* [57]. © 1988 The Electrochemical Society. Reprinted with permission.)

gases by Unéus et al. and is described in Section 2.7.3 [59]. Hunter et al. have also suggested the use of arrays of their SiC-based Schottky diodes at different temperatures to enhance the versatility of their sensors [60].

2.3 Field-Effect Chemical Gas Sensor Devices

The hydrogen sensitivity of palladium-oxide-semiconductor (Pd-MOS) structures was first reported by Lundström et al. in 1975 [61]. A variety of devices can be used as field-effect chemical sensor devices (Figure 2.6) and these are introduced in this section. The simplest electronic devices are capacitors and Schottky diodes. SiC chemical gas sensors based on these devices have been under development for several years. Capacitor devices with a platinum catalytic layer were presented in 1992 [62], and Schottky diodes with palladium gates the same year [63]. In 1999 gas sensors based on FET devices were presented [64, 65]. There are also a few publications where p-n junctions have been tested as gas sensor devices [66, 67].

Since the capacitor, Schottky diode, and transistor all contain an insulating layer under the catalytic metal, they are all referred to in this chapter as field-effect devices. In published literature, the capacitor and diode SiC devices are often referred to as MISiC devices, and the transistor as an MISiC-FET device.

2.3.1 Capacitors

The simplest device is the capacitor, which consists of an insulator on top of a low-doped semiconductor with a metal contact on the top surface (Figure 2.6). To use this device as a sensor, a catalytic metal such as Pt or Ir is used as the contact metal. A capacitor is the simplest device to produce and therefore especially suited for measurements in the lab. Rather complicated equipment is required for making sensor measurements, especially since the sensor response preferably should be measured as the change in voltage at a constant capacitance [68]. An ac voltage with a frequency of 1 MHz and maximum amplitude of about 100 mV is normally used for the capacitive measurements, and a dc bias normally between –10V to 10V is then swept to get a *C-V* curve. Even though this is a rather small voltage, the electric field produced in the insulator of the capacitor produces sufficient stress at high temperatures to eventually cause breakdown of the insulator. A high-quality insulator stack based on SiO_2/Si_3N_4 and densification of the nitride, which forms a thin layer of SiO_x (~5 nm), improves the capacitance-voltage (CV) measurements to some extent. A typical *C-V* measurement at 400°C is shown in Figure 2.2(a). For long-term stability, capacitor devices should still preferably be operated at ≤ 500°C. In Section 2.4.1, *C-V* curves from operation at 500°C and 700°C are demonstrated.

SiC capacitor sensors have demonstrated gas-sensitivity to gases such as hydrogen and hydrocarbons [21, 46, 68] up to a maximum temperature of 1,000°C [1, 68]. Devices that can be operated both as MOS capacitors (reverse bias) and as Schottky diodes at temperatures greater than 490°C have also been demonstrated (see Section 2.4.2) [10]. These devices showed sensitivity to combustible gases such as propane, propylene, and CO and were tested at temperatures up to 640°C.

2.3.2 Schottky Diodes

The development of SiC Schottky diode sensors was of interest due to their simple associated electronic circuitry. A Schottky diode usually consists of a metal contact on top of a low-doped semiconductor (Figure 2.6). These devices were pioneered by

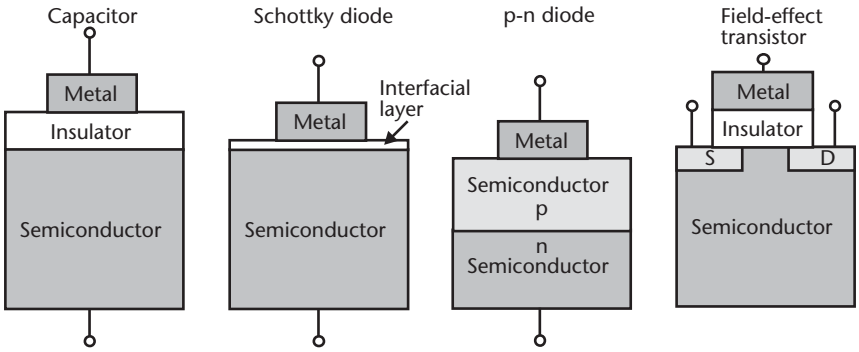


Figure 2.6 Schematic diagrams of the different field-effect devices described in this chapter. (*From:* [19]. © 2003 Springer-Verlag. Reprinted with permission.)

Hunter [63] et al., and several research groups have contributed to the development. For a review, see [69]. In the same way as the *C-V* curves [Figure 2.2(a)], the *I-V* characteristics shift along the voltage axis when there is a change in the gas ambient, for example, between excess hydrogen and excess oxygen [Figure 2.2(b)]. We believe that the gas ambient has a similar influence on both devices, as further described later in this section.

2.3.2.1 Interfacial Layers

The first Schottky diode sensors were produced by processing the catalytic contact metal directly onto the semiconductor surface using hydrofluoric acid (HF) to remove the native oxide. These devices showed poor stability and reproducibility. This could be attributed to the presence of surface states, caused by dangling bonds, for example, which are known to introduce pinning of the Fermi level. In the worst case, changes in the metal work function caused by the ambient gas would not cause a change in the barrier height, thus preventing a gas response [70].

It was demonstrated that reproducible gas-sensitive silicon Schottky sensors could be produced after terminating the silicon surface with an oxide layer [71, 72]. This interfacial oxide layer permits the device to function as a sensor, but also as a diode, as the charge carriers can tunnel through the insulating layer. The layer made the Schottky diode behave like a tunneling diode, and the ideality factor could be voltage-dependent [73].

An ozone treatment (10 minutes at room temperature) of the HF-etched SiC surface before the metallization step was introduced as a very convenient processing step to produce Schottky diode gas sensors with an increased stability and reproducibility. The use of spectroscopic ellipsometry analysis and also photoelectron spectroscopy using synchrotron radiation showed that an oxide, 1-nm in thickness, was formed by the ozone exposure [74, 75]. The oxide was also found to be close to stochiometric SiO_2 in composition. This thin oxide increased the stability of the SiC Schottky diodes considerably, without the need for any further interfacial layer such as Ta or $TaSi_x$, which have been frequently used. Schottky diodes employing a porous Pt gate electrode and the ozone-produced interfacial layer have been successfully operated in both diesel exhausts and flue gases [76, 77].

Weidemann et al. found that wet etching of a GaN surface before Pd deposition also produced an interfacial oxide, which increased the hydrogen sensitivity by approximately a factor of 50 [14]. They concluded that comparing device parameters between different GaN Schottky diode gas sensors requires a defined standard treatment of the GaN surface to introduce a controlled interfacial oxide.

Tobias et al. investigated Pt-gate 6H-SiC Schottky diodes with an interfacial layer of 1-nm Ta or 10-nm $TaSi_x$ [78]. Both n-type and p-type diodes showed a gas response to hydrogen at 400–600°C. It was postulated that the gas response to hydrogen observed in the forward direction is mainly due to a change in the resistance of the gate contact.

Nakagomi et al. have studied the stability of a Pt-thin oxide-SiC diode by repeatedly heating and cooling the device [79]. The stability of the *I-V* and *C-V* characteristics of the diode were good during exposure to an ambient of H_2 (20%) or O_2 (20%) at a temperature lower than 300°C. However, annealing for 6 hours at 600°C in air reduced the absolute value of the current, the capacitance, and the *I-V* gas sensitivity, and caused these to become unstable after this high-temperature annealing.

Hunter et al. demonstrated palladium-gate SiC Schottky sensors, but a drift was experienced when the sensors were operated at 350°C for a period of several weeks [4]. It was suggested that this was caused by a reaction between Pd and SiC. Hunter et al. tested two different approaches to remove this drift. First an alloy of Pd/Cr was tested, which caused the sensitivity to hydrogen to increase by two orders of magnitude. Second, SnO_2 was tested as an interfacial layer under the Pd contact, which resulted an increased sensitivity to hydrogen, methane, and propylene. The long-term stability was substantially improved in both cases.

Another problem with Schottky diodes is that at high temperatures, the metal contact can anneal to the semiconductor, forming a silicide in the case of silicon and SiC [72, 80–83]. This can destroy the diode characteristic of the device, thus producing an unstable sensor. Use of an interfacial insulating layer, such as the oxide layer already mentioned, can prevent this from occurring.

Chen et al. have investigated the effect of a high-temperature anneal on Pd/SiC and Pd/SiO_2/SiC Schottky diodes [84]. After annealing at 425°C for 140 hours, the Pd/SiC device lost some of its sensitivity to hydrogen. Pd_xSi was formed with a small quantity of SiO_x on the surface of the Pd/SiC diode. The Pd/SiO_2/SiC lost almost all hydrogen sensitivity after the same anneal. The surface of the device contained a large quantity of SiO_x and the interface had changed to a stable composition of Pd and Pd_4Si.

2.3.2.2 Introduction of a Resistance Term

Nakagomi suggested a relationship, involving a barrier height change in series with a resistance change, for the hydrogen response of Schottky sensors based on Pt-TiO_x-SiC devices, whereas the hydrogen response of Pt/SiC diodes could be modeled by considering only changes in the barrier height [73]. The response of the latter device was found to be constant, whereas the response of the former device was dependent on the current level and increased with increasing current level. The varying gas response was attributed to a change in the resistance of the device [73].

$$I = SA^{*}T^{2}\ \exp\left[-q\phi_{Bn} / kT\right] \cdot \left(\exp\left[q(V - IR_{s}) / nkT\right] - 1\right) \tag{2.7}$$

Now the response may be written:

$$\Delta V = n\Delta\phi_{Bn} + I\Delta R_{s} \tag{2.8}$$

The dependence of the response (voltage difference in hydrogen and oxygen) was measured as a function of forward current for devices with 10- or 50-nm TiO_x and compared with devices without the TiO_x layer and at higher temperatures. The current dependence of the response increases for the thicker TiO_x layer and higher temperature (Figure 2.7). This phenomenon was confirmed by Nakagomi et al. for a device with tungsten trioxide as the interfacial layer, a Pt-WO_3-SiC structure [85].

Also Tobias et al. reported, as already described, resistivity changes to be the main reason for the hydrogen response observed in the forward direction of the *I-V* characteristic of Schottky diodes with a Pt gate and an interfacial layer of $TaSi_x$ [78].

AlN exhibits both a high band gap (6.3 eV) and also a high dielectric constant. Therefore it is capable of replacing either the semiconducting material or the insulator in SiC-based sensors. AlN has the potential to form an excellent insulating layer on SiC, as the crystalline materials are latticed-matched. Crystalline AlN can be formed on SiC by epitaxial growth [5, 10]. Sarina et al. have demonstrated the use of Pt-AlN-SiC as a highly selective hydrogen sensor, by the epitaxial growth of AlN by plasma source molecular beam epitaxy (PSMBE) [10]. Samman et al. have

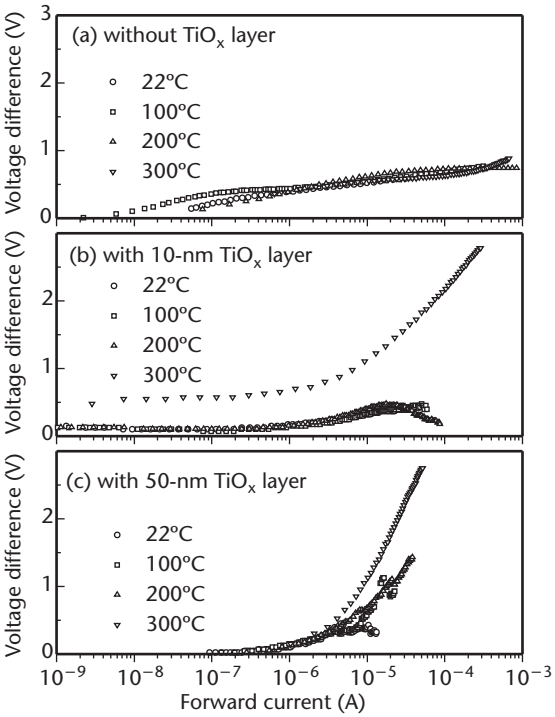


Figure 2.7 The dependence of the response to hydrogen (the voltage difference between 20% H_2/N_2 and 20% O_2/N_2) on the forward current level of three devices: (a) without the TiO_x layer, (b) with 10-nm TiO_x, and (c) with a 50-nm TiO_x layer. (*From:* [73]. © 2001 The Electrochemical Society of Japan. Reprinted with permission.)

processed Pt-AlN-SiC devices, where both Pt and AlN are deposited by a laser ablation technique (see Section 2.6.2). The latter devices could be used as both a MOS capacitor (in reverse bias) and as a Schottky diode (in forward bias) [5]. In the capacitive mode the maximum response was caused by hydrogen, whereas in the forward-bias mode at 5 μA, propane, propylene, and carbon monoxide (CO) produced the largest responses. The device could be operated in the Schottky diode mode in the temperature range of 250–650°C. These results led to the conclusion that the normal diode equation for thermionic emissions had to be adjusted by a resistance term (see (2.7)]. Hydrogen introduces a polarized layer on top of AlN for a Pt electrode device, whereas hydrocarbon (HC) and CO does not. However, HC and CO change the resistance in the AlN layer.

2.3.2.3 Introduction of the Nernst Potential

The function of ionic conducting materials is well known to be based on the bulk diffusion of oxygen, for example, zirconium dioxide [86]. Also proton conductors exist, as reported by Visser et al. [87]. The most common way to employ these materials as gas sensors is as electrochemical cells. A dehydrogenation catalyst is placed on one side of the proton-conducting material with two electrodes placed on opposite sides of the material. For the case of zirconia, when the oxygen concentration is different on either side of the material, oxygen ions supplied to the zirconia from dissociation on the Pt electrodes will build up a gradient through the material, and so a potential will be measured. These ion-conducting materials may also be employed in SiC field-effect devices, enabling device use without the need for a reference electrode and reference air. This was also achieved in SiC-based capacitor devices through the introduction of a metal oxide on top of the SiO_2, for example ZrO_2 [88], LaF_3 [7], CeO_2 [89], and $BaSnO_3$ [90].

Jacobsen et al. have demonstrated a Schottky diode with a mixed ion conductor, Pt/CeO_2/SiC, which showed very high sensitivity to hydrogen at 500°C after annealing at 700°C [89]. It was proposed that the annealing introduced oxygen vacancies in the CeO_2 layer, which were suitable for interaction with protons, thus causing resistance changes in the layer.

A mixed ion conductor, $BaSnO_3$, has also been tested as a contact layer on a Schottky sensor [90]. The $BaSnO_3$/SiC sensor showed a response to oxygen and this was most pronounced at 400°C. The sensor was tested from 200°C to 700°C. Operated at 700°C, the sensor showed a negative resistance peak at a bias of 2V (Figure 2.8). This peak was accounted for by the tunneling or Esaki effect [91]. Up to an operation temperature of 400°C, thermionic emission was proposed to explain its behavior. At higher temperatures, a resistance connected in series with a Schottky diode can model the device [5, 73]. At temperatures of 500–600°C, the $BaSnO_3$ shows a mixed behavior of electronic and ion conduction, and the Nernst potential [92] can be added to the model. The complete proposed model is given in (2.9).

$$I = SA^{*}T^{2}\ \exp\left[-q\phi_{Bn}\ /\ kT\right]\cdot\left(\exp\left[q\left(V - IR_{s} - V_{NERNST}\right)/nkT\right] - 1\right) \tag{2.9}$$

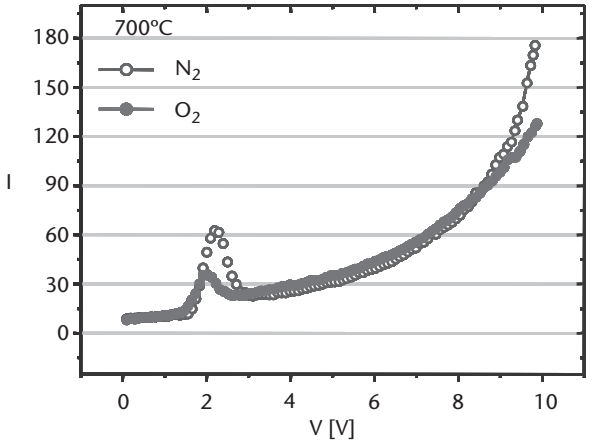


Figure 2.8 *I-V* curves at 700°C in different gas atmospheres, N_2 and 21% O_2/N_2.

The first part of the equation relates to the well-known thermionic emission equation [93]. At low temperatures (up to 400°C), the term IR_s is more significant than V_{NERNST}, and vice versa at high temperatures (above 400°C). Thus, the $BaSnO_3$/SiC device also has the potential to be used as an oxygen sensor without the need for a reference electrode and reference air.

2.3.2.4 Other Wide Bandgap Materials

Schottky diode sensors based on other wide bandgap materials have also been investigated, as previously mentioned. GaN Schottky diodes processed on either the Ga or N face have been examined by Schalwig et al. [11, 21]. A Pt/GaN Schottky diode with a barrier height of 1-eV has been shown to reversibly transform into an ohmic contact through exposure to H_2 [94]. Kokobun et al. have also investigated Pt-GaN Schottky diodes as hydrogen sensors up to 600°C [15].

Pt/SnOx/diamond diode gas sensors have been investigated by Gurbuz et al. [12]. This sensor responded in seconds to small concentrations of O_2, CO, and H_2 at operation temperatures up to 450°C.

Zhu et al. [95] demonstrated the use of Pd/amorphous $Ba_{0.67}Sr_{0.33}Ti_{1.02}O_3$/Pt as a sensor. The *I-V* characteristic of this device showed a very large shift when exposed to hydrogen. This was about 5V for a switch between an oxygen-rich and a hydrogen-rich atmosphere.

2.3.3 The P-N Junction Diode

The p-n junction diodes employing catalytic metal contacts have recently been tested for their gas-sensing properties [66, 67]. The catalytic metal contact was placed directly on the semiconductor in this device, as shown in Figure 2.6. In general the response appears to be lower than for the traditionally used devices described earlier in this section. However, this means that for any catalytic metal used as an ohmic contact to a p-n junction, it can be expected that the *I-V* characteristics will be influenced, for example, in a hydrogen-containing atmosphere.

Nakshima et al. have fabricated p-n junction devices by employing Al implantation to yield a p-doped layer in n-type 6H-SiC [66]. A Pt layer on top of the p-type ohmic contact (PtSi) provided both protection and a catalytic metal contact to create a chemical gas sensor device. A response (30 and 60 mV, respectively) was obtained to both 50 ppm and 100 ppm of ammonia in nitrogen at 500°C.

Another p-n junction-based hydrogen sensor has been produced by implanting palladium ions into 6H n-type SiC material [67]. Gold-plated copper contacted the p-n junction device. The gas response was measured as (small) changes in current as the gas ambient was varied between air and 4% H_2 in argon in the temperature range 23–240°C. For an absolute voltage above 1.2V, the p-n junction broke down.

2.3.4 Field-Effect Transistors

Both capacitor and Schottky sensors have disadvantages. Capacitors require complex surrounding circuitry to measure the gas response. Schottky sensors require an extremely thin insulating layer under the catalytic metal through which current must constantly flow, which can degrade at high temperatures and during long-term operation. The use of a thick interfacial layer in a Schottky sensor has been shown in the previous section to lead to low repeatability due to a current dependent gas response [73]. The best characteristics of these two devices can be combined in a MOS transistor device, where simple circuitry can be combined with the use of a thick gate insulator through which no current flows. The FET is the most complicated device design tested to date but is maybe the most stable and reliable gas sensor. In this device, an ordinary ohmic metal contact is made to the n-type source and drain regions, and the catalytic metal is used as the gate contact placed on top of an insulating layer over the channel region (Figure 2.6). In traditional FETs, small voltages applied to the gate contact can control large currents that pass through the channel region between the source and drain regions. In the case of the sensor, the small changes induced in the catalytic metal by the reactant gases can cause large changes in the source-drain current, which makes this device a very sensitive sensor.

The transistor we describe here has been developed as a chemical gas sensor in a cooperative effort between Swedish Sensor Center (S-SENCE) and the development company ACREO AB [64, 65, 96]. The sensor is based on a catalytic MISiC-FET, with buried source, drain, and channel regions to improve high-temperature performance [64]. The MISiC-FET functions as a gas sensor by the application of catalytic gate materials, such as Pt or Ir, on the device surface over the channel region. The device design is shown in Figure 2.9. The source and gate of this device are connected together to create a convenient two-terminal device. A voltage applied between the source and drain contacts causes a current to flow between these contacts through the buried channel region (Figure 2.9). The buried source, drain, and channel region move the conducting path in the device away from the surface of the SiC, thus reducing the influence of surface and environmental effects.

This device has shown stable gas sensitivity to hydrogen, ammonia, hydrocarbons, and CO up to temperatures of 500°C. Detection of hydrocarbons up to a temperature of 775°C has been demonstrated [65], but a slow drift was detected in the response at temperatures above 600°C.

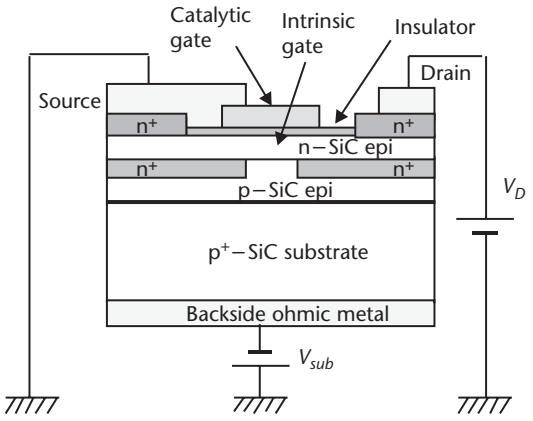


Figure 2.9 A schematic drawing of the design of the MISiC-FET sensor. Gate and source contacts are connected together. The design allows the application of a voltage on the substrate, as indicated in the drawing. The location of the intrinsic gate is indicated in the drawing. (*From:* [98]. © 2003 IEEE. Reprinted with permission.)

2.3.4.1 Negative Substrate Bias

It is possible to influence both the position of the base line and the size of the gas response by the application of a negative potential on the substrate [97, 98]. The drain current-voltage (I_d-V_D) characteristics of a chemical gas sensor based on an MiSiC-FET with a $TaSi_x$ (10 nm) + Pt (100 nm) gate (Figure 2.10) was measured in H_2 and O_2 ambient while applying negative substrate biases at temperatures up to 600°C. This device is effectively a junction field-effect transistor (JFET) structure with a buried short channel and reveals nonsaturation (triode-like) characteristics [99], as shown in Figure 2.11. In addition to the increased drain current as normally observed in H_2 ambient, compared with O_2 ambient, an increased negative voltage on the substrate gives rise to an increased drain voltage V_D at a given drain current. This provides the possibility to adjust the base line of the device. Furthermore, we

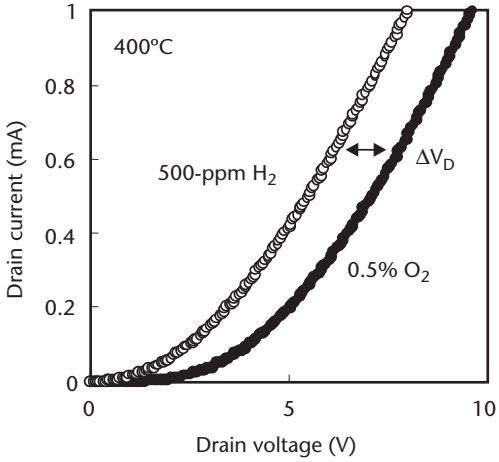


Figure 2.10 Drain current and voltage (I_d-V_D) characteristics of the MISiC-FET in 500-ppm H_2/N_2 or 0.5% O_2/N_2 at 400°C. The drain-voltage shift caused by a change in ambient at a given drain current is defined as V_D.

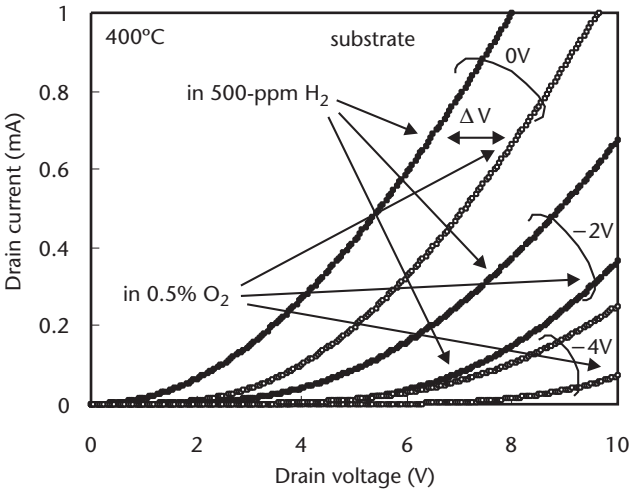


Figure 2.11 The influence of substrate bias on the drain current-voltage characteristics in 500-ppm H_2 or 0.5% O_2 at 400°C. (*From:* [97]. © 2004 Material Science Forum. Reprinted with permission.)

found that the drain voltage shift between H_2 and O_2 ambient at a given drain current increases for an increasing negative substrate bias. This is due to a dependence of the amplification factor on the substrate bias, which will be described later.

The applied negative substrate bias depletes part of the n^--doped epilayer on top of the buried channel from mobile carriers. The conducting channel of the JFET device will then in fact extend also into this depleted epilayer. Then we can define the "intrinsic gate" of the device as the area in the epilayer, on top of the conducting channel, where the electrons have the highest energy.

Figure 2.12 shows I_d-V_D characteristics of the SiC-FET for several temperatures and for two substrate bias conditions. The drain current increases with increasing temperature in the lower drain voltage region or in the lower current region. In contrast, in the higher current region, the current is suppressed with an increase in temperature due to a series resistance effect originating from lattice scattering. An increase in the resistance between source and intrinsic gate caused by an increase in temperature leads to a negative temperature dependence of the SiC-FET device in the higher current region. This behavior effectively averts a thermal breakdown, especially in a power device.

2.3.4.2 Comparison to the Static Induction Transistor

The I_d-V_D characteristic of the device shows similar behavior to that of a static induction transistor (SIT) (Figures 2.11 and 2.12) [99]. Therefore we evaluated the amplification factor we found by modifying the equation proposed for the SIT:

$$I_d = Aq\sqrt{\frac{kT}{2\pi m_n^*}}n_s \exp\left(-\frac{qV_{G'S}}{kT}\right)\exp\left\{\frac{q\left(-\eta V_G + \frac{V_D}{\mu}\right)}{kT}\right\} \tag{2.10}$$

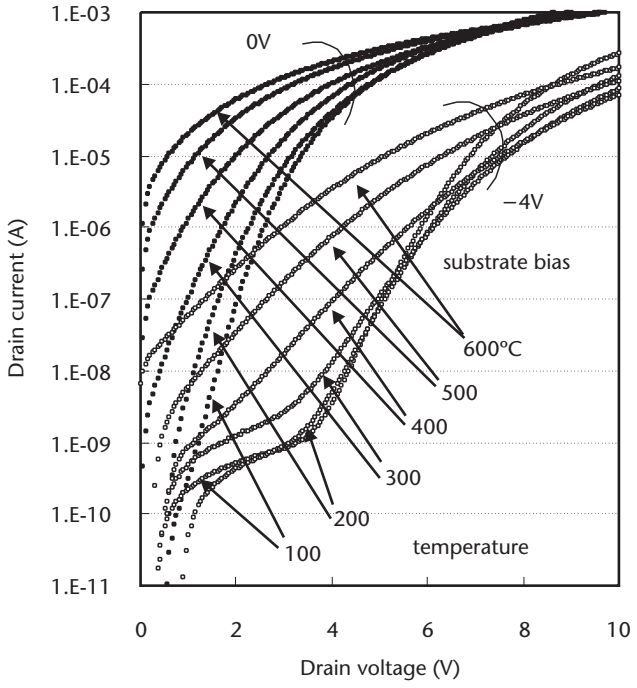


Figure 2.12 Temperature dependence of the drain current-voltage characteristics in 0.5% O_2 in Ar under two substrate bias conditions. (*From:* [97]. © 2004 Material Science Forum. Reprinted with permission.)

with $n_S = N_C \exp\left(\frac{E_C - E_F}{kT}\right)$.

Here the expression $qV_{G'S}$ is the diffusion potential between the intrinsic gate and source region, qV_G is the surface potential of the n^- region just under the gate electrode, η is the efficiency of qV_G for the intrinsic gate potential, is the amplification factor, that is the efficiency of the applied drain voltage on the intrinsic gate. Figure 2.13 shows a schematic band diagram of the device from source to drain through the intrinsic gate for an applied drain voltage, V_D. A change in ambient gas leads to a change in gate potential qV_G. This changes the intrinsic barrier height and gives rise to a change in drain voltage at a constant drain current.

When the drain voltage is $V_{D(H2)}$ for $V_{G(H2)}$ in H_2 ambient and is $V_{D(O2)}$ for $V_{G(O2)}$ in O_2 ambient, a change in drain voltage for a certain drain current is given by

$$\Delta V_D \equiv V_{D(O2)} - V_{D(H2)} \equiv \eta\mu\left(V_{G(O2)} - V_{G(H2)}\right) \tag{2.11}$$

ΔV_D is a change in drain voltage caused by an ambient change from O_2 to H_2 for the case when the drain current is kept constant. ($V_{G(O2)}$–$V_{G(H2)}$) is a change in surface potential of the n^- region just under the gate electrode. This equation shows that a change in surface potential can be amplified through the product of η and μ.

The influence of substrate bias V_{sub} on η and μ can be estimated from (2.10) using the linear region of the log (I_d) versus V_D curve. From the dependence of the inclination on temperature, the values of $1/\mu$ are obtained. It is almost independent

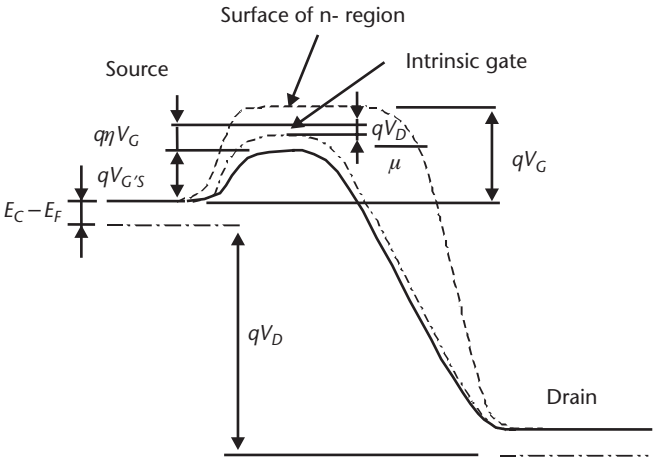


Figure 2.13 Schematic band model of the region from source to drain through the intrinsic gate with an applied drain voltage, V_D. (*From:* [98]. © 2003 IEEE. Reprinted with permission.)

of the ambient and decreases with increasing negative substrate bias. From the dependence of the vertical axis intercept on temperature, η is calculated. The value in O_2 ambient is higher than that in H_2 ambient and increases with an increasing negative substrate bias. This effect is attributed to the intrinsic gate in the n^- region below the insulator [99].

2.3.4.3 Other Wide Bandgap FET Devices

GaN modulation-doping field-effect transistors (MODFETs) have been developed by Pyke [100]. These are operated in a constant drain current mode. Pt and Rh catalytic metal gates are used to detect and distinguish between hydrogen and carbon monoxide. This device shows the best high-temperature performance of the GaN and AlGaN-based devices reported so far. It performs at temperatures as high as 600°C for some time. However, it is not clear if the failure at higher temperatures is due to the device itself or due to packaging, which is a critical issue at these temperatures.

Schalwig [21] et al. and Stutzmann [94] et al. have processed HEMTs with the structure Pt/GaN/AlGaN/GaN or Pt/AlGaN/GaN and tested their sensor performance. Owing to the band-offsets and the discontinuous change in the spontaneous and piezoelectric polarization at the GaN/AlGaN interfaces, a two-dimensional electron gas (2-DEG) forms underneath the AlGaN barrier layer. The devices are processed on sapphire substrates by plasma-induced molecular beam epitaxy (PIMBE) at 800°C and show a response to H_2, HC, and CO, up to a temperature of 400°C. Some baseline drift indicates that improvements in the material quality are needed [21, 94].

GaAs JFET devices have been tested as gas sensors. An n-type SnO_2 layer was used to form a hetero-junction to the p-type channel region. Palladium on top of the SnO_2 caused the device to detect NO_2 at a device temperature around 200°C [101].

2.4 Sensor Properties at Elevated Temperatures, Influence of Hydrogen

High-temperature operation, ≥ 500°C, causes distinctive phenomena to occur in the case of hydrogen gas. At these elevated temperatures, atomic hydrogen easily diffuses through most materials, even diamond [102]. It can be expected that all wide band- gap devices operated at elevated temperatures are affected by hydrogen.

It has been shown by secondary ion mass spectroscopy (SIMS) measurements that Pt facilitates deuterium incorporation, which is most likely trapped on boron atoms, in p-type SiC at 600–800°C [103]. The penetration depth was 3 μm at 600°C for a 4-hour anneal in deuterium. This is due to the fact that hydrogen (deuterium) or hydrocarbons dissociate on the catalytic metal surface of Pt and hydrogen atoms are formed that diffuse through the metal and into the SiC at $T \geq 600$°C in an oxygen-deficient atmosphere. The hydrogen is only detected if trapped, for example, on boron or aluminium dopants or contaminants. This method was introduced as a simpler method to introduce hydrogen into the bulk material, without causing damage, as occurs, for example, during ion implantation. Also it has been discovered that a Ni contact can act as a source for the introduction of hydrogen atoms into p-type SiC, in contrast to an Au contact [104]. Ti did not introduce any hydrogen into the SiC bulk, but a large hydrogen peak was found in connection with the Ti contact. No hydrogen could be detected in n-type material for similar annealings in hydrogen (D_2) at 600–800°C. This may be because no suitable traps exist that make hydrogen visible in SIMS measurements. The hydrogen may be trapped or react with surface states or with defects or different impurities, such as compensational doping atoms in the SiC lattice, which in turn will affect the net carrier concentration in a device. This will show up as a change in the *I-V* characteristic of a Schottky diode.

Hydrogen introduced into the SiC lattice from both bulk and CVD growth may be trapped and cause changes in the properties of the material. Jansson et al. have reported that a post growth anneal at temperatures ≥ 1,000°C reduces the H content in the (p-type) layers, whereas the carrier concentration increases [104]. Hydrogen trapped on C and Si vacancies in the lattice are potential traps for free carriers, or generation sites for free minority carriers, which passivate dopants or prevent dopant activation [104, 105]. Boron (B) and/or aluminum (Al) dopants are also easily passivated by hydrogen through complex formation during different process steps such as epitaxial growth, plasma-hydrogenation, ion implantation, or treatment in hydrogen gas [104]. All this would lead to unwanted changes in the electrical properties. Janson et al. has recently shown that the dissociation energy for the Al-H complex has been determined to be 1.61 ± 0.02 eV, whereas the H-B complex is determined to be 2.51 ± 0.04 eV. The difference in the dissociation energy for the two complexes suggests that the atomic configurations are significantly different [105].

In a similar way hydrogen is introduced into Mg-doped GaN material during CVD growth in a hydrogen-containing atmosphere. Activation of Mg, the p-type dopant, has to be performed as a post growth anneal at 800°C, during which hydrogen migrates to the surface and desorbs. Contrarily, hydrogen remaining in nonannealed material will migrate during applied reverse bias into the depleted zone. This

H distribution can be retained if the temperature is lowered to room temperature [106]. Saeger et al. suggest that hydrogen diffusivity is unisotropic in the hexagonal GaN material (i.e., hydrogen diffuses more slowly along the *c*-axis of the material compared with the a-b plane [107]). The diffusion is activated with an activation energy of ~1.2 eV. Under applied bias, positively charged hydrogen atoms drift into a p-n junction, for example at temperatures as low as 300°C. A plasma source has been used to introduce hydrogen atoms into GaN at 250–350°C, and measurements of the conductivity temperature dependence suggest that hydrogen passivates Mg traps in the p-doped GaN. This causes a strong decrease of the hole concentration in the GaN [108].

In silicon devices, which are operated at temperatures below 200°C, hydrogen annealing at ≥ 450°C is used to passivate surface states at the oxide-semiconductor interface. Hydrogen forms electrically inactive complexes with the surface states.

In Section 2.4.1, we discuss the reversible influence of hydrogen on SiC-based capacitors and Schottky diodes when operated at elevated temperature.

2.4.1 Influence of Hydrogen on Capacitors

Ghosh et al. investigated Pt/SiO_2/SiC capacitors at high temperature (527°C) by in situ *C-V* spectroscopy in oxygen or hydrogen atmosphere [6]. Exposure to hydrogen resulted in a negative flat band voltage shift as well as a sharper transition from accumulation to inversion, that is, over a narrower voltage range (Figure 2.14). The broader transition in oxygen is accredited to the creation of a large number of interface states. Above 427°C, hydrogen diffuses through the SiO_2 insulator in millisecond time. From this, two hydrogen-induced phenomena are deduced, a chemically induced shift in the metal/semiconductor work-function difference and the passivation of charged states (D_{IT}) at the SiO_2/SiC interface. This has implications for the operation of a MOS capacitor in the constant capacitance mode because both reproducibility of the devices, as well as device response times, become dependent on the choice of operating point. For example, a response time in the order of 30 minutes when switching from hydrogen to oxygen was found and attributed to a slow emptying of interface states. They also conclude that in the upper part of the *C-V* curve

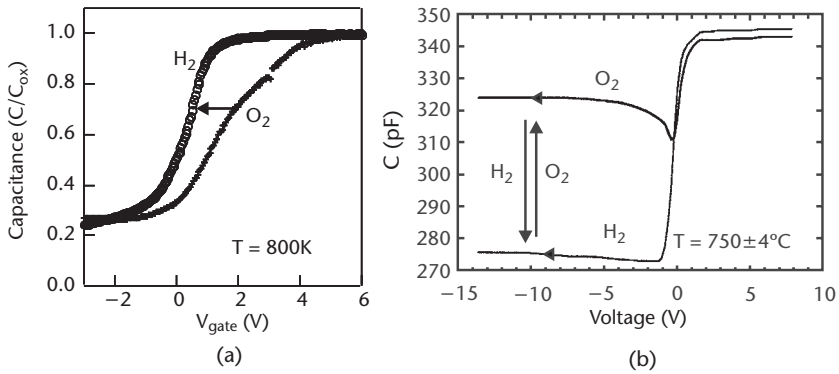


Figure 2.14 (a) *C-V* curve of a Pt/SiO_2/6H/SiC capacitor in oxygen and hydrogen at 527C (800K). (b) *C-V* curve of a Pt/$TaSi_x$/ SiO_2/6H/SiC capacitor at 750C (1,023K) in oxygen and hydrogen atmosphere (1 MHz and sweep rate 100 mV/s). (*From:* [109]. © 1995 American Institute of Physics. Reprinted with permission.)

both the work function and the interface states are influenced by hydrogen, whereas near midgap, which is found in the lower part of the *C-V* curve, the response is dominated by the metal/insulator work-function difference [110].

Baranzahi et al. have found that hydrogen affects the inversion capacitance value and that this is reversible when the hydrogen is removed. This proceeds at a considerable speed at temperatures above 650°C for a Pt/$TaSi_x$/SiO_2/SiC capacitor where the thickness of the SiO_2 is about 120 nm [109]. This effect is also seen in devices that do not contain the interfacial $TaSi_x$ layer. The inversion capacitance decreases in the presence of hydrogen at 750°C by about 50 pF [Figure 2.14(b)]. This was interpreted such that in the absence of hydrogen, there is a large minority carrier generation at the oxide-silicon carbide interface and/or in the surface layer of the silicon carbide, which increases the level of the inversion capacitance. In the presence of hydrogen, hydrogen atoms produced on the catalytic metal surface diffuse through the oxide and most likely form complexes with the species responsible for the carrier generation. The activation energy for this process to occur has been estimated to be 0.9 eV, whereas the reversible process requires an activation energy of 2.8–2.9 eV, indicating that the complex is rather stable [109]. This phenomenon was also investigated for the case of 4H-SiC by Tobias [111] et al. The reversible hydrogen-induced shift in the inversion capacitance took place also in this material but at a somewhat higher temperature. The higher bandgap of the 4H polytype requires a higher energy for minority carrier generation.

2.4.2 Influence of Hydrogen on Schottky Diodes

The reversible influence of hydrogen on the Schottky device characteristics have been studied by recording the *I-V* characteristics in an oxygen ambient at 300°C after annealing at 500°C or 600°C in either hydrogen or oxygen for 4 hours, 1 hour, or 10 minutes, respectively [112]. Annealings were performed for both n- and p-type samples. The temperature was lowered to 300°C in the annealing ambient and then changed to oxygen when needed (i.e., all *I-V* measurements were performed at 300°C in an oxygen ambient). For more details, see Figure 2.15.

Figure 2.15 shows the effect on the forward current for an n-type sample after a 4-hour anneal at 600°C. The shift is larger than that obtained after an anneal at 500°C. These effects are stable and reversible. The effect of annealing in oxidizing or reducing ambient increases with both time and temperature. The interpretation of this is that the hydrogen anneal-induced shift in the *I-V* curve is due to only one phenomena with a fairly high activation energy.

The annealing-induced shift of the *I-V* characteristics was also investigated for the case of p-type Schottky diodes by Unéus et al., and clear differences were shown between n- and p-type material. For n-type diodes, the *I-V* curves at 300°C, after annealing in oxidizing or reducing ambient at $T \geq 500$°C, are parallel shifted, as can be seen in Figure 2.15(b), whereas for the p-type samples the annealing-induced shift only shows up in the voltage range > 1V, as shown in Figure 2.15(a). That is, these *I-V* curves are not parallel-shifted. This difference may be related to the difference in barrier height between the n- and p-doped materials. An n-type Schottky diode with $TaSi_x$/Pt as gate material has a barrier height of approximately 1 eV as estimated by Nakagomi et al. [113]. This gives a very high barrier height for the

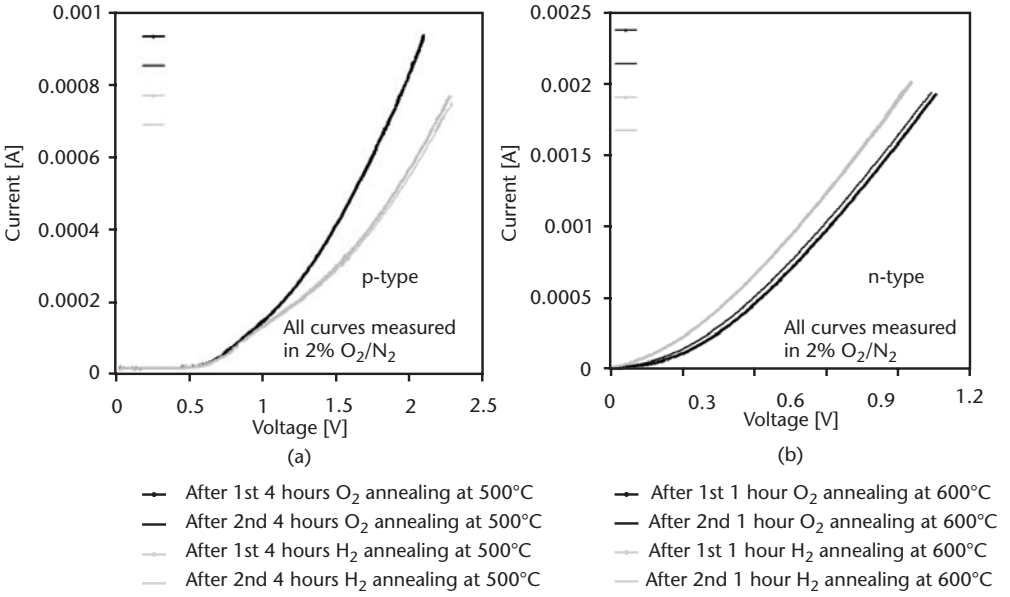


Figure 2.15 *I-V* characteristics measured in oxygen at 300°C for (a) p-type SiC Schottky diodes annealed at 500°C for 4 hours and (b) n-type Schottky diodes after 1-hour anneal in either 2% O_2/N_2 or 2% H_2/N_2-containing ambient at 600°C. The temperature is lowered to 300°C in the annealing ambient and then, when needed, changed to oxygen and after 20 minutes in oxygen, the *I-V* curve is recorded. Samples: The investigated MISiC Schottky devices were processed from wafers with p-type ($N_a = 6\times10^{15}$) and n-type ($N_d = 4.5\times10^{15}$) epilayers purchased from Cree, Inc., in 1997 [112]. The devices have gate contacts of 1-nm Ta + 100-nm Pt, or 10-nm $TaSi_x$ + 100-nm Pt and ohmic back contacts of 200-nm $TaSi_x$ + 400-nm Pt.

p-type material, since the SiC material has a bandgap of about 3 eV. This means that the current level for a p-type Schottky diode should be significantly lower, or that the resistance of the device is higher, compared with the n-type diode.

The difference observed between annealing at 4 hours or 10 minutes for the n-doped material indicates the existence of a hydrogen-induced phenomenon with a high activation energy, whereas the difference for p-type material indicates a phenomenon with lower activation energy.

We also investigated what happened to the hydrogen response after the annealings. The results can be seen in Figure 2.16. The sensor response to hydrogen is approximately the same after both the hydrogen and oxygen anneal. This indicates that the shift in the *I-V* characteristics due to the annealing is not connected to the sites involved in the hydrogen gas sensor response. The responses are in fact somewhat larger after the hydrogen anneal compared with after the oxygen anneal. This indicates that the sensor response to hydrogen has nothing to do with the observed shifts in Figure 2.15. It should also be observed that the hydrogen gas-induced response is in the same direction as the hydrogen annealing-induced shift in the *I-V* characteristics, in Figures 2.15 and 2.16.

Capacitance measurements were performed to investigate the $1/C^2$ versus voltage relationship. Measurements were performed at 300°C after annealing the samples in oxygen- or hydrogen-containing ambient. The curves show the same

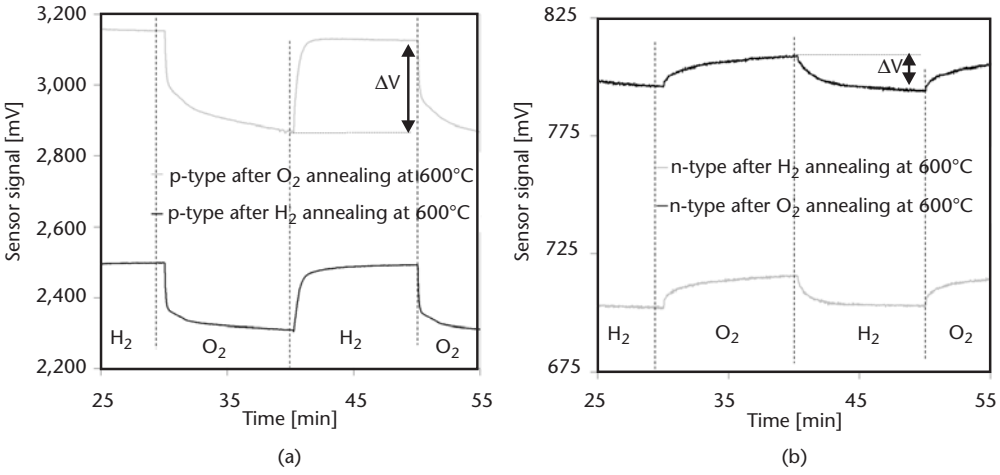


Figure 2.16 Sensor signals, the voltage over the diodes at 0.6 mA, for (a) p-type and (b) n-type Schottky diodes while exposed to alternating 2% O_2/N_2 or 2% H_2/N_2 ambient at 300°C.

characteristics after annealing in both hydrogen- and oxygen-containing ambient, which indicates that there is no dramatic change in the doping of the semiconductor. However, the slope of the curves changes at higher capacitance values, which indicates that the carrier concentration increases near the surface of the diodes.

Possible sites for the hydrogen anneal phenomena might be surface states, for example, on either side of the native oxide on top of the SiC surface. However, lattice defects and contamination in the surface layer of the epilayer may also be involved, as indicated in the $1/C^2$ curves. These may be on different sides of the thin insulator between the metal and the SiC. The thin insulator in these samples is probably a thin native oxide, SiO_x and oxidized Ta, Ta_xO_y, from the $TaSi_x$ layer.

It should also be noted that a nonparallel shift in the *I-V* characteristics due to annealing was always seen for the p-type material and sometimes for the n-type material. This may be due to the $TaSi_x$ layer, which may oxidize to different layer thickness in different components, or different thickness of the native oxide. A thick insulator introduces a serial resistance (see Section 2.3.2.2).

2.5 More Sensor Properties

Chemical gas sensors are characterized by properties such as sensitivity and selectivity, which has been discussed in Section 2.2. Properties like speed of response and long-term stability are of crucial importance for applications such as combustion control in car exhausts or flue gases from boilers.

2.5.1 Speed of Response

The speed of response is normally determined by the adsorption, desorption, and chemical reactions of the gas molecules on the sensor surface. The time constants

involved are in the second to millisecond time range. This means that the speed of response is defined by the type and structure of the catalytic metal and insulator in combination with the operation temperature of the device. It is normally not dependent on the choice of the semiconductor material. The shortest time constants for the gas response are in the millisecond range. Thus, device properties such as the carrier mobility, which are of great importance in electronic devices, are in general not important for chemical gas sensor devices.

In order to be able to measure the time constants for the gas response, it must be possible to change the gas atmosphere surrounding the sensor surface at a frequency of 1–20 Hz. This challenging experimental problem was elegantly solved by Tobias et al. through the development of moving gas outlets (MGOs), which are vibrated under the sensor surface by a small electrical engine [114]. A diagram of the construction is shown in Figure 2.17. Another solution was the use of a very small cavity, a 6-ml chamber in this case, around the sensor and high-speed injection of the gases through automotive injection valves [115]. In this way, the response time of $SrTiO_3$ sensors was estimated to be below 10 ms. Also Schalwig et al. built a system with MGOs to estimate time constants in the order of milliseconds, with a frequency range of 0.01–10 Hz [116]. In SiC-based capacitor devices with a gate material of 40-nm $TaSi_x$ plus 40-nm Pt, response time constants to hydrogen in the millisecond range have been measured at 200°C. Response time constants to CO, ethylene, and propane have been measured as less than 50 ms at a temperature of 500°C, whereas the time constant of the NO response was found to be several seconds [116].

The largest influence on the response speed is found to be the temperature. Wingbrant et al. has investigated the temperature-dependence of the response speed for a large number of different devices, with gate metals of 100-nm Pt + 10-nm $TaSi_x$, porous Pt, and porous Ir of different thicknesses used as both hydrogen and ammonia sensors [2] (Figure 2.18).

For cylinder-specific measurements, see Figure 2.18(a, b) and Section 2.7.1. It is important that the time constant of the gas response is below 10 ms. This is also the case for the cold start sensor, an application that is briefly described in Section 2.7.1. In Figure 2.18(a, b), it is shown that sensors with this response time have been

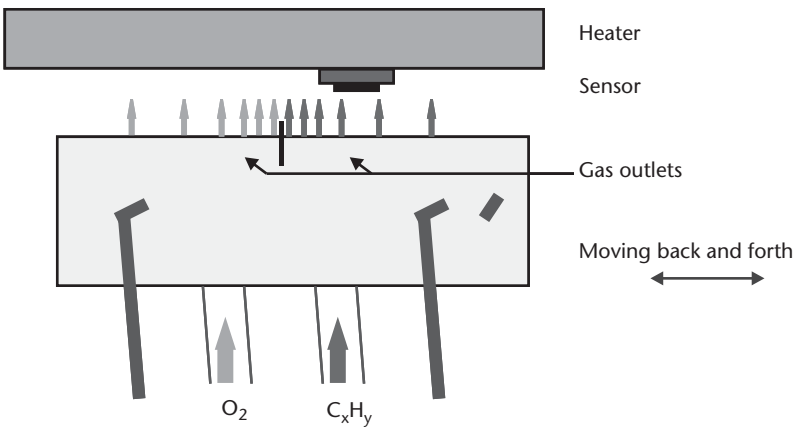


Figure 2.17 The gas outlets of the MGO equipment are moving back and forth under the sensors, exchanging their immediate environment at a high frequency. (*From:* [19]. © 2004 Springer-Verlag, Inc. Reprinted with permission.)

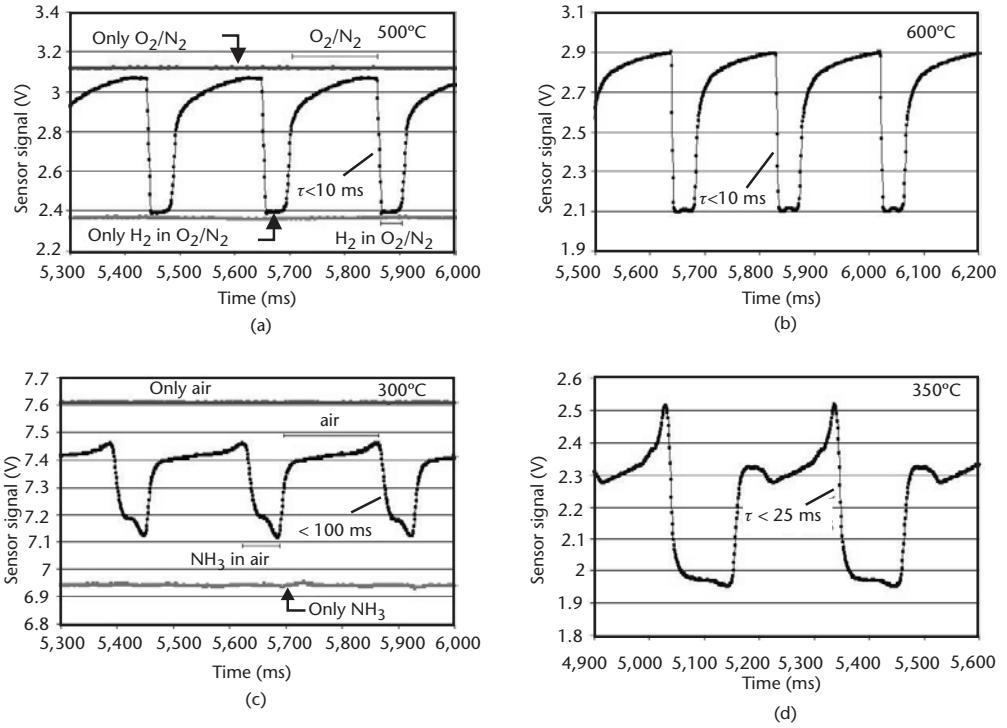


Figure 2.18 The sensor response to 1% H_2 / 0.4 % O_2 or 0.4% O_2 (carrier gs N_2) for a 10-nm $TaSi_x$ and 100-nm Pt sensor at (a) 500°C and (b) 600C and to 500-ppm NH_3/20% O_2 or 20% O_2 (carrier gas N_2) for (c) the 25-nm porous Pt sensor at 300°C and (d) the 60-nm porous Ir sensor at 350°C. The steady-state values at constant gas concentrations are also shown in (a, c). The two gas outlets are switched at a frequency of 5 Hz in (a, b) and 3 Hz in (c, d). The current between source and drain is 0.1 mA. Sampling is performed each ms.

demonstrated and that the MGO equipment previously described is capable of measuring it [2]. The sensor signal was sampled by the MGO equipment every millisecond over a period of 10 seconds at an exposure frequency of 5 Hz. The gas mixture from one of the outlets was chosen as 1% H_2 in 0.4% O_2 and from the other outlet as 0.4% O_2, which gives alternatively hydrogen and oxygen in excess.

An ammonia sensor has been developed for another automotive application, the selective catalytic reduction (SCR) of NO_x gases in diesel exhaust, for which a speed of response of 1 second is required (see Section 2.7.2). The response in the MGO was noted from sensors exposed to pulses of 500-ppm NH_3 in 20% O_2. The sensor signals were sampled every millisecond for 10-second periods at an exposure frequency of 3 Hz. The sensor response, as measured at 300°C, which is the temperature normally encountered in the SCR system, is shown in Figure 2.18(c). As can be seen in the figure, the sensor signal reaches its lowest level in less than 100 ms for both types of sensor. However, in this case, neither the highest or lowest signal level reaches the steady-state values, indicating that the gas exposure frequency is too high for the reactions on the sensor surface to reach a steady state. This means that the response time, traditionally defined as the time required for the response to reach from 10–90% of its final value, would have been longer if a slower-exposure frequency had been used. In Figure 2.18(d), the response is shown as measured at

350°C, when the gas surface reactions can be expected to occur at a faster rate. Now it is seen that the response has reached a steady-state value after exposure to the ammonia atmosphere. The extra dip in the response curve seen in the oxygen environment might be due to the slow diffusion of ammonia. Some gas molecules might still be left under the sensor surface in this experiment when hit by the oxygen gas outlet.

Due to the results mentioned in Section 2.4.1 by Tobias et al. [110] and Gosh [6] et al., the authors tested the response (not using the MGO equipment) of the MISiC-FET sensors at 500°C for different constant current levels. A current of 65 μA showed the same fast speed of response as for normal operation at 100 μA. For a constant current of 500 μA, the MISiC-FET showed the same size and speed of response but also a slow drift of the baseline, which was not sensitive to a change between oxygen and hydrogen.

2.5.2 Long-Term Stability

The long-term stability of a sensor that is to be used at high temperature and in corrosive atmospheres can be affected by many parameters. An overview of these is presented in this section.

The quality of the insulator under the catalytic material is an important parameter for high-temperature operation. The formation of good-quality insulators is especially difficult on wide bandgap materials, because the barrier height at the interface decreases as the bandgap of the semiconductor increases. Several techniques have been developed to improve the insulator quality, but it is still not as good as that on silicon. However, a $SiO_2/Si_3N_4/SiO_x$ (densified Si_3N_4) insulator stack, as used in MISiC-FET devices (see Section 2.3.4) has shown good stability at temperatures up to 500°C [51]. It has been reported that N_2O nitridation improves the SiO_2/n-type 6H-SiC interface [117, 118].

The effect of hydrogen annealing on the passivation of insulator-semiconductor interface states is well known. This is normally carried out at temperatures around 500°C, and normally improves the electrical characteristics of devices operated below this temperature. However, at high-temperature operation the hydrogen complexes at the insulator semiconductor interface may break again (see Section 2.4). An investigation has been carried out on Schottky sensors into the effect of annealing the devices in either H_2 or O_2 at 500°C or 600°C [112]. Changes in the *I-V* curves, which shows up as a change in the baseline of the devices by up to 200 mV, was experienced due to the different anneal cycles.

Mixing and reaction between adjacent layers in the sensor device has also been observed to be a problem at elevated temperatures. Capacitor sensors with a platinum contact layer, a buffer layer of tantalum silicide, and a thermal SiO_2 as the insulator were investigated by X-ray photoelectron spectroscopy (XPS) and AES after heat treatment at about 550°C in oxygen and hydrogen atmosphere for about 1 hour. It was concluded that considerable mixing of layers and some consumption of the oxide had occurred during this time [119]. Other researchers have also found interdiffusion of metals and insulators as well as silicide formation at elevated temperatures [84, 120]. Therefore, the introduction of new diffusion barriers might be necessary for the design of sensors operating at 600°C or above.

Ohmic contacts that stand corrosive environments at high temperatures are still to be fully developed, for a review, see [121]. It has been shown that TiW contacts covered by $TaSi_x$ + Pt as corrosion protection performed better at high temperature in an environment of H_2/O_2 pulses than standard alloyed Ni contacts, also with $TaSi_x$ + Pt protection [122]. During high-temperature operation, care should be taken when catalytic metals like Pt are used as contacts. It was shown by Linnarsson [103] et al., using SIMS, that hydrogen (deuterium) is introduced into SiC at temperatures ≥ 600°C through contacts of Pt and Ni (see Section 2.4).

2.6 Experimental

2.6.1 Sample Preparation

The SiC Schottky diodes and capacitors that have been processed by the authors were processed on either 6H or 4H substrates (n-type, about $1 \times 10^{19}cm^{-3}$) with a 5–10-μm n-type epilayer ($2–6 \times 10^{15}cm^{-3}$) [123, 124]. A thermal oxide was grown and holes were etched for the metal contacts. In the case of the Schottky sensors, the SiC surface was exposed to ozone for 10 minutes before deposition of the contact metal. This ozone treatment produces a "native" silicon dioxide of 10 ± 1 Å, as measured by ellipsometry [74, 75]. The MISiC-FET sensors (Figure 2.9) were processed on 4H-SiC, as previously described [125]. The catalytic metal contacts consisted of 10-nm $TaSi_x$/100-nm Pt, porous Pt, or porous Ir deposited by sputtering or by e-gun.

The layout of the MISiC-FET device connects the gate and source together. This creates a "two-terminal" device, which produces diode-like *I-V* characteristics, as shown in Figures 2.9 and 2.10. For more details of sample preparation, see [1, 125].

The sensor signal is the change in voltage of the device measured at a constant current of 0.1mA.

2.6.2 Gate Metal Deposition

Two different kinds of catalytic metal structure are required. Thick films, which are assumed to be dense, are needed for high-temperature operation and detection of excesss oxidizing or reducing molecules in environments such as exhaust gases. Porous metal films are needed for selective detection of molecules such as NH_3, CO, NO, and HC in excess air in environments such as diesel exhausts or flue gases.

In the case of thick films, adhesion is a major problem for high-temperature operation, that is greater than 500°C. Also restructuring and even catalytic etching may occur during high-temperature operation in corrosive atmospheres [126]. Several adhesion layers, Ta, $TaSi_x$, Ti [73, 78, 79], have been used in the work carried out by the authors. But care must be taken in the use of these, as they can introduce a serial resistance in the Schottky sensors [73, 78]. Sputtered films have a better adhesion than evaporated films. Samman et al. [46] introduced laser-ablated Pt gate electrodes. These were very smooth compared with the sputtered Pt gates and they were much less susceptable to restructuring during high-temperature operation. Ghosh et al. used e-beam evaporation at a substrate temperature of 350°C to deposit Pt gate contacts on capacitor devices. The films adhere well to the substrate following repeated cycling up to 600°C [6].

The authors tested a technique developed by Krause et al. [127] that involves the use of a sputtering process at a high pressure, 50 mTorr. This produces films with large grains and good adhesion properties, which has the advantage of enabling metal patterning to be performed by using the lift-off process. These films also have a favorable porosity and thus perform very well as ammonia sensors, as described in Section 2.2.2 [52].

2.6.3 Mounting

For testing in both laboratory and industrial applications, the sensor chip produced by the authors is mounted by gluing onto a ceramic heater, which is attached to a 16-pin holder while maintaining an air gap underneath [Figure 2.19(b)]. This allows the sensor chip to be heated to 600°C, whereas the holder below stays at 200°C. A Pt 100 element is also glued to the heater and used for temperature control.

To carry out measurements in exhaust gases, the 16-pin holder is mounted in a specially designed tube [Figure 2.19(a) [128], which was improved recently [52]. The exhaust gases are cooled while passing through the tube, which makes it possible to make measurements with the sensor chip at a constant temperature that is somewhat below the exhaust gas temperature.

Hunter et al. have mounted their sensors by gluing the SiC sensor chip onto a thin membrane realized by spin-on glass, with a heater and temperature detector underneath. This mounting technique enabled operation of the sensor at 600°C with a heater power of close to 1W [4].

Micromachining in SiC is developed by several groups, for a review see [129]. Solzbacher et al. have constructed a microhotplate based on a SiC-membrane and a HfB_2 thin-film heater, where the active part of the membrane is separated from the surroundings by six SiC microbridges. The heater is designed for operation temperatures up to 700°C and can be operated at 400°C with a power of 35mW [130, 131]. Boston Microsystems also offers a monolithic microhotplate in SiC [132].

2.6.4 Device Operation

It is advantageous to operate the FET devices in a constant current mode using a feedback system to compensate for the voltage change caused by the gas molecules.

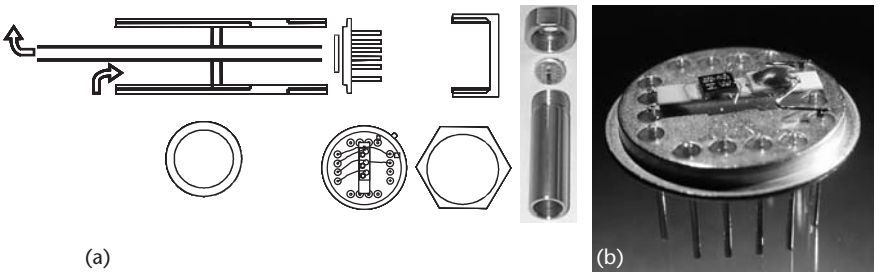


Figure 2.19 (a) The tubing mounting used for engine exhaust measurements. The flow direction of the gas is indicated by the arrows. To the left a schematic drawing of the device is shown, and to the right a photograph of the real device without the inner tube. (b) A sensor chip mounted together with a ceramic heater and a Pt-100 element on a 16-pin holder. (*From:* [128]. © 2003 Elsevier B.V. Reprinted with permission.)

It is considered to be more relevant to measure the voltage change, and it has been proposed this will give less baseline drift because the electric field over the sensor remains constant [16, 47].

The testing of the basic properties of the SiC devices is often performed in intermittent pulses of oxygen and hydrogen (1% O_2/N_2, 60 seconds, and 3% H_2/1% O_2/N_2, 30 seconds). This treatment is chosen since the corrosive oxygen atmosphere combined with the hydrogen/oxygen atmosphere can be regarded as very rough for the catalytic metals. For example, catalytic etching is known to take place in O_2/H_2 at temperatures above 450°C [126]. This treatment has been used by the authors to speed up aging phenomena in the sensors. In this way, improvement of the stability and reproducibility of the gas response can be achieved.

2.7 Applications

The MISiC and MISiC-FET sensors have been tested in a variety of applications, both in simulated environments in the laboratory [24, 116] and in real applications in the field [51, 76, 77, 128, 133, 134]. The authors have identified several areas in automotive and industrial applications where the excellent properties of SiC can be exploited. This section will review applications in both car exhaust gases and flue gases from boilers.

2.7.1 Petrol Engine Exhausts

The SiC-based MISiC sensors have been used to demonstrate cylinder-specific control of the combustion process in car engines [128, 133, 134]. Prerequisites for this application are gas responses in the order of a few milliseconds [2, 114] and a sensitivity to the change between oxidizing and reducing gases at very high temperatures [128]. Tests have been performed in an engine test bench using both MISiC-FET transistor sensors and MISiC Schottky sensors operated at about 600°C with a catalytic gate metal of 100-nm Pt with a 10-nm layer of $TaSi_x$ underneath [128, 133, 134]. During field tests, the SiC sensor is placed in the exhaust system at the point where the four outlet pipes from the cylinders join together. The signal from a Schottky diode sensor is shown in Figure 2.3, when it is operated at 600°C in the exhaust of a four-cylinder engine where the air-to-fuel ratio to one cylinder is deliberately run fuel-rich. The deviating cylinder is immediately identified by a sharp dip in the sensor signal. Also MISiC-FETs have been successfully operated in a similar experiment [133]. The MISiC sensors are fast enough to identify the deviating cylinder during on-line monitoring.

Chemometric evaluation methods can be applied to the signal from a single sensor by feeding the whole data set into an evaluation program [133, 135]. Both principle component analysis (PCA) and partial least square (PLS) models were used to evaluate the data. These are chemometric methods that may be used for extracting information from a multivariate data set (e.g., from sensor arrays) [135]. The PCA analysis shows that the MISiC-FET sensor differentiates very well between different lambda values in both lean gas mixtures (excess air) and rich gas mixtures (excess fuel). The MISiC-FET sensor is seen to behave as a linear lambda sensor [133]. It

should be noted that the sensor in these measurements is operated at 500°C, whereas the binary responding sensor in Figure 2.5(a) is operated at 600°C [56]. Fast algorithms are available that would make it possible to use a sensor array and evaluate the signals by chemometric methods for on-line control of the engine by gas sensors.

During a cold start of a car engine, as much as 95–98% of the total emission during an entire test driving cycle is emitted [128]. Therefore, a sensor that functions even during this period of the engine cycle is highly desirable. During a cold start, water droplets form on the cold walls of the exhaust pipe and are subsequently carried downstream by the gas flow. A cold-start sensor then has to tolerate the thermal shock of being hit by these water droplets. Zirconia is a rather brittle ceramic material. Therefore, vehicle manufacturers currently choose to prevent the zirconia lambda sensor, which is used to control the air-to-fuel ratio of the engine, from functioning until the engine is warm [86].

One way to solve this problem, and thereby control emissions directly from the start, is to use a sensor based on a material more resistant to thermal shock as a cold-start sensor [128]. SiC, as the second hardest material in existence only surpassed by diamond, is such a material and has therefore been tested for its suitability as a cold-start sensor. The water-splash resistance of SiC is still not verified because these experiments are complicated to perform in a laboratory engine test bench.

The sensitivity of the sensors toward λ was tested in a 5-cylinder, 2.5-liter turbo engine, in a test bench at Volvo Cars in Gothenburg, Sweden [128]. The sensor holder was placed in a tube mounting [Figure 2.19(a)] and plugged into the exhaust pipe of the engine, between the manifold and the catalytic converter. The tube mounting was used to cool the gases because the exhausts are at a temperature of 700–900°C and the 16-pin holder [Figure 2.19(b)] cannot withstand this temperature. It is also important to be able to control the temperature of the sensors during operation. The lambda value in the engine was varied during idle running. It was shown that the MISiC-FET sensor signals responds to lambda in the 0.98–1.06 range.

2.7.2 Diesel Engine Exhausts

SCR is a process by which NO_x gases in diesel exhausts can be reduced to levels that will meet future legislation. SCR is based on the reduction of NO_x in the catalytic converter by the injection of ammonia or urea into the exhaust gases before they enter the catalytic converter, where NO_x and NH_3 react to form N_2 and H_2O. The ammonia injection process may be controlled by measuring either the ammonia or nitric oxide slip after the catalytic converter. Such an ammonia sensor should be able to tolerate contaminants such as particles in the exhaust gases and should show very low cross sensitivity to NO_x and HC. Typical diesel exhaust contains 3–9% CO_2, 50–250 ppm CO, 6–12% O_2, 200–1,000 ppm NO_x, and 130–260 ppm HC. Furthermore, the response to NH_3 should have a time constant in the order of 1 second.

The MISiC-FET sensor operated at 300°C has demonstrated very promising results in this application [52, 76]. In Figure 2.20, the sensor response to NH_3 obtained from two MISiC-FET sensors with porous Pt gates is compared with the NH_3 concentration as measured by an optical instrument [52]. It is seen that the MISiC-FET sensors follow the optical signal very closely. It can also be noted that

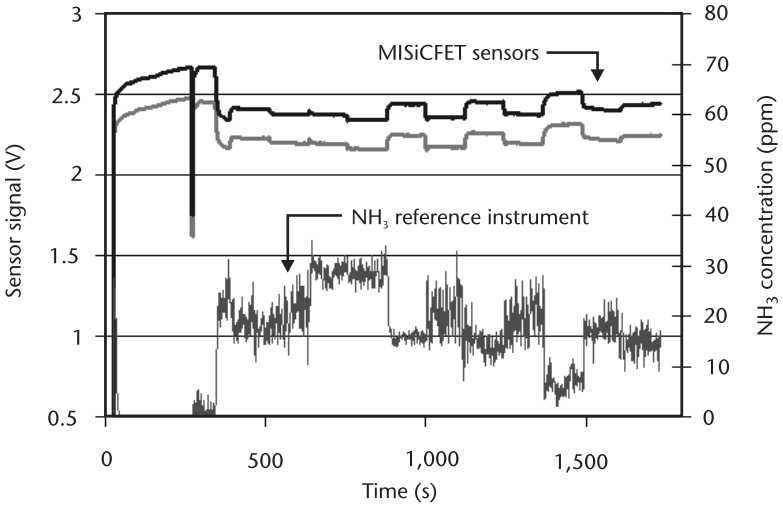


Figure 2.20 The sensor signal from two MISiC-FET sensors (upper curves) and the optical reference instrument (lower curve) during engine test rig measurements to simulate standard drive. (*From:* [52]. © 2004 IEEE. Reprinted with permission.)

even very small concentrations of ammonia produce a significant response in the MISiC-FET sensors, which is an important fact if the sensor is to detect small amounts of ammonia that slip through the catalytic converter. At a device temperature of 300°C, the time constant for the sensor response is estimated to be 50 ms [see Figure 2.18(c) and Section 2.5.1], which falls well within the required limit.

Although the response to NH_3 of a MISiC-FET with a porous Pt gate shows an optimum at around 250°C, an operation temperature of 300°C is chosen because it has been observed that this ensures a clean sensor surface even in diesel exhaust [76]. The choice of Ir as the gate material produces a high NH_3 sensitivity over a broader temperature range and at a somewhat higher temperature, as shown in Figure 2.4 [23].

Schalwig et al. have tested the feasibility of using a SiC MOS capacitor sensor containing a contact metal of 40-nm $TaSi_x$ plus 45-nm Pt to detect NO_x and HC after the catalytic converter. This was carried out by simulating lean burn engine exhausts [116]. It was observed that the sensor signal increased for NO_x detection and decreased for HC detection. This could permit this sensor to be used in a sensor array to differentiate these two gases.

2.7.3 Flue Gas Monitoring

In flue gases MISiC sensors can be used to either monitor the gas components, such as CO, nitric oxide (NO), and oxygen, or identify different modes of combustion in the boilers of small power plants. In this way, it is possible to optimize the combustion in boilers of about 0.5–5 MW in which optical techniques such as Fourier transform infrared (FTIR) are too expensive and complex. The authors have performed measurements in a 100-MW boiler, which has been used to heat houses and industries and generate electricity in Nyköping, Sweden, and in which there was a natural randomization of the flue gases [59]. Data was collected over several

months. The data from the sensors was evaluated using PCA and PLS models [135]. The results indicate the possibility to use an array of sensors and chemometric data evaluation to control the operation mode of the boiler as well as fine-tuning of the combustion by measuring the CO concentration in the preferred boiler mode. The MISiC sensors have been operated in the flue gas environment at 300°C for a total of 6 months without failure.

2.8 Outlook and Conclusions

The technology of field-effect devices based on high bandgap materials is rapidly becoming mature as a technology for mass-production of sensors. Material properties have improved to enable long-term stable devices and the processing technology allows batch processing. The robustness of the materials and their tolerance of extreme environments makes them very attractive for use in high-temperature and corrosive environments. GaN, AlN, and diamond have larger bandgaps than SiC and will probably be important as sensor materials in the future. However, their production and processing technology is not so mature as that of SiC, and commercialization of devices produced on these materials is expected at a somewhat later date than for those produced on SiC. The chemical inertness of wide bandgap materials also make them biocompatible and thus interesting as biosensor material [136].

A number of field-effect devices such as capacitors, Schottky diodes, p-n junctions, and transistors have been explored for use as chemical gas sensors. Advanced transistor sensors have been demonstrated in both SiC and GaN. The use of transistor devices has many advantages, such as greater stability and simple electronic circuitry. It also permits the use of less-conducting gate materials, which enables a greater range of catalytic materials to be used. MISiC-FETs can be operated over a large temperature range, from 100°C to 700°C. This makes it possible to design arrays of sensors, which enables these sensors to be used in a large number of applications, such as in combustion engine and for flue gas monitoring. The small size and versatility of these sensors also permits their use in sensor systems such as the electronic nose.

The gas response of the field-effect devices is determined by the catalytic properties of the contact material, which includes both the catalytic layer and the underlying material. The temperature plays a dominant role in the detection process because the origin of the gas response is found in the chemical reactions that take place on the sensor surface, and it is furthermore also influenced by the mass transport properties of the molecules in the gas phase. This permits arrays of sensors of a common design to be tailor-made for detection of a range of gases and for use in a range of applications

SiC material and processing technology is rapidly reaching maturity. Wafers of 3 inches in diameter are already available and 4-inch wafers are expected to follow soon. SiC also offers the possibility to integrate electronics on the sensor chip in the future, which makes this technology very attractive. Free-standing chips of SiC can include in the future arrays of chemical sensors, a heater, temperature control, and signal processing circuitry. The high thermal conductivity of SiC will permit heating of these chips up to 600°C within a few seconds and also rapid cooling

should be possible. Furthermore, microhotplates based on SiC have already been demonstrated.

SiC technology provides the opportunity for the exploitation of chemical gas sensors in the near future in environments and applications that are problematic today. The extension of this technology to these areas will enable the reduction of unwanted emissions and will promote reductions in the use of fuel and energy, resulting in positive implications for natural resources and the environment.

Acknowledgments

Our research on high-temperature chemical sensors based on silicon carbide is supported by grants from the Swedish National Board for Industrial and Technological Development, and Swedish Industry through the Center of Excellence, S-SENCE, the Swedish Research Council for Engineering Sciences, and the SSF-SiCEP program. Measurements have been carried out together with the Laboratory of Applied Physics at AB Volvo Technology Corporation in Göteborg, Sweden; Vattenfall Development, Älvkarleby, Sweden; AppliedSensor, Mjärdevi Science Park, Linköping, Sweden; Ford Research Laboratory, Dearborn, Michigan; and Mecel AB, Åmål, Sweden. The MISiC-FET devices were designed and processed at ACREO AB in Kista, Sweden. The skillful metal gate deposition and mounting of the sensor chips was performed by Jeanette Nilsson and Evald Mild, respectively, at Linköping University in Sweden.

References

[1] Lloyd Spetz, A., et al., *Phys. Stat. Sol. (a),* Vol. 185, 2001, p. 15.
[2] Wingbrant, H., I. Lundström, and A. Lloyd Spetz, *Sens. Actuators B*, Vol. 93, Nos. 1–3, 2003, pp. 286–294.
[3] Nakagomi, S., T. Azuma, and Y. Kokubun, *Electrochemistry*, Vol. 70, 2002, p. 174.
[4] Hunter, G. W., et al., *Mat. Sci. Forum*, Vols. 338–342, 2000, p. 1439.
[5] Samman, A., et al., *J. Appl. Phys.*, Vol. 87, No. 6, 2000, p. 3101.
[6] Ghosh, R. N., P. Tobias, and B. Golding, *Mat. Res. Symp.*, Vol. 742, 2003, p. 363.
[7] Vasiliev, A., et al., *Sens. Actuators B*, Vol. 49, 1998, p. 133.
[8] Kim, C. K., et al., *Sens. Actuators B*, Vol. 77, 2001, p. 455.
[9] Roy, S., C. Jacob, and S. Basu, *Sens. Actuators B*, Vol. 94, 2003, p. 298.
[10] Serina F., et al., *Appl. Phys. Lett.*, Vol. 79, No. 20, 2001, p. 3350.
[11] Schalwig, J., et al., "Hydrogen Response Mechanism of Pt-GaN Schottky Diodes," *Appl. Phys. Lett.*, Vol. 80, No. 7, 2002, p. 1222.
[12] Gurbuz, Y., et al., *IEEE Trans. Electron Devices*, Vol. 46, No. 5, 1999, p. 914.
[13] Tilak, V., et al., *Proc. MRS Fall Meeting*, 2003.
[14] Weidemann, O., et al., "Influence of Surface Oxides on Hydrogen-Sensitive Pd-GaN Schottky Diodes," *Appl. Phys. Lett.*, Vol. 83, No. 4, 2003, p. 773.
[15] Kokubun, Y., T. Seto, and S. Nakagomi, *Jpn. J. Appl. Phys.*, Vol. 40, 2001, p. L663.
[16] http://www.infineon.com/cgi/ecrm.dll/ecrm/scripts/prod_cat.jsp?oid=-8681.
[17] Brown, D. M., et al., *Electrochem. Soc. Proc.*, Vol. 3, 2002, p. 83.
[18] Bertuccio, G., et al., *Mat. Sci. Forum*, Vols. 433–436, 2003, p. 941.

[19] Lloyd Spetz, A., and S. Savage, in *Silicon Carbide: Recent Major Advances*, W. J. Choyke, H. Matsunami, and G. Pensl, (eds.), New York: Springer, 2004, pp. 869–896.
[20] Nakagomi, S., et al., *Sens. Actuators B*, Vol. 45, 1997, p. 183.
[21] Schalwig, J., et al., *Phys. Stat. Sol. (a),* Vol. 185, No. 1, 2001, p. 39.
[22] Ekedahl, L.-G., M. Eriksson, and I. Lundström, *Acc. Chem. Res.*, Vol. 31, No. 5, 1998, p. 249.
[23] Wingbrant, H., et al., *Proc. IEEE Sensors,* Toronto, Canada, October 22–24, 2003, pp. 428–433.
[24] Andersson, M., et al., *Proc. CAPoC6,* Brussels, Belgium, October 22–24, 2003, pp. 555–565.
[25] Fogelberg, J., et al., *J. Appl. Phys.*, Vol. 78, No. 2, 1995, p. 988.
[26] Yates, D. E., S. Levine, and T. W. Healy, *J. Chem. Soc., Faraday Trans.*, Vol. 70, 1974, p. 1807.
[27] Salomonsson, A., et al., *Proc. IMCS,* Boston, MA, July 7–10, 2002, p. 500.
[28] Neuberger, R., et al., *Mat. Sci. Eng.*, Vol. B93, 2002, p. 143.
[29] Schalwig, J., et al., *Mat. Sci. Eng.*, Vol. B93, 2002, p. 207.
[30] Spetz, A., M. Armgarth, and I. Lundström, *J. Appl. Phys.*, Vol. 64, No. 3, 1988, p. 1274.
[31] Löfdahl M., et al., *Sens. Actuators B*, Vol. 80, 2001, p. 183.
[32] Holmberg M., and I. Lundström, *Appl. Surf. Sci.*, Vol. 93, 1996, p. 67.
[33] Eriksson, M., and L.-G. Petersson, *Surf. Sci.*, Vol. 311, 1994, p. 139.
[34] Löfdahl, M., "Spatially Resolved Gas Sensing," *Linköping Studies in Science and Technology,* Dissertation No. 696, 2001, pp. 93–111.
[35] Åbom, A. E., et al., *J. Appl. Phys.*, Vol. 93, No. 12, 2003, p. 9760.
[36] Lundstsröm, I., et al., *Sens. Actuators B*, Vols. 13–14, 1993, p. 16.
[37] Dannetun, H., I. Lundström, and L. Petersson, *Surf. Sci.*, Vol. 193, 1988, p. 109.
[38] Svenningstorp, H., et al., *Sens. Actuators B*, Vol. 77, 2001, p. 177.
[39] Eriksson, M., and L.-G. Ekedahl, *Sens. Actuators B*, Vol. 42, 1997, p. 217.
[40] Schalwig, J., et al., "Response Mechanism," *IEEE Sensors Journal,* Vol. 2, No. 5, 2002, p. 394.
[41] Dean, V. W., M. Frenklach, and J. Phillips, *J. Phys. Chemi.*, Vol. 92, 1988, p. 5731.
[42] Nylander, C., M. Armgarth, and C. Svensson, *J. Appl. Phys.*, Vol. 56, No. 4, 1984, p. 1177.
[43] Fridell, E., et al., *Topics in Catalysis*, Vol. 16/17, No. 1–4, 2001, p. 133.
[44] Holmes, P. D., et al., *Catalysis Today*, Vol. 9, 1991, p. 15.
[45] Olander, J., and K. Larsson, *J. Phys. Chem.*, Vol. 103, 1999, p. 9604.
[46] Samman, A., et al., *Sens. Actuators B*, Vol. 63, 2000, p. 91.
[47] Lundström, I., M. Armgarth, and L.-G. Petersson, *CRC Crit. Reviews*, Vol. 15, No. 3, 1989, p. 201.
[48] Armgarth, M., T. H. Hua, and I. Lundström, *Techn. Digest. Transducers '85,* Philadelphia, PA, 1985, p. 235.
[49] Hughes, R. C., et al., *J. Appl. Phys.*, Vol. 62, 1987, p. 1074.
[50] Löfdahl, M., et al., *J. Appl. Phys.,* Vol. 91, 2002, p. 4275.
[51] Wingbrant, H., et al., *Mat. Sci. Forum*, Vols. 433–436, 2003, p. 953.
[52] Wingbrant, H., et al., *IEEE Sensors Journal*, 2004.
[53] Spetz, A., M. Armgarth, and I. Lundström, *Sens. Materials*, Vol. 4, 1988, p. 187.
[54] Unéus, L., et al., *Sens. Materials*, Vol. 11, No. 5, 1999, p. 305.
[55] Marinova, T. S., and K. L. Kostov, *Surf. Sci.*, Vol. 185, 1987, p. 203.
[56] Baranzahi, A., et al., *Sens. Actuators B,* Vol. 43, 1997, p. 52.
[57] Baranzahi, A., et al., *J. Electr. Soc.*, Vol. 145, No. 10, 1988, p. 3401.
[58] Rinnemo, M., et al., *Surf. Sci.*, Vol. 376, 1997, p. 297.

[59] Unéus, L., et al., *Proc. Transducers '01 and Eurosensors XV*, Munich, Germany, 2001, p. 1754 (4D3.10P).
[60] Hunter, G. W., et al., *Mat. Sci. Forum*, Vols. 264–268, 1998, p. 1093.
[61] Lundström, K. I., M. S. Shivaraman, and C. M. Svensson, *J. Appl. Phys.*, Vol. 46, No. 9, 1975, p. 3876.
[62] Spetz, A., A. Arbab, and I. Lundström, *Proc. Eurosensors VI*, San Sebastian, Spain, October 5–7, 1992, p. 9.
[63] Hunter, G. W., et al., NASA Technical Memorandum, 106141, 1993.
[64] Savage, S. M., et al., *Mat. Sci. Forum*, Vols. 338–342, 2000, p. 1431.
[65] Svenningstorp, H., et al., *Mat. Sci. Forum*, Vols. 338–342, 2000, p. 1435.
[66] Nakashima, K., et al., *Mat. Sci. Forum*, Vols. 389–393, 2002, p. 1427.
[67] Muntele, C. I., et al., *Mat. Sci. Forum*, Vols. 338–342, 2000, p. 1443.
[68] Lloyd Spetz, A., et al., *Physica. Status Solidi. (a)*, Vol. 162, 1997, p. 493.
[69] Lloyd Spetz, A., et al., *IEEE Trans. Electron Devices*, Vol. 46, No. 3, 1999, p. 561.
[70] Tongson, L. L., et al., *J. Appl. Phys.*, Vol. 50, 1979, p. 1535.
[71] Shivaraman, M. S., et al., *Electron. Lett.*, Vol. 12, 1976, p. 483.
[72] Zemel, J. N., et al., *Sens. Actuators*, Vol. 1, 1981, p. 427.
[73] Nakagomi, S., H. Watanabe, and Y. Kokubun, *Chemical Sensors*, Vol. 17, Supplement B, 2001, (2A09), p. 50.
[74] Zangooie, S., et al., *Mat. Sci. Forum*, Vols. 338–342, 2000, p. 1085.
[75] Mikalo, R. P., et al., *Mat. Sci. Forum*, Vols. 353–356, 2001, p. 219.
[76] Svenningstorp, H., et al., *Proc. Eurosensors XIV*, Copenhagen, Denmark, August 27–30, 2000, p. 933 (W3E5).
[77] Unéus, L., et al., *Proc. ISOEN 2000*, Brighton, England, July 24–26, 2000, p. 291.
[78] Tobias, P., et al., *Mat. Sci. Froum*, Vols. 264–268, 1998, p. 1097.
[79] Nakagomi, S., Y. Shindo, and Y. Kokubun, *Physica. Status Solidi. (a)*, Vol. 185, 2001, p. 33.
[80] Lundberg, N., and M. Östling, *Physica. Scripta*, Vol. T54, 1994, p. 273.
[81] Papanicolaou, N. A., A. Christou, and L. Gipe, *J. Appl. Phys.*, Vol. 65, 1989, p. 3526.
[82] Madsen, L. D., et al., *Electrochemistry*, Vol. 71, 2003, p. 6394.
[83] Zetterling, C. -M., et al., *J. Appl. Phys.,* Vol. 82, 1997, p. 2990.
[84] Chen, L. -Y., et al., *Sci. Technol. A*, Vol. 15, 1997, p. 1228.
[85] Nakagomi, S., K. Okuda, and Y. Kokubun, *Sens. Actuators B*, Vol. 96, 2003, p. 364.
[86] Visser, J. H., and R. E. Soltis, *IEEE Trans. on Instrumentation and Measurement*, Vol. 50, 2001, p. 1543.
[87] Visser, J. H., et al., Meeting Abstract, No. 1131.
[88] Tobias, P., et al., *Proc. 8IMCS*, Basel, Switzerland, 2000, p. 149.
[89] Jacobsén, S., et al., *Proc. Transducers '01 and Eurosensors XV*, 2001, p. 832.
[90] Cerdà, J., J. R. Morante, and A. Lloyd Spetz, *Mat. Sci. Forum*, Vols. 433–436, 2003, p. 949.
[91] Sze, S. M., *Physics of Semiconductor Devices,* New York: John Wiley & Sons, 1981, pp. 513–515.
[92] Ebbing, D. D., *General Chemistry,* 5th ed., Boston, MA: Houghton Mifflin, 1996, p. 807.
[93] Cohen, S. S., and G. S. Gildenblat, in *VLSI Electronics Microstructure Science*, N. G. Einspruch, (ed.), Vol. 13, Orlando, FL: Academic Press, 1986.
[94] Stutzmann, M., et al., *Diamond and Related Mat.*, Vol. 11, 2002, p. 886.
[95] Zhu, W., et al., *Int. Ferroelectrics*, Vol. 44, 2002, p. 25.
[96] Savage S., and A. Lloyd Spetz, *Compound Semiconductor*, Vol. 6, No. 3, 2000, p. 76.
[97] Nakagomi, S., et al., *Mat. Sci. Forum*, Vol. 457–460, 2004, p. 1507.

[98] Nakagomi, S., et al., *Proc. IEEE Sensors*, Toronto, Canada, October 22–24, 2003, pp. 1168–1173.

[99] Nishizawa, J., T. Terasaki, and J. Shibata, *IEEE Trans. Electron Devices*, Vol. ED-22, 1975, p. 185.

[100] http://www.eere.energy.gov/ search button: Stephen C. Pyke.

[101] Wöllenstein, J., et al., *Sens. Actuators B*, Vol. 68, 2000, p. 22.

[102] Looi, H. J., et al., *Thin Solid Films*, Vols. 343–344, 1999, p. 622.

[103] Linnarsson, M. K., et al., *Mat. Sci. Froum*, Vols. 338–342, 2000, p. 937.

[104] Jansson, M. S, et al., "Hydrogen Diffusion, Complex Formation, and Dissociation in Acceptor-Doped Silicon Carbide," *Phys. Rev. B*, Vol. 64, 2001, p. 195202-1.

[105] Jansson, M. S., et al., "Hydrogen-Boron, Complex Formation and Dissociation in 4H-Silicon Carbide," *Appl. Surf. Sci.*, Vol. 184, 2001, p. 257.

[106] Wright, A. F., *J. Appl. Phys.*, Vol. 94, No. 4, 2003, p. 2311.

[107] Saeger, C. H., *J. Appl. Phys.*, Vol. 92, No. 12, 2002, p. 7246.

[108] Polyakov, A. Y., et al., *J. Appl. Phys.*, Vol. 94, No. 6, 2003, p. 3960.

[109] Baranzahi, A., A. Lloyd Spetz and I. Lundström, *Appl. Phys. Lett.*,Vol. 67, No. 21, 1995, p. 3203.

[110] Tobias, P., B. Golding, and R. N. Ghosh, *IEEE Sensors Journal*, Vol. 3, No. 5, 2003, p. 543.

[111] Tobias, P., et al., *Mat. Sci. Forum*, Vols. 264–268, 1998, p. 1089.

[112] Unéus, L., et al., *Mat. Sci. Forum*, Vols. 389–393, 2002, p. 1419.

[113] Nakagomi, S., et al., *Proc. Transducers '01 and Eurosensors XV*, Munich, Germany, June 10–14, 2001, p. 1758 (4D3.11P).

[114] Tobias, P., et al., *Sens. Actuators B*, Vol. 58, 1999, p. 389.

[115] Gerblinger, J., U. Lampe, and H. Meixner, *Sens. Actuators B*, Vols. 24–25, 1995, p. 639.

[116] Schalwig, J., et al., SAE Technical Paper Series, 2002-01-1095.

[117] Dimitrijev, S., et al., in *Silicon Carbide: Recent Major Advances*, W. J. Choyke, H. Matsunami, and G. Pensl, (eds.), New York: Springer, 2004, pp. 373–386.

[118] Jamet, P., et al., *Mati. Sci. Forum,* Vol. 389–393, 2002, p. 973.

[119] Lloyd Spetz, A., et al., *Thin Solid Films*, Vol. 299, 1997, p. 183.

[120] Danielsson, E., et al., *Mat. Sci. Forum*, Vols. 264–268, 1997, p. 805.

[121] Tanimoto, S., H. Okushi, and K. Arai, in *Silicon Carbide: Recent Major Advances*, W. J. Choyke, H. Matsunami, and G. Pensl, (eds.), New York: Springer, 2004, pp. 651–669.

[122] Unéus, L., et al., *Proc. ICSCRM2001*, Vol. 410, Tsukuba, Japan, October 28–November 2, 2001, p. 410.

[123] Cree Research Inc., Durham, NC, http://www.cree.com.

[124] Okmetic Oyj, Vantaa, Finland, http://www.okmetic.com.

[125] Savage, S., et al., *Mat. Sci. Forum*, Vols. 353–356, 2001, p. 747.

[126] Dean, V. W., M. Frenklach, and J. Phillips, *J. Phys. Chemi.*, Vol. 92, 1988, p. 5731.

[127] Krause, S., W. Moritz, and I. Grohmann, *Sens. Actuators B*, Vol. 9, 1992, p. 191.

[128] Wingbrant, H., et al., *Sens. Actuators B*, Vol. 93, Nos. 1–3, 2003, p. 295.

[129] Zorman, C. A., and M. Mehregany, in *Silicon Carbide: Recent Major Advances*, W. J. Choyke, H. Matsunami, and G. Pensl, (eds.), New York: Springer, 2004, pp. 671–698.

[130] Solzbacher, F., et al., *Sens. Actuators B*, Vol. 64, 2000, p. 95.

[131] Solzbacher, F., et al., *Sens. Actuators B*, Vol. 78, 2001, p. 216.

[132] http://www.bostonmicrosystems.com.

[133] Larsson, O., et al., "SAE Technical Paper Series, 2002-01-0847," *SAE2002*, Detroit, MI, March 4–7, 2002.

[134] Baranzahi, A., et al., "SAE Technical Paper Series 972940, Combustion and Emisson Formation in SI Engines," 1997, p. 231 (SP-1300).

[135] Box, G. E. P, W. G. Hunter, and J. S. Hunter, *Statistics for Experimenters: An Introduction to Design, Data Analysis, and Model Building,* New York: John Wiley & Sons, 1978.
[136] Steinhoff, G., et al., *Adv. Funct. Mater.*, Vol. 13, No. 11, 2003, p. 841.

CHAPTER 3

Silicon Carbide Technology and Power Electronics Applications[1]

C. Wesley Tipton IV and Stephen B. Bayne

The basic circuit topologies of switch-mode power conversion have been known for more than 100 years. One of the earliest examples is the hertzian oscillator shown in Figure 3.1. Here, the applied dc potential is converted to an ac current flowing in a tuned circuit. The switch and the coupled inductor form an electromechanical multivibrator that produces a chopped dc current in the primary winding. Note that a "snubber" circuit is connected between the contacts of the switch to provide a commutation path during turnoff. The snubber is needed to extend the life of the switch's contacts. As Severns [1] points out, although switch technologies continue to change, the basic physics of these circuits remains the same. This chapter provides an overview of power-conversion applications using the latest generation of SiC semiconductor devices. We explore the motivations for applying SiC technology, review recent SiC circuit demonstrations, and discuss the implications of high power-density electronics. We have divided power-circuit applications into three categories: dc-dc conversion, dc-ac conversion, and pulse-power applications. We have also included a section on high-temperature and high-voltage packaging that is an enabling technology for the application of SiC.

3.1 DC-DC Conversion

The purpose of dc-dc switched-mode power-conversion (SMPC) circuits is to condition or transform input dc power to the required dc output. These converters usually perform a step-up or step-down transformation of the input voltage. However, it is also possible to use these circuits in power-isolation applications where the input and output voltages are nearly equal. Because of their high conversion efficiency and power density, SMPC systems have found widespread use in applications ranging from low-power consumer electronics to very high-power industrial systems. SMPC circuits contain inductors and capacitors as energy storage components and semiconductor switches and diodes to transfer the energy from the input to the output. Although there are numerous SMPC circuit forms that address various aspects of the power-conversion spectrum, we will focus only on a few of the

1. The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the U.S. Army Research Laboratory or the U.S. government.

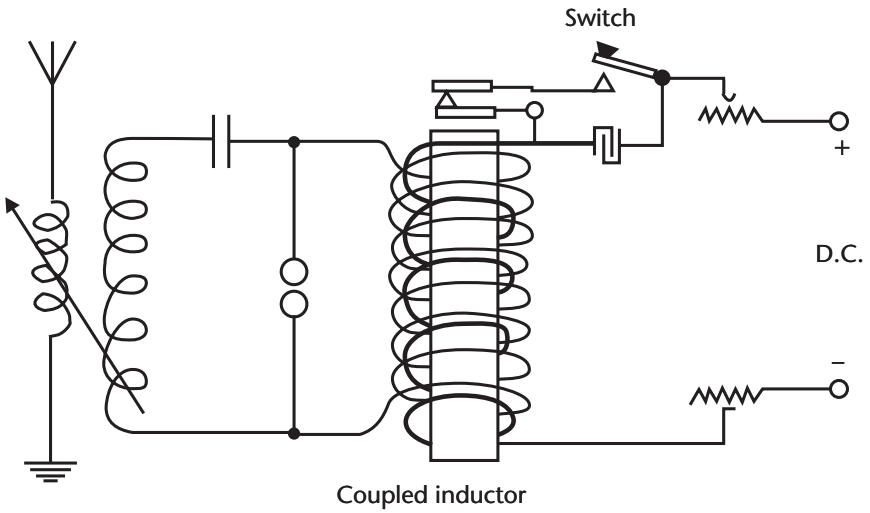


Figure 3.1 Hertzian oscillator (circa 1900) demonstrating basic switch-mode power-conversion technology. Note: $n_1 = n_p$ and $n_2 = n_s$.

basic topologies such as buck and full-bridge converters, as these have been widely used as demonstration circuits for SiC technology.

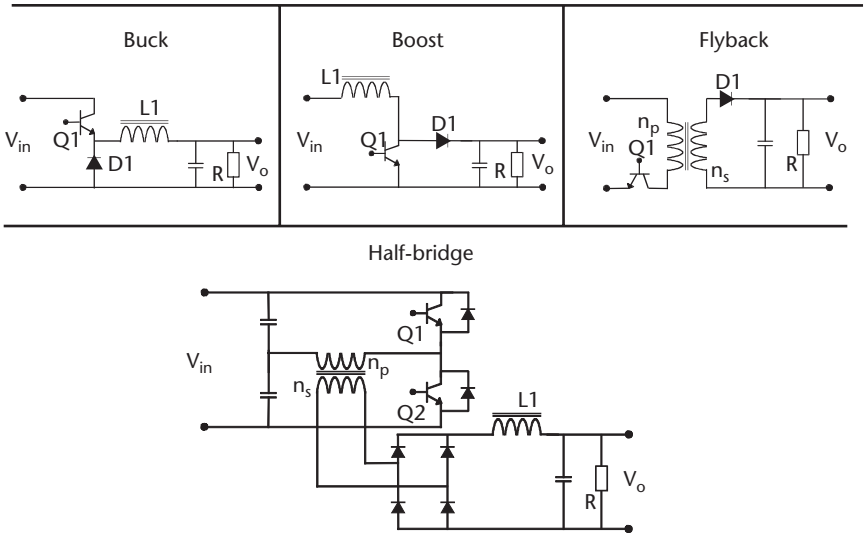
3.1.1 SMPC Circuit Topologies and Operation

Figure 3.2 shows a comparison of some common SMPC circuit topologies and their associated maximum current and voltage stresses. The buck, boost, and flyback converters are all single-switch circuits and have similar operating characteristics in that they use a switched inductor (or coupled inductor in the case of the flyback circuit) to store energy. A diode (D1) provides an alternate current path for the inductor to transfer its energy during a portion of the conversion cycle. The duty cycle (D) in these circuits is defined as

$$D = \frac{\tau}{T} \tag{3.1}$$

where τ is the conduction time of the transistor (Q1) and T is the total cycle time. In applications requiring galvanic isolation between the input and output or where a large step-up or step-down ratio is desired, transformers are typically used in SMPC circuits and bridge topologies are employed. The half-bridge circuit uses two switches to produce a bidirectional current in the primary winding of the transformer. The capacitor voltage divider biases one side of the primary winding at half the input voltage (V_{in}) so that the voltage imparted on the winding is one-half V_{in}. However, the maximum voltage stress on either switch remains V_{in}.

The full-bridge converter is the dominant circuit topology in high-power applications. In this circuit, the capacitor divider found in the half-bridge has been replaced with two switches. This allows the full input voltage to be applied across the primary winding. During one conduction cycle, either S1 and S4 or S2 and S3 are turned on simultaneously. For a given switch, the full-bridge circuit has twice the



	Buck	Boost	Flyback	Half-bridge*	Full-bridge*
Switch voltage	V_{in}	V_o	$V_{in}+V_o\left(\frac{n_1}{n_2}\right)$	V_{in}	V_{in}
Switch current	$I_R+\frac{\Delta I_{L1}}{2}$	$I_R(1-D)^{-1}+\frac{\Delta I_{L1}}{2}$	$I_R+\frac{n_2}{n_1}(1-D)^{-1}+\frac{\Delta I_{L1}}{2}$	$\frac{n_2}{n_1}\left(I_R+\frac{\Delta I_{L1}}{2}\right)+I_{mag}$	$\frac{n_2}{n_1}\left(I_R+\frac{\Delta I_{L1}}{2}\right)+I_{mag}$
Diode voltage	V_{in}	V_o	$V_{in}\left(\frac{n_2}{n_1}\right)$	$V_{in}\left(\frac{n_2}{n_1}\right)$	$2V_{in}\left(\frac{n_2}{n_1}\right)$
Diode current	$I_R(1-D)$	I_R	I_R	$\frac{I_R}{2}$	I_R

*Secondary diode ratings

Figure 3.2 Switch-mode power-conversion circuit topologies and their associated maximum voltage and current stress. Note: $n_1 = n_p$ and $n_2 = n_s$.

power-conversion rating of the half-bridge circuit due to the increased switching voltage. The maximum collector current of the bridge circuits includes the magnetizing current (I_{mag}) associated with the transformer. The electrical ratings of the semiconductor components are typically 1.5 to 2 times the values estimated by Figure 3.2 to provide margin for parasitic effects. Of course, the extra design margin does not come without penalties such as higher conduction losses or higher device capacitance.

Following an analysis presented by Brown [2], Figure 3.3 shows the operational regimes of the buck/boost/flyback, half-bridge, and full-bridge converter topologies. The boundaries indicated in this figure are, of course, not hard limits and are based on factors such as the maximum current rating of the switches. In the present case, the boundaries are set using a peak current of 60A; a typical rating of contemporary discrete bipolar transistors and metal-oxide-semiconductor field-effect transistors (MOSFETs). As one increases the power requirements of the converter, the thermal and electrical stresses are also increased. To attain higher power-conversion levels, more switches are incorporated into the circuit to reduce the stress imparted

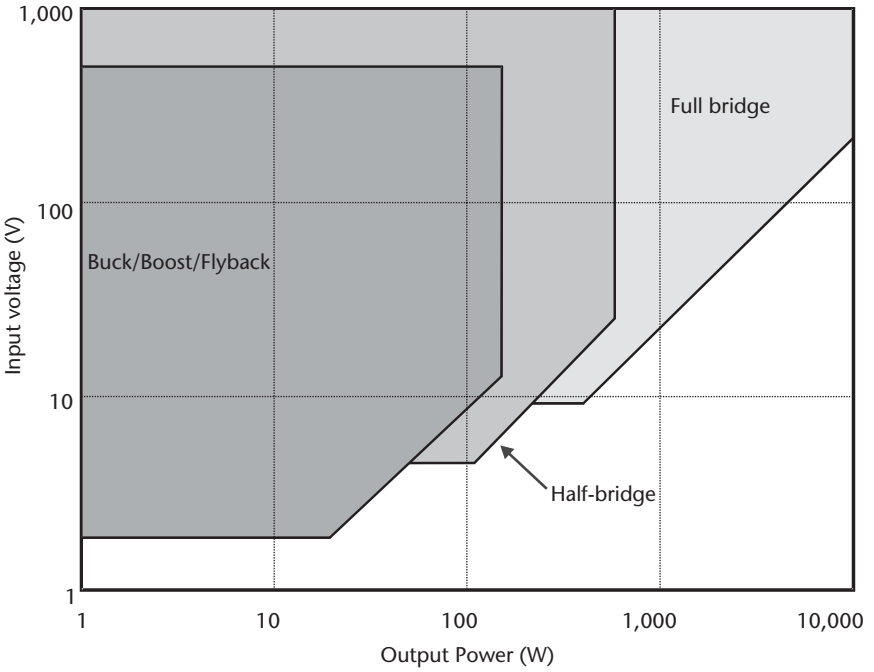


Figure 3.3 Operating regimes of the basic switched-mode power-conversion topologies.

on each switch. The full-bridge converter having the largest number of switches is able to attain the highest power levels.

The idealized waveforms of the buck converter are shown in Figure 3.4. When Q1 is conducting, D1 is reversed-biased and the current flowing through the inductor (I_{L1}) increases to a value of I_{peak} before Q1 is turned off by the control electronics. As Q1 becomes nonconducting, I_{L1} is commuted through the forward-biased D1. If the stored energy in L1 is allowed to fully dissipate (transferred to the load) before Q1 is again turned on, the converter is said to operate in the *discontinuous conduction mode*. In this mode, switching loss is minimized; however, the conduction loss is maximized, and the large ripple current (ΔI_{L1}) gives rise to higher power loss in the output capacitor. If the switch is turned off before a significant portion of the energy stored in the inductor is dissipated, the converter is operated in the *continuous conduction mode*. Here, switching losses are increased and conduction losses are decreased.

In our discussion of SMPC circuits, the switching method has been assumed to be *hard switching*. In hard switching, the current and voltage stresses imposed on the switches and diodes are not considered (or minimized) by the control electronics. The duty cycle or frequency of the system is adjusted solely to maintain the required output voltage, current, or power. Switching losses in these systems can be quite high.

In applications where high power density or thermal management is of prime importance, hard- switched converters are not feasible using conventional Si components. In these cases, resonant or quasi-resonant (also termed "soft-switching") topologies can be used. The electrical resonance is obtained through parasitic

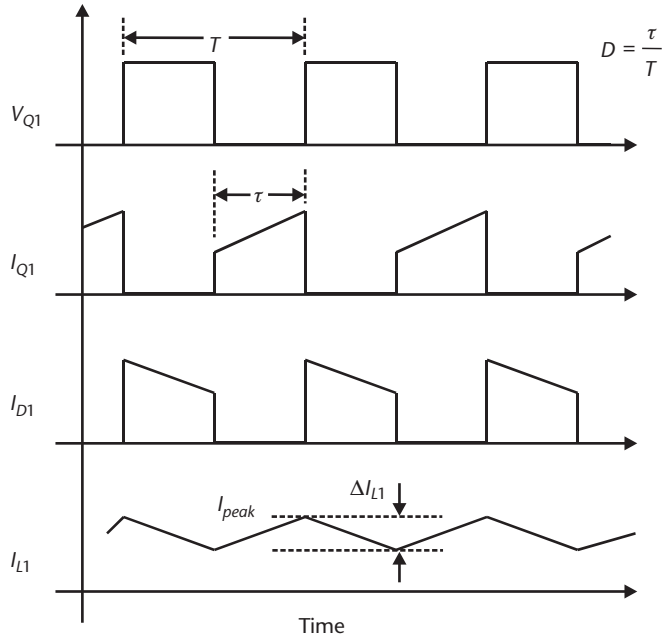


Figure 3.4 Ideal voltage and current waveforms for the buck converter operating in the continuous conduction mode.

inductances and capacitances and lumped inductances and capacitances combined to "tune" the resonant frequency of the circuit to the desired switching frequency. The goal is to provide zero voltage switching (ZVS) or zero current switching (ZCS) through the oscillatory behavior of the circuit.

3.1.2 Silicon Carbide Devices in SMPC Applications

SiC Schottky diodes have just recently been introduced as the first commercially available power components. Not only is the Schottky barrier diode the least complicated device to manufacturer, but it also has the broadest applicability to SMPC circuits. Consider the two roles diodes play in dc-dc converter circuit topologies: current commuting "switch" and output rectifier. In the case of the buck converter, for example, the commutating diode (D1 in Figure 3.2) alternates between the forward- and reverse-biased states as depicted in Figure 3.4. As D1 is switched from the conducting (or forward-biased) to blocking (or reverse-biased) condition, minority charge is removed from the diode junction and a depletion region is established. During this process, the collector-to-emitter voltage of Q1 becomes essentially V_{in} and a large current spike, supplied by the diode's minority charge, is conducted by Q1, resulting in large, transient power dissipation in the transistor during the diode's recovery time [3]. This switching process is one of the dominant sources of power loss in high-frequency, silicon-based SMPC systems and the focus of much research in both circuit and device design.

Silicon diodes used as output rectifiers in SMPC circuits also contribute to power loss. As the diodes switch between the forward- and reverse-biased states, a

large current spike flows in the transformer. The combination of the diode capacitance and transformer's leakage inductance causes severe voltage overshoot and oscillation across the rectifier circuit. This is a significant problem in high-voltage, high-power applications where the use of fast-recovery Si Schottky diodes is not feasible due to the voltage limitation of Si technology. Figure 3.5 shows the operation of a silicon-based, 2-kW full-bridge converter operating at 100 kHz. The top waveforms are the voltage and current across the transformer primary winding and the bottom waveforms are the voltage across the output rectifiers. The 200-V overshoot and ringing across the output rectifier observed in Figure 3.5(a) not only decreases efficiency and exacerbates thermal management but also requires that the diodes have higher reverse-breakdown voltage ratings. We note that the minority carrier lifetime of silicon devices has again caused a problem for the circuit designer. Several circuit modifications have been proposed to reduce the electrical stress on the output rectifiers. These include dissipative and nondissipative snubbers [4], active and passive clamps [5], and synchronous rectifiers. Figure 3.5(b) shows one example of how the oscillation may be eliminated using an active snubber [6]. This circuit uses an additional diode, capacitor, and MOSFET to clamp the voltage across the rectifier diodes and recycle the energy associated with the transformer's leakage inductance back to the load.

Based on the characteristics of the semiconductor devices, it is clear that soft-switching (SS) should have an efficiency advantage over hard-switching (HS), especially at high switching frequencies. Coponet [7] simulated the operation of three SMPC circuits to quantify the efficiencies of HS and SS converters. Figure 3.6 shows the basic circuit topology used in the HS simulations. By adding snubber capacitors in parallel with the free-wheeling diodes (D1-D4), the circuit becomes a ZVS converter, in that the turnoff transition of each switch is slowed by the added capacitance. In a second modification, a capacitor and saturable inductor were added in series with the transformer's primary winding and capacitors are added in parallel with D1 and D2; the circuit becomes a ZVS-ZCS converter. Table 3.1 summarizes the simulation results of the three converter types. Because conduction loss in the switches remains essentially constant over the different topologies, increased efficiency is attributed to the reduction in switching loss. Through the addition of a

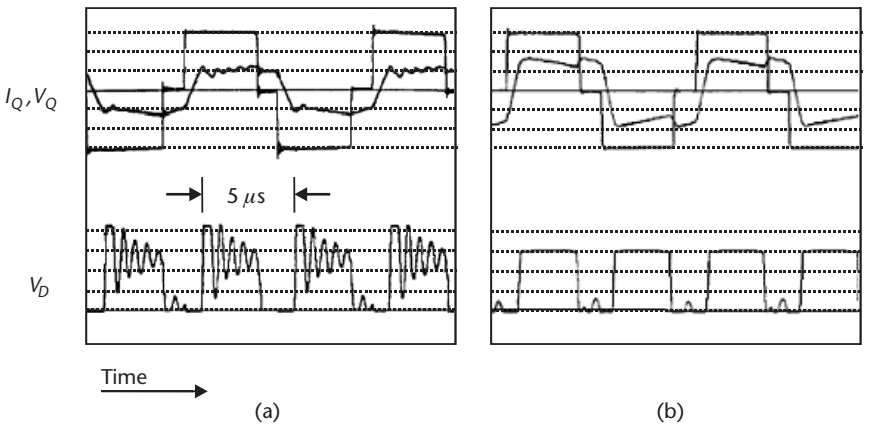


Figure 3.5 Rectifier voltage waveforms of a 2 kW silicon full-bridge converter (a) without and (b) with active snubber circuitry. (*From:* [6]. © 1991 IEEE. Reprinted with permission.)

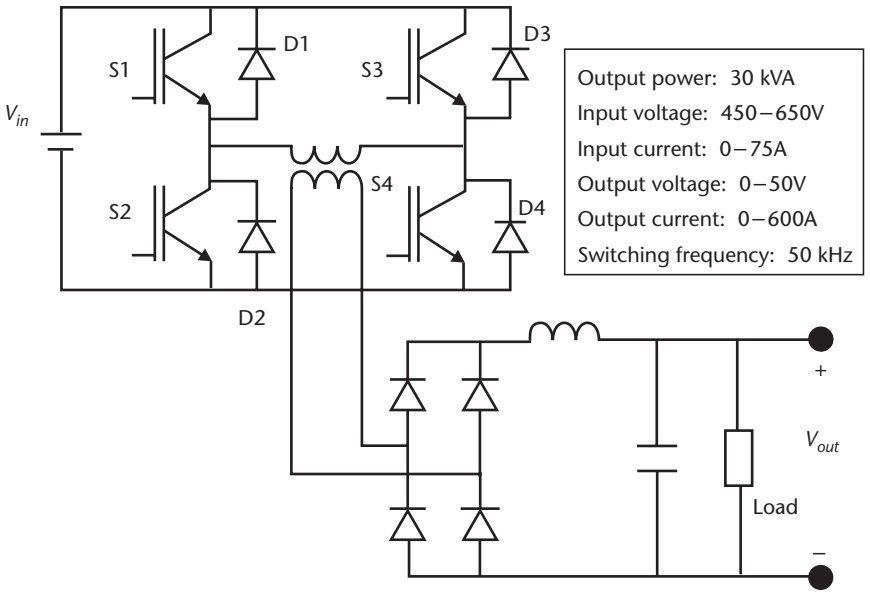


Figure 3.6 Power stage of a full-bridge, dc-dc converter.

handful of components (note that for high power levels these components may occupy a significant volume), the loss in the HS, full-bridge converter has been reduced by 7% or 2,100W!

Richmond [8] has performed a comparison of the loss in HS, Si insulated-gate bipolar transistors (IGBTs) driving an inductive load and using Si and SiC freewheeling diodes. Recall that Si-based bipolar diodes have a significant reverse recovery time that causes energy loss in their companion switch under HS operation and that unipolar Si Schottky diodes are limited to an operating voltage of approximately 200V. SiC Schottky diodes have very low reverse-recovery charge and therefore should obviate the need for snubbers and the more complex SS topologies. Figure 3.7 shows the comparison of the turn-on current characteristic of an Si IGBT (turnoff of the antiparallel diode) using Si and SiC diodes at 25°C and 125°C. As expected, the SiC diode introduces relatively little additional turn-on current to the IGBT and this characteristic is temperature-invariant at least to 125°C. The ultrafast Si diode, on the other hand, doubles the peak switch current at 125°C. Because the IGBT has its own power loss associated with the turnoff tail [9], the additional power loss in the transistor imposed by the antiparallel diode during turn-on will

Table 3.1 Power Loss and Efficiency Comparison of Hard-Switched and Soft-Switched Converter Topologies

	HS	*ZVS*	*ZVS-ZCS*
Power loss in S1 + D1 + S2 + D2	587W (2%)	484W (1.5%)	75W (0.3%)
Power loss in S3 + D3 + S4 + D4	587W (2%)	484W (1.5%)	65W (0.2%)
Total loss	2,350W	1,940W	280W
Efficiency	92%	94%	99%

Source: [7].

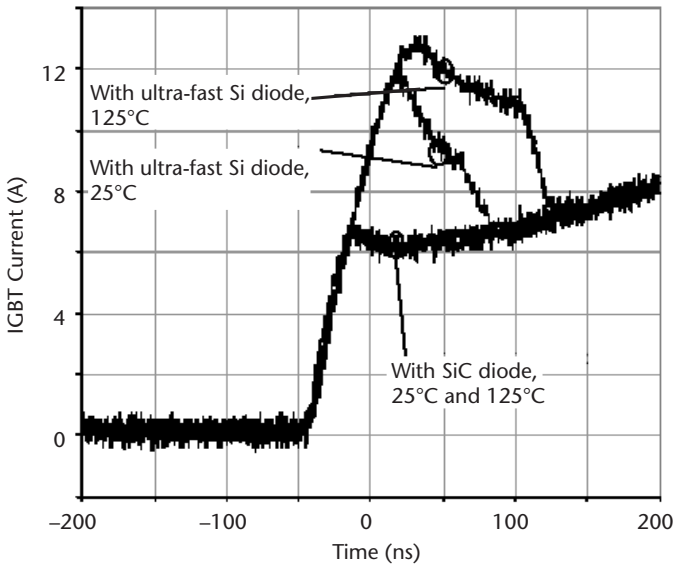


Figure 3.7 Comparison of the turn-on current of an Si IGBT with Si and SiC antiparallel diodes. (*From:* [8]. © 2003 Cree, Inc. Permission granted by Cree, Inc.)

limit the operating frequency of the IGBT in HS applications. Figure 3.8 shows the total power loss in the IGBT as a function of switching frequency and temperature. At 100 kHz and 125°C, the power loss using the Si diode is more than double the value of the loss when a SiC diode is used. Since the SiC diode contributes very little to the total switching loss, the change in the SiC loss curves is due to the temperature dependence of the IGBT's turnoff time.

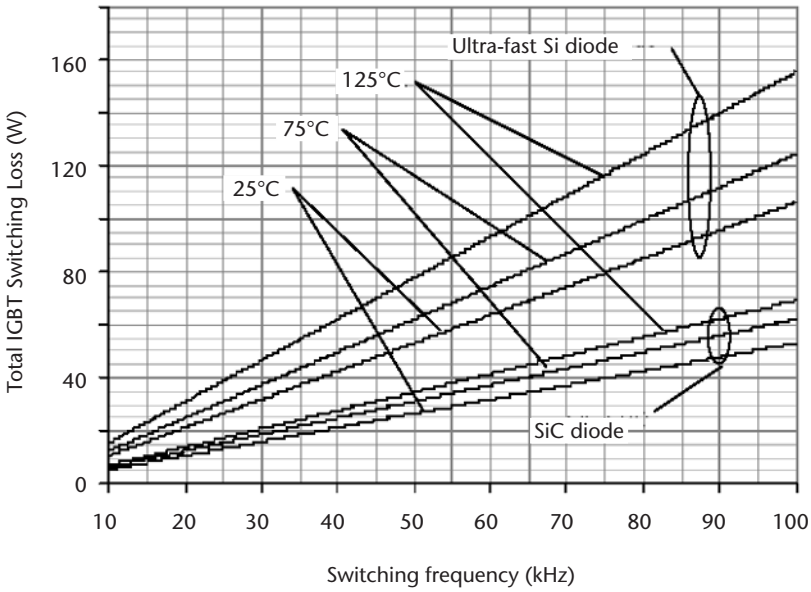


Figure 3.8 Comparison of the power loss in an Si IGBT with Si and SiC antiparallel diodes. (*From:* [8]. © 2003 Cree, Inc. Permission granted by Cree, Inc.)

Based on the previous presentation of the topologies and operation of dc-dc converters, it is clear that stored minority charge in semiconductor devices has a significant impact on their performance. Unfortunately, Si device technology is limited in terms of its reverse recovery performance limits. Depending on voltage rating, the reverse recovery time of Si power diodes may be as low as 25 ns for low breakdown voltage devices (< 200V) [10]. The majority of contemporary power electronics research is focused on circuit techniques and control methods to circumvent the limitations of Si power components. The advent of SiC devices will reduce complexity, or at the very least, provide additional design margin and improved performance.

Until recently, most reported evaluations and analyses of SiC components, as they relate to circuit performance, have been limited to p-*i*-n and Schottky diodes. This has been due to both the complexity of the analyses and availability of stable components. In the previous discussions, it was noted that a variety of techniques have been employed to expand the operating regime of Si-based switching converters by ameliorating the electrical stress. The introduction of commercially available SiC semiconductor components by Infineon and Cree have raised the question of how SiC technology will impact the next generation of switching power circuits.

Hefner et al. [11] performed a comparison of a 600V ultra-fast recovery diode (Si) and a 1,500V, merged p-*i*-n Schottky diode (SiC) in a 50-W Cúk converter. This single-switch converter was operated at 100 and 186 kHz and performed a 500-V to 100-V dc-dc conversion. Figure 3.9 shows the measured efficiency as a function of output power for the two diodes. Using Si diodes, the converter operated at efficiencies between 81% and 85% over most of the loading conditions. When configured with SiC diodes, the converter operated at efficiencies between 87% and 89%. An analysis of individual power-loss components revealed that the switch's conduction and turnoff losses did not change when the circuit was configured with SiC diodes. The switch's turn-on loss, however, was reduced from 2.3W to 0.75W.

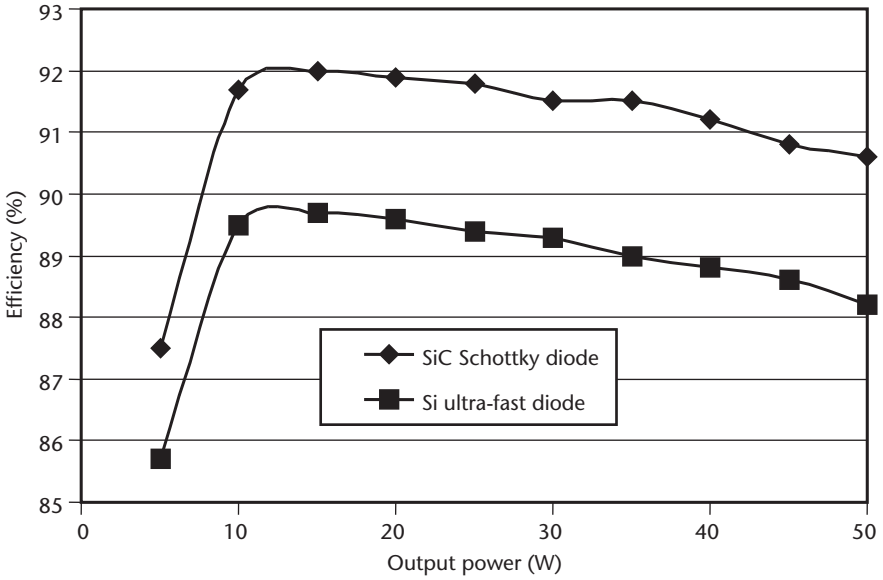
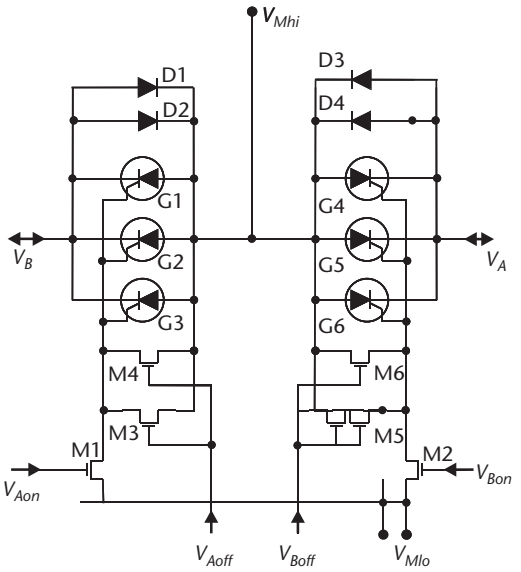


Figure 3.9 Comparison of the conversion efficiency of a Cúk converter using Si and SiC diodes. (*From:* [11]. © 2000 IEEE. Reprinted with permission.)

3.1.3 Other SiC Switches

In addition to unidirectional switches, bidirectional switches also find application in power-conversion and conditioning circuits. One example is the auxiliary resonant commuted pole (ARCP) converter [12]. In this circuit, the familiar four-transistor bridge circuit shown in Figure 3.6 (H-bridge) is augmented by two bidirectional switches (BDS). These auxiliary switches are used as commutation switches and allow for zero-voltage switching of the H-bridge devices. The power loss within the ARCP circuit depends primarily on the values of the resonant inductors and snubber capacitors located across the H-bridge switches. Higher values of snubber capacitance leads to lower turnoff loss in the H-bridge switches but increases the peak current through the BDS that, in turn, leads to higher conduction loss [13]. Usually, high-power switches have a significant turnoff time, which is related to the minority carrier lifetime and requires the use of large-value resonant capacitors at high switching frequencies. In addition to loss considerations, the design of the ACRP circuit is complex as the resonant components determine the maximum switching frequency, *dI/dt*, and *dV/dt* stresses. If one considers the use of SiC components in the ACRP circuit, the design process becomes less complicated due to the very small turnoff times of the switches and diodes.

The authors have developed a hybrid SiC-Si BDS for use in high-temperature power-conversion circuits. The schematic and implementation are shown in Figure 3.10. As high-temperature, high-power SiC MOSFETs are only now becoming available as research-grade components, Si MOSFETs were used to provide voltage control of the SiC gate turnoff thyristors (GTOs). At 150°C, the current rating of the power MOSFETs is de-rated to approximately 10A. The GTOs are asymmetric devices and have a lower reverse-blocking voltage than forward blocking. The antiparallel diodes of the BDS limit the reverse voltage across the GTOs. The BDS was designed to operate a 150°C at a forward current of 17A with a blocking voltage of 400V. The nominal current density was 150 A/cm^2 to keep the die temperature



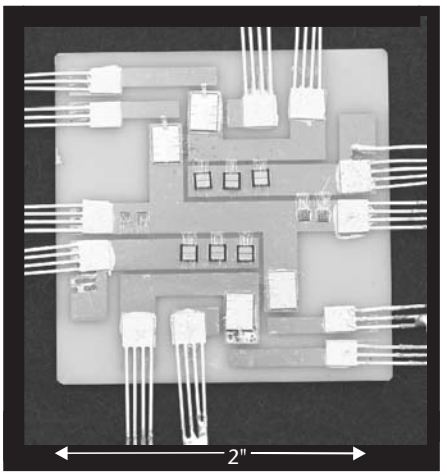


Figure 3.10 Bidirectional switch using SiC gate turnoff thyristors and p-*i*-n diodes.

below 250°C. The antiparallel SiC junction barrier Schottky (JBS) diodes were limited to 125 A/cm^2.

3.1.4 SiC AC-DC Inverter Example

With the advent of regulations aimed at maintaining power quality, traditional off-line power supplies used in high-volume markets such as telecommunications and consumer electronics are required to have a power factor (PF) near unity. The PF is defined as the ratio of the total active power to the total apparent power. Any significant deviation from a unity PF causes phase displacement and/or harmonic distortion on the input power bus. At issue is the design of traditional off-line ac-dc power supplies that use transformers to match voltage requirements and subsequently introduce a large inductive load to the ac line. Again, this large inductance causes the PF to be much less than unity. To maintain power quality, these systems are now required to include a power factor correction (PFC) circuit so that the input current will be controlled to match the input voltage, causing the input to appear resistive (PF=1). A typical PFC circuit is shown in Figure 3.11. The ac line voltage is first rectified then conditioned by the PFC circuit before being passed to the SMPC circuit. Note that the PFC is a boost topology and, in this example, generates a nominal 390 VDC output from the rectified 85 to 265 VAC input. The PFC may be operated in the discontinuous and continuous conduction modes—DCM and CCM, respectively. As previously discussed, DCM operation is not preferred because of performance issues related to high peak currents. On the other hand, the PFC's switching frequency in CCM is limited by the reverse-recovery time of the diode, thereby impacting its size and efficiency. The major SiC device developers regard the PFC application to be a significant near-term market for SiC Schottky diodes due to the combination of high blocking voltage, high thermal conductivity, and near-zero reverse-recovery loss.

Singh [14] and Zverev [15] have evaluated SiC diodes in PFC applications. Figure 3.12 shows a comparison of the voltage and current stresses seen by the PFC's MOSFETs using Si and SiC diodes, respectively. In Figure 3.12(a), two paralleled MOSFETs, an Si diode, and snubber circuit were evaluated, whereas in Figure 3.12(b), the snubber circuit was removed and the Si diode was replaced with a SiC Schottky diode. Using these data and assuming a fixed switching frequency, we

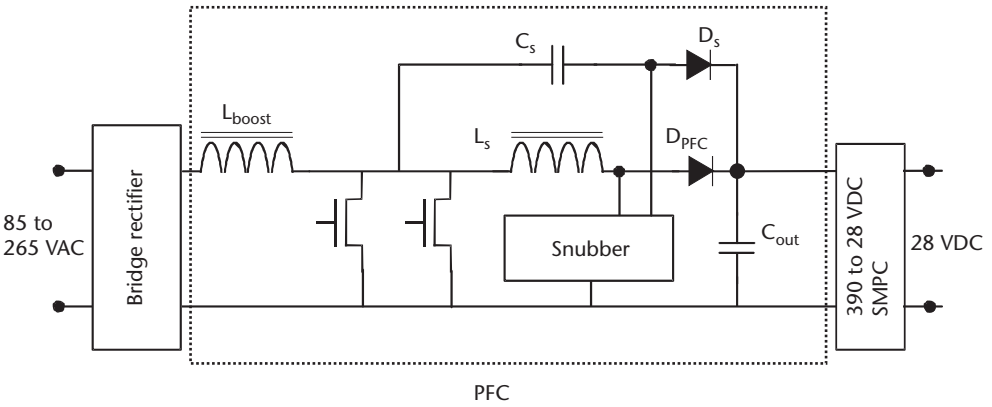


Figure 3.11 Typical power factor correction circuit.

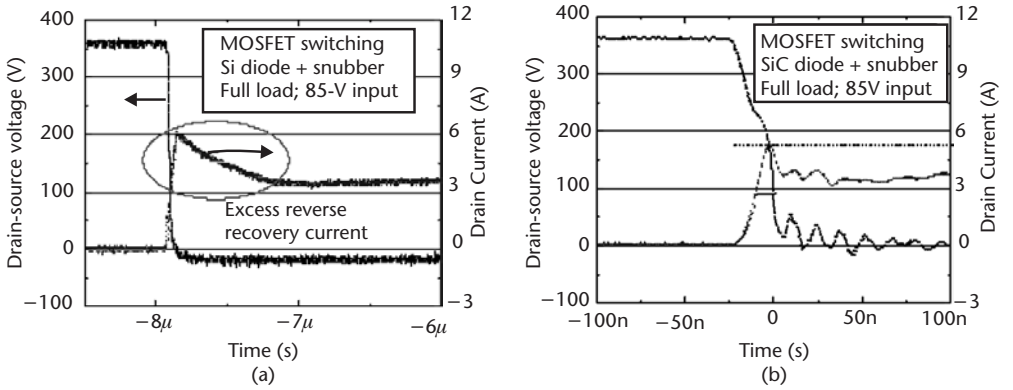


Figure 3.12 Current and voltage for MOSFETs operating in the power factor correction circuit using (a) Si diodes and snubber circuit and (b) SiC diodes only. (*From:* [14]. © 2002 Cree, Inc. Reprinted with permission.)

estimate that the Si diodes and snubber circuit double the switching power loss dissipated in the MOSFETs relative to the SiC diode case.

3.2 DC-AC Power Conversion

Power inverters are a key application in modern electronics industries mainly due to the need for synthesized ac power sources. Variable speed motor drives and uninterruptible power supplies are two primary applications for inverters. SiC represents an enabling technology that has the potential of placing the power-conversion electronics in areas of extreme temperature. This is especially true in military traction applications, hybrid electric vehicles, and avionics systems. Power conversion using SiC solves several problems faced in present-day IGBT and MOSFET-based inverter designs. Specifically, SiC diodes have been demonstrated to reduce the magnitude and duration of the reverse-recovery process. Therefore, inverters built using SiC components promise improved efficiency and flexibility in high-temperature applications.

3.2.1 DC-AC Power Inverter

A simplified schematic of the switching section of a three-phase inverter is given in Figure 3.13. The circuit consists of three half-bridge subcircuits each composed of two switches (*S*) and two antiparallel diodes (*D*). In each leg (A, B, or C), only one switch (e.g., S_1 or S_2) is active at any given time and the output of each half-bridge, V_{AN}, for example, depends only on the input bus voltage (V_I) and the state of the switches. When driving inductive loads, the antiparallel diodes provide an alternate current path to dissipate stored energy once a switch has been turned off. Electrical stresses in the switches are determined by the voltage and currents provided by the dc source to the load. Because of complementary switching these stresses are shared among the switches and are nearly the same for each switch. Therefore, when one switch is on, it carries the full-load current whereas the other switch blocks the full-dc source voltage.

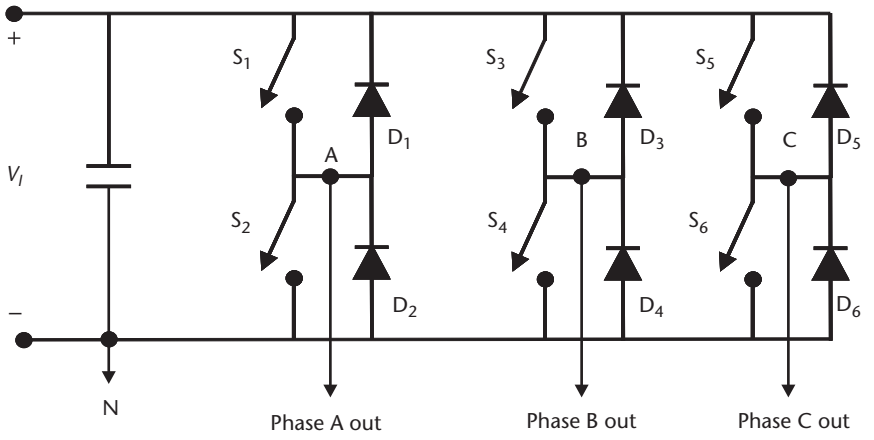


Figure 3.13 Simplified three-phase, full-bridge dc-ac inverter circuit.

The advantage of using SiC components is twofold: reduced switching losses and higher operating temperatures. The reduction in switching losses allows for higher power density or operation at higher switching frequencies. Silicon devices such as IGBTs and MOSFETs continue to have improved switching characteristics but a major impediment is the requirement to have their junction temperature maintained below 150°C to meet reliability standards.

3.2.2 Inverter Control Techniques

Sine-triangle or space vector modulation control techniques are often employed to produce an alternating current from a dc bus. In the first case, the sine wave is approximated by comparing a high-frequency triangular wave to the desired low-frequency sine wave. The resultant waveform is a pulse-width modulated (PWM) control signal that is applied to the upper switch and its complement to the lower switch of a phase leg. To generate three-phase outputs, three low-frequency sine waves (displaced by 120°) are used to generate the six PWM control signals. Complementary operation ensures that the two switches in each leg never conduct simultaneously. High-power inverters typically use switch modules that incorporate multiple IGBTs or MOSFETs connected by many paralleled wire bonds or through low-inductance power planes such as a laminated bus bar. Because the parasitic inductance connecting the switches is quite low, high currents will flow if switches within a phase leg are conducting at the same time. This is called a diametric fault and it is remedied by using carefully designed timing circuits to account for the non-ideal response of the semiconductor devices. To accommodate incomplete turnoff due to minority carrier lifetime, such as that found in IGBTs, a small time delay (dead time) is inserted in the switching cycle. In IGBTs the incomplete turnoff is referred to as the current tail [16]. A consequence of adding dead time is to force either of the two free-wheeling diodes in each phase leg to turn on. This action creates an opportunity for the diode to conduct the full-load current until the next switch is turned on.

When the next switch in the timing sequence is turned on, it must conduct the reverse-recovery current of the diode. As in the case of dc-dc converters, the diode reverse-recovery process usually causes large current to flow, not only because reverse-recovery times can last hundreds of nanoseconds, but also because of the low-inductance power planes. Figure 3.14 shows the reverse-recovery characteristics of a silicon fast-recovery epitaxial diode (FRED) and a SiC diode. It is clear from this figure that the SiC diode is a far more capable replacement for the typical Si diode due to the lack of recovery current.

The application of semiconductor switches in dc-ac conversion circuits requires that the switches be capable of operating at high current, high voltage, and high frequency. The power level for inverter circuits ranges from several watts for fans up to hundreds of kilowatts for traction systems. There are different types of power semiconductor switches, but the switches can be divided into two major categories: voltage-controlled and current-controlled switches. A voltage-controlled switch such as a MOSFET has a very high gate input impedance, requiring relatively little continuous current. A current-controlled device, such as a bipolar junction transistor (BJT), has low input impedance, requiring higher drive currents.

For low-power applications, the devices of choice are the MOSFET, the IGBT, and the BJT. For applications up to 1 kV, the MOSFET is the device of choice because it is a voltage-control device and has a fast switching speed. For applications ranging in voltage from 1 kV up to 4 kV, the IGBT is most often used. The thyristor and the GTO are used for voltages over 4 kV.

The majority of circuit topologies used for inverter circuits are hard-switched. In hard-switched circuits the device sees the full operating voltage while switching the current; hence the power dissipation is dominated by the switching losses, which increase with increasing switching frequency.

3.2.3 SiC DC-AC Inverter Example

The first report of an all-SiC, three-phase dc-ac inverter was presented by Seshadri et al. [17] in 1999. Although Seshadri's inverter used SiC GTOs and p-*i*-n diodes, it was operated at ambient temperature and at voltage and current levels so low that the authors were unable to "…determine typical switching characteristics of the individual SiC components." From the standpoint of technology development, there exists a need to evaluate SiC technology under relevant circuit stresses.

In 2001, the authors of this chapter developed a 400-W, dc-to-ac inverter using SiC GTOs and p-*i*-n diodes for operation at case temperatures up to 150°C for driving three-phase, inductive loads up to 580W. The inverter circuit was constructed to perform the first characterization of these SiC devices under significant electrical and thermal stresses, investigate the parametric operating space of the SiC devices, and uncover circuit-related failure modes.

As previously noted, the switching devices in this dc-ac inverter are SiC GTOs. This device was designed and fabricated by Cree Inc. to provide 1,200-V forward-blocking voltage and a maximum controllable current density of 500 A/cm^2 or 7A. As these devices are asymmetric, their reverse-blocking voltage is limited to 250V. Note that the control signal for this structure is applied between the gate and anode—unlike many conventional Si GTOs. A detailed description of the Cree

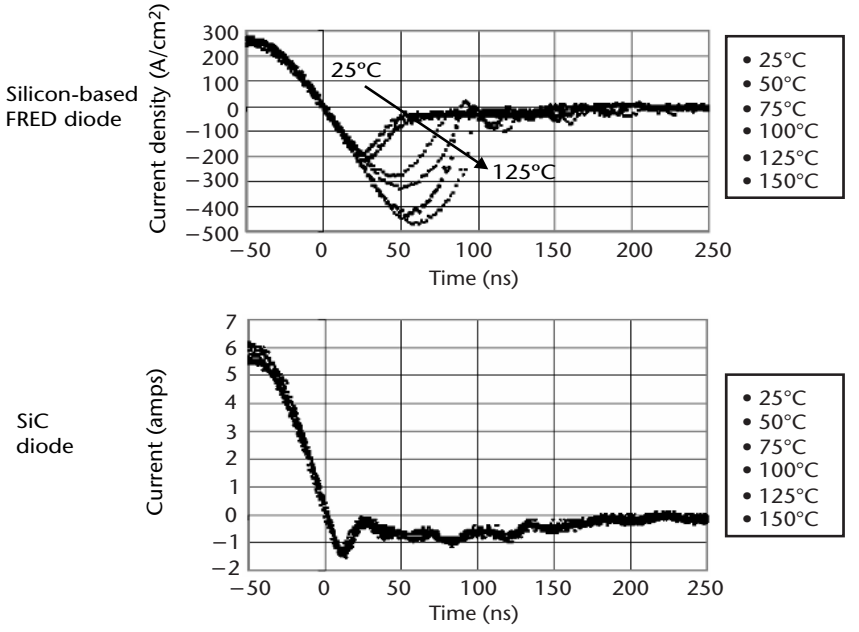


Figure 3.14 Differences between state-of-the-art (a) silicon and (b) silicon-carbide diode reverse recovery.

GTO can be found in [18, 19]. Before being incorporated into the half-bridge circuit, each GTO was screened for the following room-temperature electrical characteristics: (1) anode-cathode forward-blocking voltage of at least 800V with a leakage current of less than 2 μA (150 μA/cm^2), (2) anode-gate forward voltage ($-V_{GA}$) drop of 2.7V at a gate current (I_G) of –20 mA, and (3) anode-gate reverse leakage current of less than 5 μA (300 μA/cm^2) at a V_{GA} of 10V. The turn-on voltage of the p-*i*-n diodes decreased from 3 to 2.6V as the case temperature increased from 25°C to 250°C. The diodes were screened to ensure a forward-blocking voltage of at least 800V with a leakage current of no greater than 5 μA. Further information relating to the Cree SiC p-*i*-n diodes used in this work can be found in [20, 21]. To operate at high voltages, the SiC diodes and GTOs were encapsulated with a low viscosity coating. We found, however, that the encapsulant caused a failure mode in the GTO that was not present in the diode. Before encapsulation, the blocking voltage was measured to be in excess of 800V. After encapsulation, the blocking voltage dropped to below 50V. Based on our characterizations, we hypothesize that the GTO's passivation was degraded by the encapsulation, which in turn provided a leakage current path between the cathode and gate regions. In a study conducted by McCluskey [22] on Si die in plastic encapsulated packages, the principal failure mechanism during high-temperature life testing was the formation of intermetallic species at the die-bond interconnect. Not only did the flame retardants in the epoxy resins cause increased rates of intermetallic formation but they also decomposed at temperatures above 175°C to form corrosive byproducts like methyl bromide and hydrogen bromide that attacked the die. Based on these results, the GTOs used in the inverter circuit were not encapsulated and limited to operating voltages of 600V.

3.2.3.1 SiC DC-AC Inverter Implementation

The block diagram of the SiC inverter is shown in Figure 3.15. The primary dc power supply was varied between 0 and 600V and was "stiffened" with a 500 μF capacitor. A motor control development board was used to generate the PWM pulses for the GTO gate drivers. The PWM signals were generated under open-loop control and had a switching frequency (f_s) of 2 kHz. The output waveforms were synthesized using a 1,024-point look-up table that contained the values of the first quadrant of the sine function. The switching frequency determined the number of points from the table that were used to generate the sinusoidal output, whereas the drive frequency (0 to 60 Hz) was determined by the rate at which the values from the table were output to the drive electronics. Due to the GTO's drive-current requirements, a custom gate-drive circuit was designed to interface the PWM controller with the GTOs. This circuit operated the GTOs using a turnoff gain of 1 and a turn-on gain of 7. The gate-drive circuit was isolated from the PWM driver board by an optocoupler and its output stage consisted of two Si MOS transistors connected in a push-pull configuration. High-voltage isolation of the gate-drive circuit from the bridge circuit was accomplished using dc-dc converters. Two 12-V, 60-W converters were used on each gate-drive circuit to produce the bipolar GTO gate currents. Figure 3.16 shows a schematic of the three-phase, full-bridge power stage consisting of the SiC GTOs and p-*i*-n diodes, turn-on snubbers (SN_{on}), and turnoff snubbers (SN_{off}).

The bridge circuit topology requires that the designer prevent the input power bus from being directly shorted by the switching elements. To avoid the short-circuit condition in the present circuit, two parameters must be properly designed. The first design consideration is the possibility of exceeding the maximum rate of rise of the V_{AK} such that a GTO being turned off is inadvertently latched on. In the forward-blocking state, the center junction of the GTO is reverse-biased and therefore has a

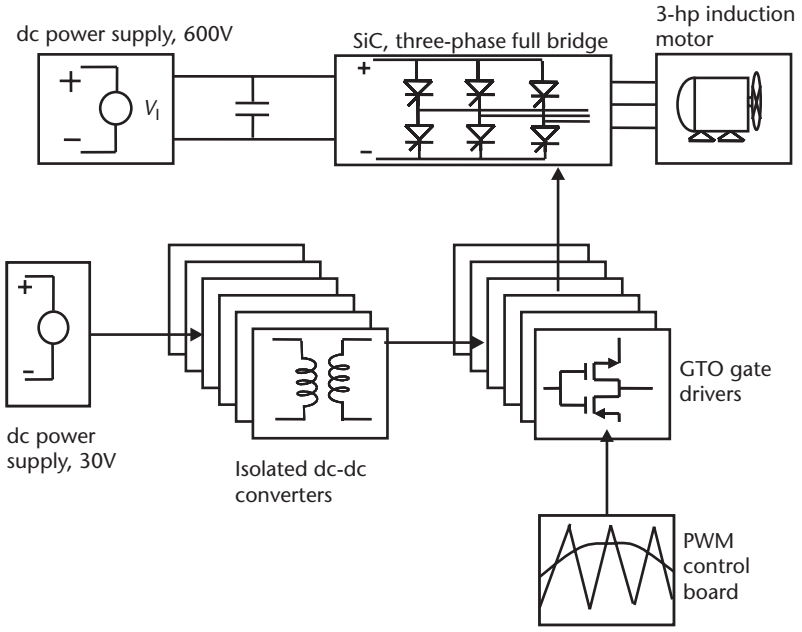
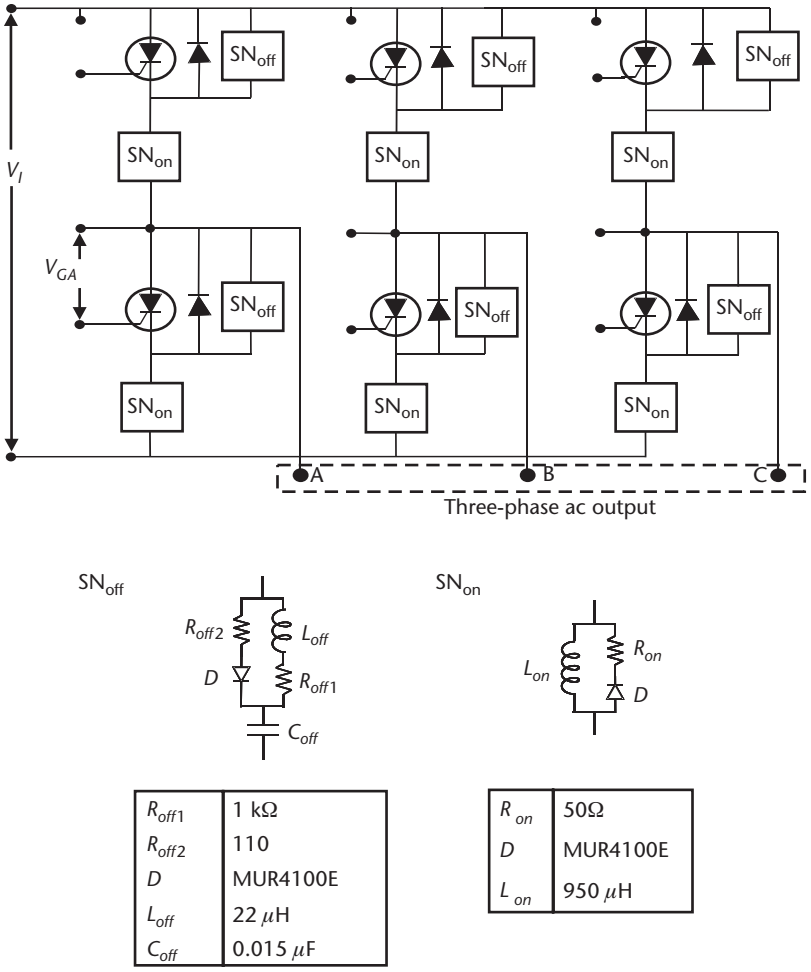


Figure 3.15 Block diagram of a dc-ac inverter.



R_{off1}	1 kΩ
R_{off2}	110
D	MUR4100E
L_{off}	22 μH
C_{off}	0.015 μF

R_{on}	50Ω
D	MUR4100E
L_{on}	950 μH

Figure 3.16 Schematic diagram of a SiC gate turnoff thyristor-based, dc-ac inverter power stage.

small junction capacitance that dominates all other internal capacitances. For a sufficiently large voltage transient across this junction capacitance, a displacement current will be produced that satisfies the conditions for turn-on [23]. To prevent this mode of turn-on, a turnoff snubber circuit was implemented to limit the rise-time of V_{AK}. The turnoff snubber circuit shown in Figure 3.16 was designed to limit the dV_AK/dt to 200 V/s. The turnoff snubber capacitance (C_{off}) is given by

$$C_{off} = I_M t_f / (2V_I) \tag{3.2}$$

where I_M is the maximum current through the GTO and t_f is the anode current's fall time [24]. For a capacitance value greater than C_{off}, the GTO voltage rises more slowly and takes longer than t_f to reach V_I. The value for C_{off} used in the snubber circuit was 0.015 μF. The value of the snubber resistor (R_{off1}) was chosen so that the current through it is 20% of I_m or

$$R_{offl} = V_I / 0.2 I_M \tag{3.3}$$

The value for R_{off1} used in the snubber design is 1 kΩ. For the turnoff snubber to be effective, the minimum on-time of the switch should be greater than the capacitor's discharge time so that the capacitor's voltage can discharge to $0.1V_I$ before the beginning of the next switching cycle; therefore, the minimum on time for the GTO should be

$$t_{on} > \ln(10) R_{off1} C_{off} \tag{3.4}$$

Based on (3.4), the PWM pulse widths were programmed to produce a maximum on-time of 470 μs and a minimum on-time of 30 μs to avoid the possibility of incomplete switching. Due to circuit topology, as the upper GTO is turned on and its V_{AK} decreases, the lower GTO's V_{AK} increases at this same rate. The opposite effect occurs during turnoff. If the upper device's slew rate (dV_{AK}/dt) is allowed to be large during turnoff, there is a possibility that the lower GTO will be inadvertently latched on. The resistor R_{off2} was adjusted to limit the turn-on slew rate. Resistor R_{off2} was added in series with the snubber diode to increase the charging time of C_{off}. Inductor L_{off} limits the peak current through the GTO during turn-on.

The second design consideration is the dead time associated with the PWM control signals. The dead time is determined by the device turnoff time and snubber decay times. Catastrophic GTO failure would occur if both devices in one half-bridge were to conduct simultaneously. The PWM control software was modified to produce a conservative 15-μs dead time.

Exceeding a critical value of dI_K/dt during turn-on presents a reliability consideration for thyristors. The turn-on process begins with the formation of excess-carrier density areas near the gate regions. These regions spread laterally until the entire cross-sectional area of the GTO is filled with excess carriers. If a large current is allowed to flow early in the turn-on process, localized heating could damage or destroy the device. In half-bridge circuits, a turn-on snubber should always be used when a turnoff snubber is used because large transient currents arise from C_{off}. When the upper switch in the half-bridge is turned on, a capacitive charging current from the lower device's snubber capacitor flows through the upper device. The capacitive current causes extra stress on the device; therefore, a turn-on snubber is used to limit the capacitive charging current. The turn-on snubber circuit, also shown in Figure 3.16, was designed to limit the slew rate to 50 A/μs. The snubber inductor L_{on} minimizes transient currents through the GTO; however, a large inductance will cause excessive voltage transients on the GTO at turnoff. When selecting the value of resistor R_{on}, consideration must be taken for the decay time of the inductor. During turnoff, the inductor's current should decay to approximately $0.1I_M$ so that the snubber will be effective during the next turn-on cycle. The equation for the minimum turnoff time (t_{off}) is

$$t_{off} > \ln(10)\, L_{on}/R_{on} \tag{3.5}$$

Both turn-on and turnoff snubber circuits used the fast-recovery silicon diode (model number MUR 4100E).

The demonstration load was a three-phase, 60-Hz, two-pole, 3-hp, 460-V induction motor having a full-load speed of 3,475 rpm and a full load current of 3.8A (rms). The mechanical load for the motor was a direct-drive fan. The power (P_{inv})

delivered to the motor by the inverter, which includes the losses in the motor and the mechanical power delivered to the fan, is given by

$$P_{inv} = \sqrt{3} V_{LL} I_L \cos(\Theta) \tag{3.6}$$

where V_{LL} is the line-to-line voltage, I_L is the line current, and $\cos(\theta)$ is the power factor of the motor. The power factor is a function of load and at full load is 0.89, at three-quarter load is 0.85, at one-half load is 0.76, and at one-quarter load is 0.56.

Based on (3.6) and assuming full load, the inverter would be required to deliver 2,695W of power to the motor (steady-state). Although this steady-state power requirement is within the capability of the GTO, there are several issues that limited the demonstration power level. Based on the motor's design, its starting current can be significantly greater than the steady-state value. For example, the starting current of the demonstration motor is 34A (rms) or 48A (peak) which is an order of magnitude greater than the GTO can control. One method of reducing the starting current is to gradually increase the line voltage and frequency to their full power values. Note, however, that the line frequency must be increased proportionally to the line voltage. Otherwise, the motor's core will saturate and excessive magnetization currents will flow, thereby causing switch failure. In practice, the open-loop, soft-starting technique is plagued by an instability attributed to electromechanical energy resonance [25]. The instability manifests itself as an oscillation in motor speed (and line current) usually occurring at low frequencies and light loads and depends on many system parameters such as f_s, motor geometry, motor core loss, and line voltage. In the present system, we found that the instability occurred at a drive frequency of 30 Hz and a dc bus voltage of 350V. The instability, therefore, required us to limit the demonstration power levels so that the GTOs would not be destroyed.

3.2.3.2 SiC DC-AC Inverter Evaluation

To study operation at elevated temperatures, the case temperatures of the GTOs and SiC diodes were regulated from 50°C to 150°C. During the course of our evaluations, the inverter was operated at 150°C and with peak GTO currents of 2.5A. A maximum peak-output current of 3.5A was obtained at a case temperature of 50°C, frequency of 30 Hz, and dc bus voltage of 350V. To estimate the power delivered by the inverter at 150°C, we begin by calculating the PWM-generated sinusoidal line voltage. The line voltage may be estimated as

$$V_{LL} \approx V_I (0.6 m_a) \tag{3.7}$$

where m_a is the PWM amplitude modulation factor. Using (3.7), a value of 0.8 for m_a, and a bus voltage of 350V, we find V_{LL} to be 168V (rms). (Note that 168V is the line voltage supplied to the motor whereas the SiC components are stressed at the dc bus voltage of 350V.) Using (3.6), a peak line current of 2.5A, and a power factor of 0.8, we estimate P_{inv} to be 400W. A similar calculation for the maximum-achieved power at 50°C gives P_{inv} to be 580W. Figure 3.17 shows the switching waveforms for the lower GTO in the "A" phase of the inverter circuit operated at 50°C case temperature. The upper waveform shows the cathode current peaking at 3.6A with

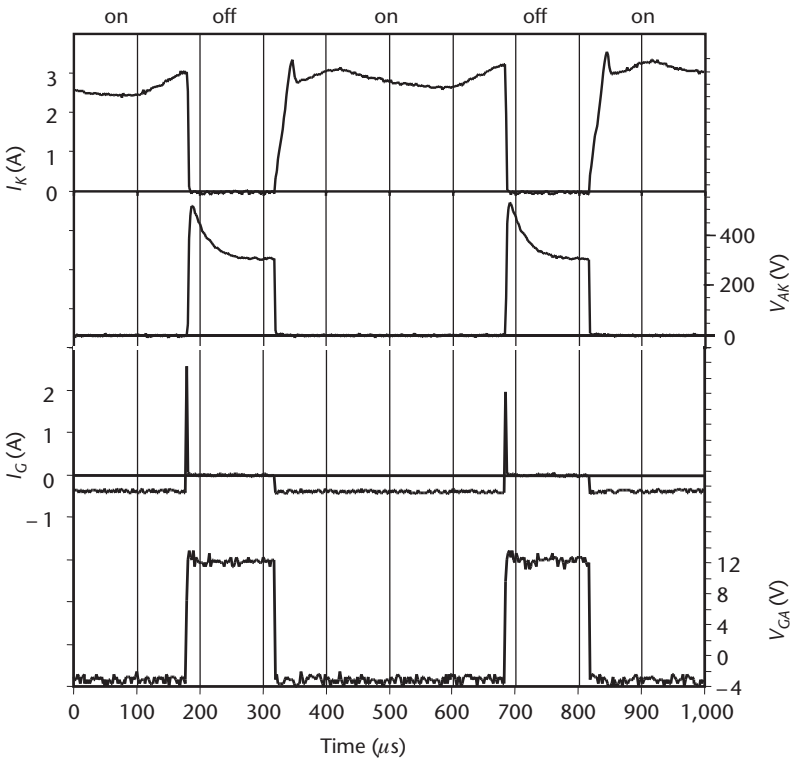


Figure 3.17 Characteristic gate turnoff thyristor waveforms during a portion of the PWM switching sequence.

rising and falling slew-rates of 0.1 and 1.7 A/μs, respectively, and the second waveform shows the corresponding V_{AK}. When the GTO is switched off (e.g., at 180 μs), the voltage across the device rises to a peak value of 550V due to stray inductance in the circuit, and after 125 μs decays to 300V. The turn-on dV_{AK}/dt is –300 V/μs and the turnoff dV_{AK}/dt is 150 V/μs. The lower two waveforms in Figure 3.17 show the gate current (I_G) and gate-anode voltage (V_{GA}). The device turns on with a gate current of –0.48A, which corresponds to a turn-on gain of 7.3. The maximum gate current at turnoff was 3.5A, which corresponds to a turnoff gain of 1. At turn-on, the gate-anode junction is forward-biased at a V_{GA} of –3.2V.

Figure 3.18 shows a series of waveforms characterizing GTO turnoff. Figure 3.18(a) shows V_{GA} along with I_G and the cathode current (I_K). Initially, the GTO was conducting 1A. At 3.5 μs, a turnoff voltage of +12V was applied to the gate. We note a transient gate current of 2.5A even though a turnoff gain of 1 only requires a peak I_G of 1A. However, the gate current is not flowing exclusively in the gate-anode path as evidenced by a transient current (I_{trans}) observed flowing through the GTO's cathode. We complete the analysis of the current path of I_{trans} with the data of Figure 3.18(b). Though not for the same PWM cycle, this data shows that I_{trans} also flows through the antiparallel diode as indicated in Figure 3.19. When the antiparallel diode was removed from the circuit, I_{trans} was also eliminated. We attribute I_{trans} to the diffusion capacitance associated with the junction of the drift and gate layers of the GTO.

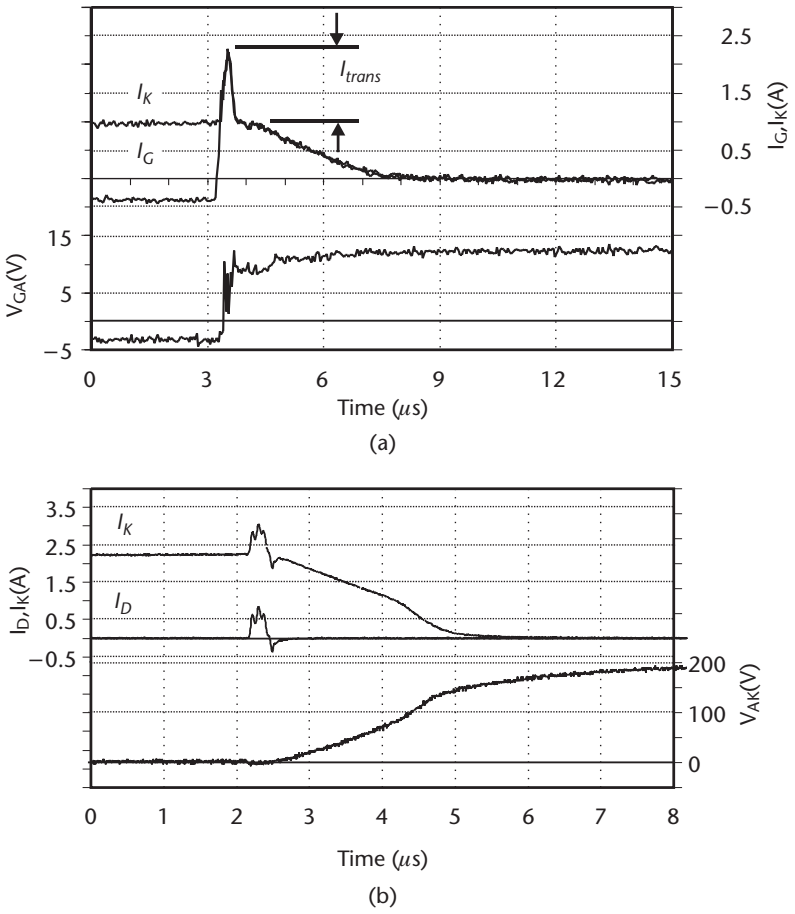


Figure 3.18 Transient current observed in the (a) gate turnoff thyristor and (b) antiparallel diode.

The switching interaction between GTOs and the antiparallel diodes was also investigated. Figure 3.20 shows the following waveforms for a single phase of the inverter circuit: lower GTO cathode current $I_{K(Lower)}$, upper antiparallel diode current ($I_{D(Upper)}$), anode-cathode voltage of the upper GTO ($V_{AK(Upper)}$), and the upper GTO cathode current ($I_{K(Upper)}$). Initially, the upper GTO is blocking 300V, the lower GTO is conducting 3A, and the upper diode is reverse blocking. At 190 μs, the lower GTO is turned off and the upper diode goes from reverse blocking to conducting. The voltage across the upper GTO is now the on-state voltage of the upper diode (3.2V). At 210 μs, the upper GTO is turned on; however, most of the load current continues to flow through the upper diode. At 300 μs, the upper GTO is turned off and I_{trans} can be seen in the $I_{D(Upper)}$ and $I_{K(Upper)}$. At 350 μs, the lower GTO is turned on and I_D is commutated from the upper diode to the lower GTO. Because the snubbers and inductive load limited dI_k/dt, no reverse recovery current was observed in the antiparallel diodes when current was commutated from the diodes to the GTOs.

In our circuit, turnoff power transients dominate the switching losses because the snubber circuits allow the voltage across the device to fall before the current

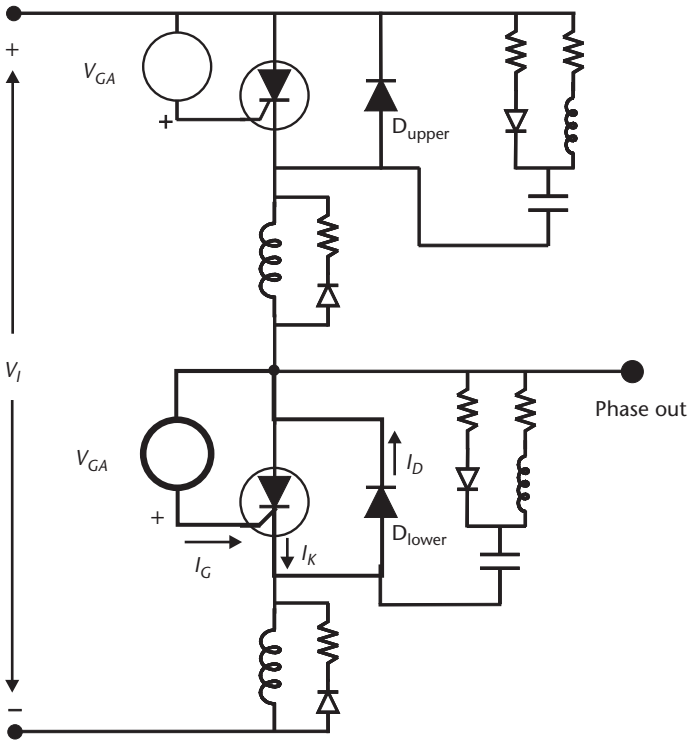


Figure 3.19 Path of the transient current observed during gate turnoff thyristor turnoff.

starts to rise. During the turnoff process, the peak power dissipated in the device is 370W with a pulse width (full width, half-maximum, t_{FWHM}) of 2 μs. The average switching power loss is approximated as

$$P_s \approx V_I I_m t_{FWHM} f_s \tag{3.8}$$

and is found to be approximately 4W. The average conduction power loss can be similarly approximated by

$$P_c \approx V_{on} I_m t_{on} f_s \tag{3.9}$$

where t_{on} is the average, per-cycle on time of the GTO and V_{on} is the on-state V_{AK}. Since this is a PWM system, we take t_{on} to be the average conducting pulse width of 220 μs and find P_c to be 5W. During switching, power is also dissipated in the GTO gate. During turnoff, the peak power dissipated in the gate is 18W with a pulse width of 2 μs. The average conduction power dissipated in the device is 0.7W and the total average power dissipated in the gate is 0.8W.

In this section, we have described a demonstration of an all-SiC dc-ac inverter (using SiC power switches and SiC diodes) operated in excess of 400W and at case temperatures of approximately 150°C. Two factors related to the system's implementation limited the operational power levels of this circuit. First, load instability caused excessive current spikes and GTO failures and was corrected using a closed-

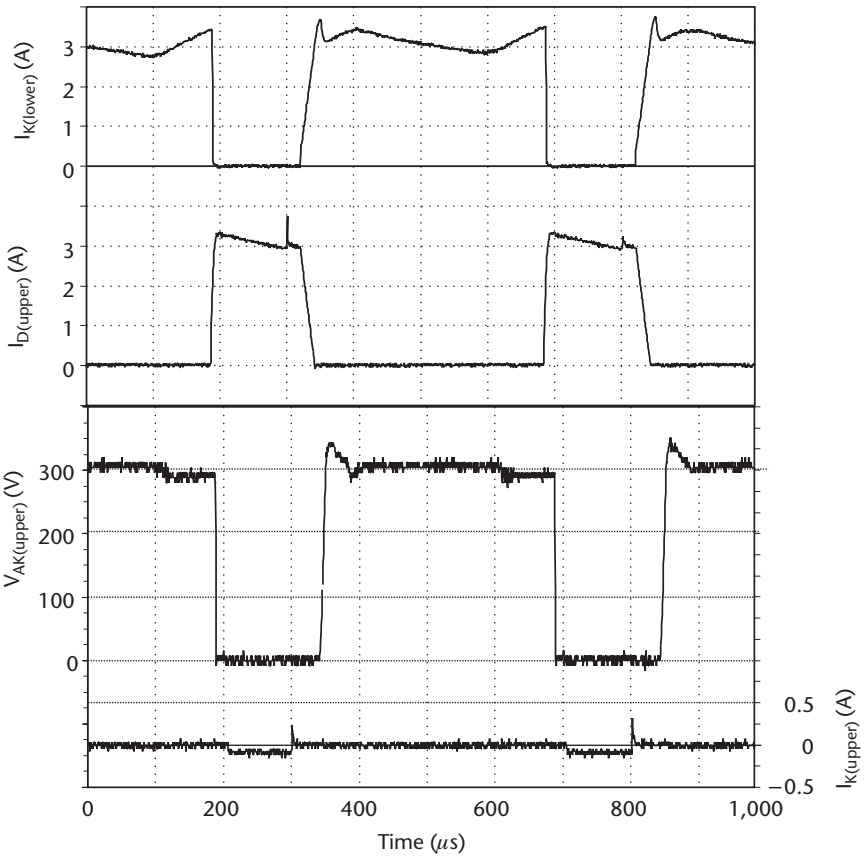


Figure 3.20 Half-bridge inverter switching waveforms.

loop PWM controller. The second limiting factor was a packaging-induced GTO failure. Given that unencapsulated GTOs were operated without this type of failure, higher power operation may be achieved through hermetic packaging of the GTOs.

3.3 Pulsed-Power Applications

Applications such as radar, electric gun, impulse welding, X-ray generation, and fusion energy research require pulse-power systems. The basic premise of pulsed-power systems is to store energy at low power levels over a period of fractions of seconds to many tens of seconds, then switch the stored energy into a load during a very short time period—usually on the order of tens of microseconds. A pulsed-power system usually consists of a prime power, energy storage, power conditioning, an output switch, and load and recovery circuits. The prime power may be a propellant, electric machine, or power supply. Energy storage systems are divided into two categories: kinetic energy storage, which consists of flywheels and rotary flux compulsators, and passive energy storage systems that use capacitors or inductors. Pulse-shaping circuits condition the output pulse as required by the load and

usually contain transformers, RLC pulse-forming networks (PFNs), and/or peaking capacitors.

The output switch is a very important component in the pulsed-power system because the rate at which the stored energy can be delivered to the load is usually limited by the characteristics of the switch. In addition, the reliability of the system is also very dependent on the switch, given the electrical and thermal stresses to which it is subjected. The switch is usually required to conduct peak currents of hundreds of kiloamperes, allowing very fast current rise-times (di/dt) on the order of 10 kA/μs and providing hold-off voltages of tens of kilovolts. Vacuum switches such as thyratrons and spark gaps are commonly used; however, electrode erosion and surface flashover limit their lifetime and reliability. Semiconductor switches have the potential of long lifetimes with fast rise times and high peak currents. Because of its low on-state voltage drop and fast turn-on characteristic, the thyristor is the most widely used solid-state pulse-power switch. In addition to the traditional thyristor, other devices such as the MOS controlled thyristor (MCT), GTO, and the optically triggered thyristor have been investigated for pulsed-power applications.

3.3.1 Thyristor Basics

Although a detailed discussion of the operation of the thyristor is beyond the scope of this book, the basic characteristics of this switch are worth noting, as it claims the highest power-handling capability of all semiconductor switches. Referring to Figure 3.21, the reverse-bias condition, the thyristor performs similarly to a reverse-biased diode. Relatively small currents are conducted through the cathode to the anode until the onset of avalanche breakdown. In the forward-biased condition the thyristor has two stable operating states. The first is a low-current, high-voltage region referred to as the forward-blocking state. The second is the low-voltage, high-current forward-conducting state. In the forward-conducting state, the thyristor can pass currents of several thousand amperes with a forward-voltage drop of only a few volts. Since the thyristor is a latching device, after it is turned on, the current through the device is independent of the gate current and gate voltage.

In pulse-power applications, the thyristor is required to supply energy to the load in a very short period of time, which requires that it provide extremely high-current slew rates. During turn-on, excess carrier density increases near the gate area and then spreads throughout the device. As the excess carriers spread, the anode-to-

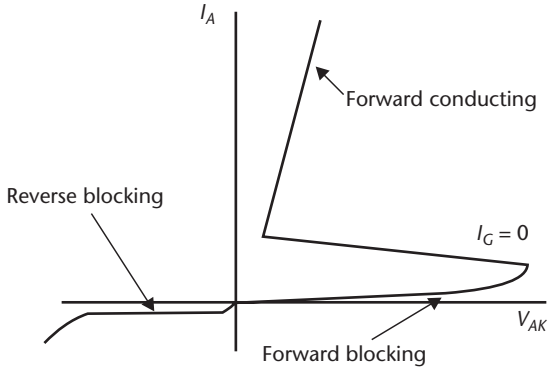


Figure 3.21 Thyristor anode current (I_A) versus anode-to-cathode voltage (V_{AK}) characteristic.

cathode voltage (V_{AK}) decreases. If the anode current (I_A) rises at a rate greater than the time required for the excess carriers to spread laterally across the device, high current will flow in a small area leading to localized heating, which may cause performance degradation or destruction. The rate of rise of current can be increased by increasing the gate current, which, in turn, increases the excess carrier concentration. The turn-on time may also be decreased by optimizing the cathode and gate structures. An interdigitated design increases the gate-to-cathode periphery and decreases the time required for the lateral spread of the conducting region. However, there is a trade-off between the degree of interdigitation and the total cathode area or current rating. Figure 3.22 shows three gate structures that are used in thyristors. The interdigitated structure is used in high-performance switches whereas the clover-leaf and involute designs are used in large-area, high-current devices.

Another parameter that must be taken into account when operating devices in pulsed-power applications is the *action*, defined as $I_A^2 t$, where t is the width of the current pulse. The *life* (N) of the switch is the number of times the device will deliver power to the load before failure and is also an important parameter used to determine the reliability of the pulse-power system. Switch failure is usually related to mechanical factures caused by thermal stresses due to power dissipation in the device at turn-on. Life is predicted using the empirical formula

$$N = \left(\frac{300}{\Delta T}\right)^9 \tag{3.10}$$

where ΔT is the rise in junction temperature due to a single current pulse. Clearly, thermal management and packaging are major factors in determining the life of the switch.

Si power devices are reaching their limits for pulse-power applications. Thyristors are available that have the capability to block voltages up to 6,500V with an average current-carrying capability of 12,000A. GTOs are available that can block voltages up to 6,000V with an average current-carrying capability of up to 1,500A. In single-pulse applications, the peak current rating for a Si thyristor is on the order of 200 kA with a maximum current slew rate of approximately 10 kA/μs. Both industrial and military applications require power switches that can deliver currents of approximately 10^6A with rise times greater than 40 kA/μs.

One approach to achieving higher current capability is to combine several individual switches in large modules. The disadvantages of multidie modules are that the module package may introduce significant inductance, the gate drive circuit may

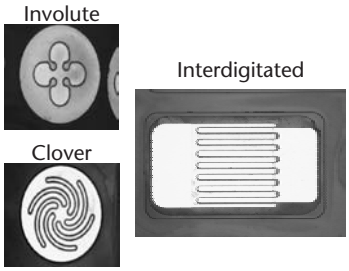


Figure 3.22 Typical thyristor gate structures.

become more complex, and extra snubber circuits may be required to ensure current and voltage sharing between individual switches.

3.3.2 Evaluation of SiC Thyristors for Pulsed-Power Switching

Because of the unique properties of SiC, such as the high electric breakdown strength and high thermal conductivity, SiC should have better performance than Si for pulse-power switching. In pulse-power applications, the fast rise time and high peak currents generate high-power dissipation within the switch. The high thermal conductivity of SiC helps to improve transfer of heat from the device to the package. Researchers have characterized SiC devices for high-temperature and high-voltage applications switching an inductive load [26]. For pulse-power applications, semiconductor devices are stressed at a higher peak current and a faster current rise time than in the continuous power electronics applications.

The authors conducted a study to investigate the performance of SiC GTOs in pulse-power applications. The subject SiC GTOs, designed for high turnoff gain and not optimized for pulse applications, were tested as discharge switches in a low-inductance circuit delivering 2-μs pulses with a maximum switching current of 1.4 kA (94.6 kA/cm^2) and a current rise time of 2.4 kA/μs.

An idealized cross-section of the GTO is shown in Figure 3.23. This device was designed and fabricated by Cree Inc. to provide 1,200V forward-blocking voltage and a maximum controllable current density of 500 A/cm^2 or 7A. As these devices are asymmetric, their reverse-blocking voltage is limited to 250V. The junction termination extension reduces the electric field crowding at the edges of junction J_2, thereby increasing the forward-blocking voltage [27]. Note that the control signal for this device is applied between the gate and anode—unlike many conventional GTOs. This design was optimized for switching and not for high *di/dt* pulse-stress performance. A detailed description of the Cree GTO has been previously published [28]. These SiC GTOs are capable of operating at case temperature up to 150°C [29, 30].

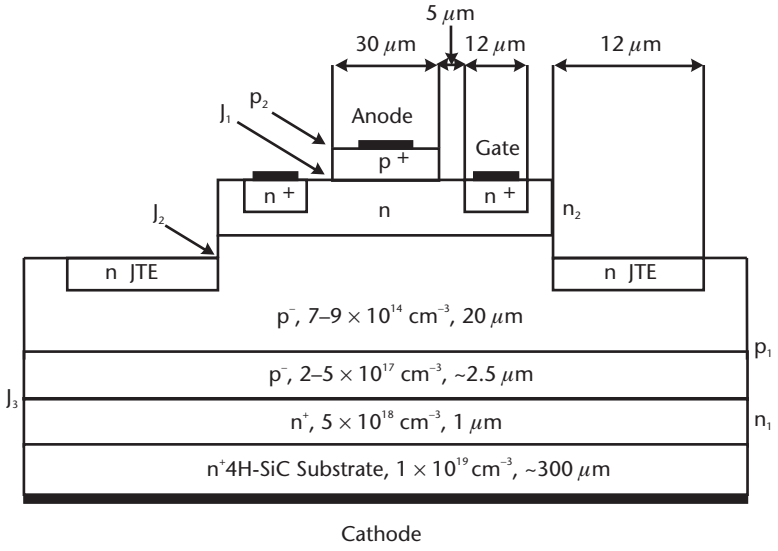


Figure 3.23 4H-SiC asymmetric gate turnoff thyristor structure.

A typical pulsed-power GTO evaluation circuit, presented in Figure 3.24, was used for this experiment. The capacitor (C) is charged through resistor R_C. The GTO is triggered to discharge the stored energy into the load resistor (R_L). The circuit, when charged up to 700V, will produce a peak current of 1.4 kA with a pulse width of 2 μs. The *di/dt* was designed for 3.5 kA/μs and to achieve fast current rise time, all parasitic inductances must be minimized.

Figure 3.25 shows a representative switching voltage and current waveforms at a peak cathode current I_C of 1.4 kA, full pulse width of 2 μs, *di/dt* of 2.36 kA/μs, and anode-to-cathode voltage of 700V. The maximum current density achieved was 95 kA/cm^2. As shown in Figure 3.26, the peak power dissipated in the switch during the switching interval was 240 kW with a pulse width of 1 μs. At the peak current, the device was switched once before failure. As the total number of pulses applied to the GTO increased, a small increase in holding current was observed from 0.22A at a peak current of 800A to 0.35A at a peak current of 1.4 kA; however, the forward voltage remained unchanged.

Forward-blocking voltage was also investigated and the results showed no degradation of the device over the range of peak power. The forward-conduction characteristics of the gate-to-anode diode did not change as the number of shots was increased. However, as shown in Figure 3.27, the reverse-blocking voltage degraded with increasing pulse count.

It can be seen in Figure 3.27, trace D, that the leakage current is about 3 μA at a gate voltage of 15V after the device was stressed at 400V and 800A for 1,000 shots. Trace C shows a slight increase in leakage current to 5 μA after the device was stressed at 500V and 1 kA for 1,000 pulses. The device was then stressed again at 500V and 1 kA for 1,000 additional pulses, as shown in trace B; the leakage current increased to 50 μA at 15V, which indicates that the junction was being damaged. As shown in trace A, after the device was stressed at 1.2 kA for two pulses, the leakage current in the gate was over 40 μA at a gate voltage of 5V, which rendered the device uncontrollable. The results indicated that the gate-to-anode junction was being damaged by the increasing high current stress (power dissipation) on the devices, which led to higher leakage current in the gate-to-anode junction. All the devices failed with high gate leakage when the gate was in reverse blocking. The failure was most likely caused by localized heating of the GTO at turn-on. For high *di/dt* switching, the current through the device is limited to a small turn-on area of the device around the gate, which increases the current density. The high current density causes high power dissipation in the anode-gate area. The high power dissipation in the gate causes damage to the passivation over the gate-to-anode oxide, which leads to the leakage current in the gate-to-anode junction.

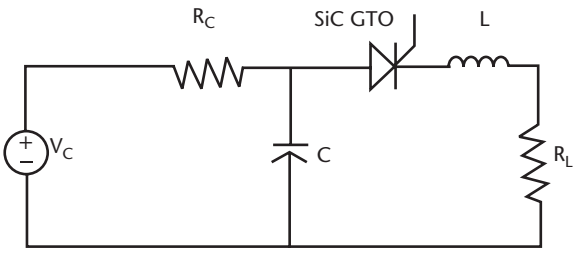


Figure 3.24 Gate turnoff thyristor pulse-testing circuit.

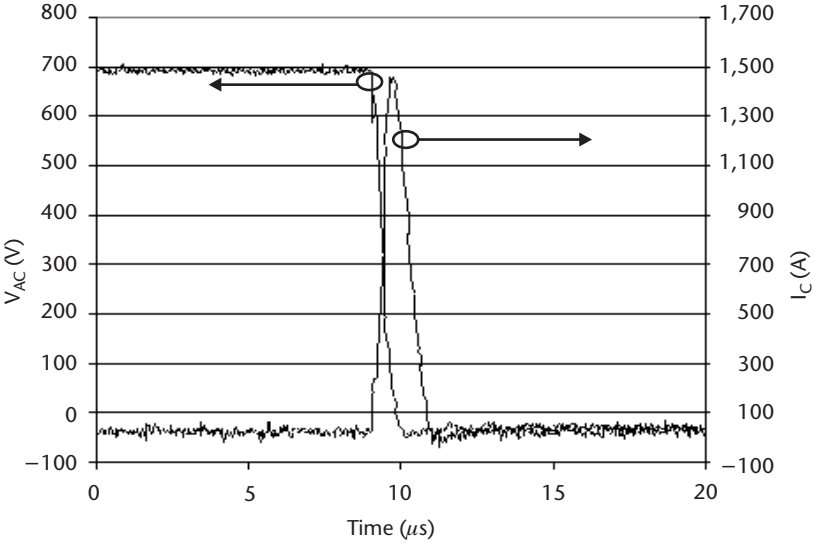


Figure 3.25 Gate turnoff thyristor voltage and current-switching waveforms.

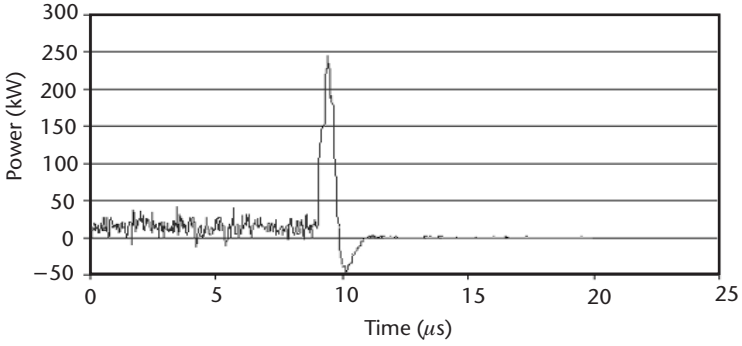


Figure 3.26 Peak power switched by the SiC gate turnoff thyristor.

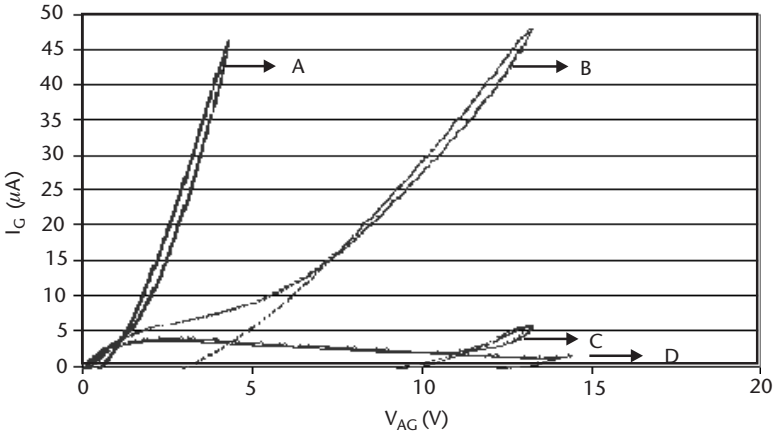


Figure 3.27 Reverse-blocking degradation of a GTO's gate-to-anode junction after accumulating (D) 1,000 pulses at 800A, (C) 1,000 pulses at 500A, (B) 1,000 pulses at 500 A, and (A) two pulses at 1.2 kA.

Figure 3.28 shows a scanning electron microscope (SEM) image of a device after failure with the arrows pointing to the gate and anode fingers. The upper gold plate is the gate metallization and the lower gold plate is the anode metallization. The SEM image shows that damage to the device occurred at the edge of the anode metallization. This suggests that current crowding at the contact edge during the turn-on process gave rise to thermally induced failure.

3.4 Thermal Management and High-Voltage Packaging

One of the salient features of SiC semiconductor devices is their ability to operate at temperatures much higher than Si. This is attributed to the combination of the wider band gap, higher ionization energies of the dopants, and high thermal conductivity. These same properties also allow high-voltage devices to be realized. Although many review papers champion the use of wide bandgap semiconductor technologies, supporting technologies such as thermal management and high-temperature, high-voltage packaging technologies have not been adequately developed to support system development. For example, most SiC devices are currently operated with a junction temperature well below 250°C. This is driven somewhat by the maturity of the technology, but primarily by our ability to effectively remove heat from the die. A second area of concern is that of high-voltage packaging. The majority of discrete Si devices have been designed for voltages less than 2,000V. Wide bandgap devices, however, may operate in excess of 10,000V and at high temperature. This brings to light significant packaging technology issues. Under severe operating conditions, the reliability of these devices has not been thoroughly evaluated and must be considered. In general, we categorize a component's cause of failure to these areas:

1. Immature device technology: high-temperature oxide reliability; high-temperature, high-voltage electromigration; defect formation and transport.
2. High-temperature interconnections: intermetallic formation, high-temperature encapsulation.

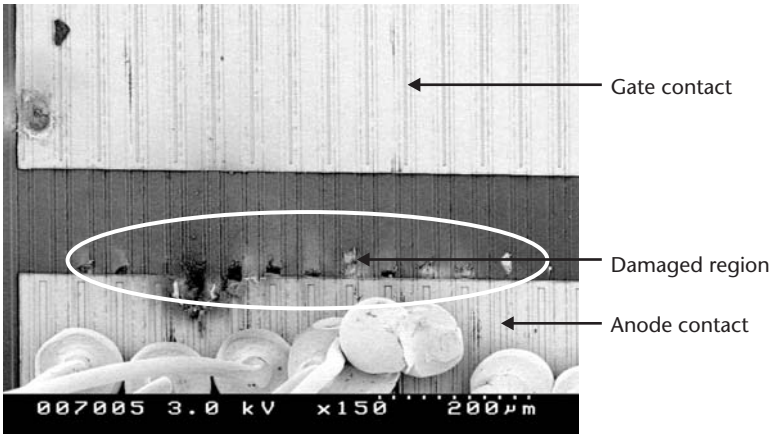


Figure 3.28 Scanning electron microscope image of the SiC gate turnoff thyristor's anode and gate regions after failure.

3. High-temperature packaging: coefficient of thermal expansion matching, high-voltage package design.

The balance of this chapter will provide three examples of the integration of SiC components with a focus on packaging. The first example highlights the design of a high-power, multidie module and its thermal characteristics. The second and third examples provide designs of high-voltage packaging.

3.4.1 Hybrid Si-SiC Half-Bridge Module

A hybrid, Si-SiC half-bridge switch module has been developed under the U.S. Army's Collaborative Technology Alliance by United Defense for a 500 kW electric propulsion drive system for use in 20-ton class vehicles [31]. The module has a 600A, 1,200V continuous duty rating and uses six 100A Si IGBTs connected in parallel. Associated with each IGBT are four paralleled 25-A, 1,200-V SiC JBS diodes. Based on circuit simulations of the hybrid module operating at a switching frequency of 6 kHz, a total power loss of 810W (115W per IGBT and 5W per diode) will be incurred. Note that a three-phase inverter requires six of these switch modules for a total loss of 4.86 kW. Depending on inverter design, additional relevant thermal losses may be present such as that observed in dc link capacitors.

This module, shown in Figure 3.29, incorporates an innovative oil-cooled heat sink, with several key factors making the heat sink a significant advancement in IGBT cooling. First, the IGBT and diode die are bonded directly to a molybdenum substrate that serves as the heat spreader. Molybdenum is used to match the thermal expansion characteristics of the silicon die. By bonding the die directly to the molybdenum plate, the intermediary electrical isolation barriers found in most commercially available IGBT assemblies are removed. Removal of these barriers increases the rate of heat dissipation by eliminating an additional thermal resistance between the die and the cooling fluid. Electrical isolation between modules is achieved at the system level.

Second, the cold-plate underside consists of highly porous media composed of silver-bonded copper spheres that transfer thermal energy through conduction and aid convective heat transfer to the coolant. Heat-transfer capability is greatly

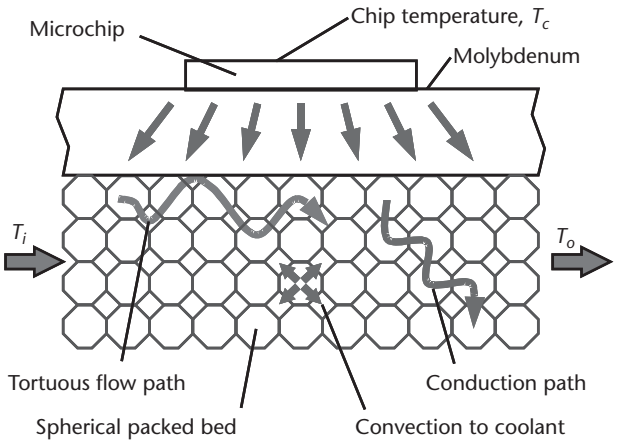


Figure 3.29 Oil-cooled IGBT module heat-transfer mechanisms. (*From:* [31]. © 2003 Army Research Laboratory.)

enhanced due to increased surface area, increased fluid turbulence, and the conductive fin effect at the underside of the molybdenum heat spreader.

The electronic reliability of the module is directly affected by the junction temperatures of the IGBTs and diodes. The silicon IGBT die temperature must be kept below 150°C and the SiC JBS diode should be operated below 200°C due to reverse-leakage current concerns. Limits must be placed on the maximum allowable waste heat production, the minimum required coolant flow rate, and the maximum allowable coolant inlet temperature (T_i). The performance of the heat sink was evaluated through a series of numerical parametric studies in which the following simplifying assumptions were made: (1) the thermal properties (specific heat, density, and thermal conductivities) of the fluid and solid phases are constant and the cooling fluid was well mixed, (2) heat generation was evenly distributed throughout the volume of the die, (3) heat was transferred to the cooling fluid only and all other surfaces were assumed to be adiabatic. Finally, the value of an effective heat-transfer coefficient between the porous packed bed and the fluid stream and the underside of the molybdenum substrate was estimated.

Numerical simulations of the thermal performance of the module were performed using finite element analysis. In the present model, the fluid path is represented by a series of interconnected nodes. Convection processes are modeled as transfer processes between these nodes (or volumes) and surfaces of the geometrical mesh. In this case, a series of analyses based on knowledge of the fluid properties, flow rates, and the relative sizes of the fluid passages and solid phase interconnections led to the value of 3.88 W/cm^2-K for the effective heat-transfer coefficient. Convective heat transfer using this coefficient was used on all of the internal free surfaces of the module.

In the target application, the coolant fluid is Castrol 399 (MIL-PRF-7808) oil at an inlet temperature of 90°C and flowing at 2/3 gpm. As seen in Figure 3.30, the oil enters at the upper left and travels the length of the module from left to right, cooling first the IGBTs and then the associated antiparallel diodes. The oil exits the

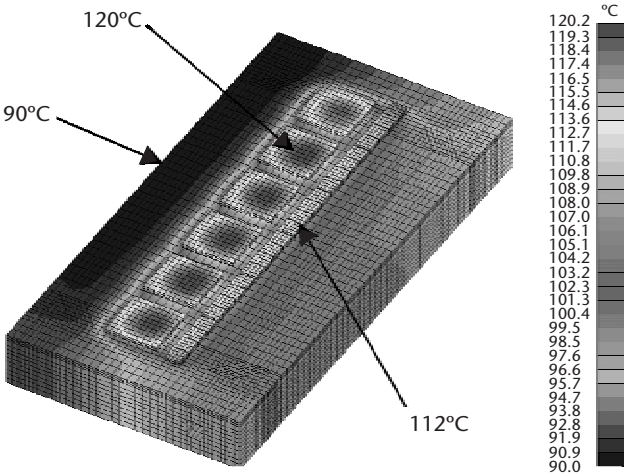


Figure 3.30 Hybrid switch module steady-state temperature profile at 810-W total power dissipation. (*From:* [31]. © 2003 Army Research Laboratory.)

module at the lower right-hand corner where the module temperature is approximately 98°C. As is desirable for adequate current sharing, the temperature profiles are nearly identical for all six IGBTs with a peak temperature of approximately 120°C at the center of each die. The peak temperature of the SiC diode die is approximately 112°C.

To represent the module cooling behavior, it is convenient to define the *heat dissipation capability* as the ratio of total heat generated to the maximum temperature difference experienced by the switch assembly. This ratio can then be plotted as a function of coolant flow rate to establish the operating range and functional safety margins. Reference [31] shows the heat dissipation capability of the heat sink assembly.

Note that as the coolant flow rate is increased at lower rates, the capability of the heat sink to remove thermal energy is enhanced. This effect has diminishing returns at high rates due to the increased dependency on conductive rather than convective heat transfer. At low flow rates and at reduced effective heat-transfer coefficients, the results are somewhat impractical. In these cases, adjacent IGBTs are not maintained at equal temperatures. This condition would generate imbalances in the electrical current sharing, resulting in undesirable switch performance.

In addition to temperature and flow-rate safety margins, the heat dissipation capability diagram can be used to establish a heat generation rate (and hence electrical throughput) operational limit as well. At a coolant flow rate of 2/3 gpm, the heat sink is capable of dissipating 26.8 W/°C. At an inlet oil temperature of 90°C and a maximum chip temperature of 125°C, the heat sink is capable of dissipating approximately 940W or roughly 16% greater thermal energy. As before, the safety margins for coolant inlet temperature and coolant flow rate can be easily calculated. Fluid-based, cold plate assemblies are widely used in high-power applications using semiconductor switches. In high-performance applications where high temperature and/or high-power density are required, custom assemblies like the module described here must be designed and fabricated. As designed, the hybrid module meets the system requirements; however, based on the results of Figure 3.30, there may be a possibility of further optimization. We note that the SiC diode devices are, from a thermal standpoint, being underutilized in that the maximum temperature is only 112°C. In subsequent design iterations, it should be possible to reduce the number of diodes or reduce the area of each diode such that the junction temperature approaches 150°C to 200°C.

3.4.2 Implementation Analysis of a High-Voltage SiC Bridge Rectifier Module

As previously discussed, the use of SiC rectifiers in high-voltage converters is an obvious application. As an example, the 150-kW resonant converter shown in Figure 3.31 produces 10 kV from a 600-V input bus. The secondary has ten 1-kV bridge rectifiers connected in series to obtain the required output voltage. Because the switching frequency is approximately 100 kHz, fast-recovery, high-voltage diodes are essential. In the current design, silicon diodes are specified but SiC diodes are being developed to improve performance. Normally, SiC p-*i*-n diodes would be chosen for this application. However, the phenomenon of forward-voltage drift observed in bipolar SiC devices is enhanced by the thick epitaxial layers needed by

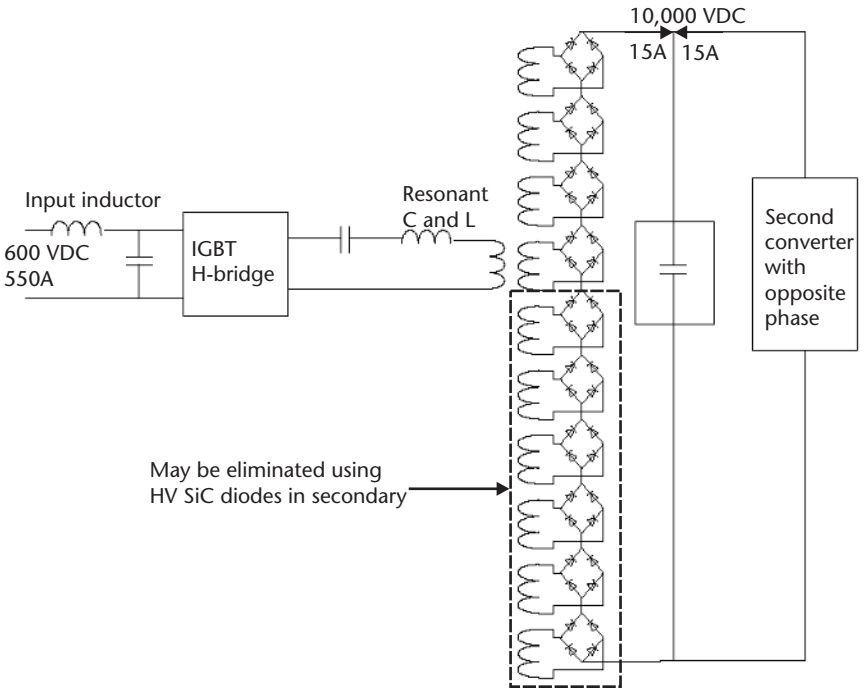


Figure 3.31 Simplified schematic of a 600-V to 10-kV dc-dc converter.

the high-voltage device. One the other hand, the JBS diodes will have higher reverse-bias leakage current at elevated temperatures.

In the following analysis, both p-*i*-n and junction barrier Schottky diodes will be evaluated for use in a 3-kV, 30A SiC bridge rectifier module. Four of these modules will replace the 10 Si diode bridge rectifiers and will reduce system volume and increase efficiency. To optimize the design of the module, we will evaluate the power density at the die level as a function of the number of paralleled diodes in each rectifier leg. A typical value of the heat-transfer coefficient of conventional, power components is 100 W/cm^2. In the present analysis, we have a design limit of 200 W/cm^2 and will determine the number of JBS and p-*i*-n diode needed to meet this goal.

The simulated input current to a Si rectifier leg is shown in Figure 3.32. In the following analysis, the current waveform is approximated by a sinusoidal pulse of the form

$$I(t) = I_{peak} \sin\left(\frac{\pi t}{5 \times 10^{-6}}\right) \quad \text{Amperes} \tag{3.11}$$

where I_{peak} is the peak current in the bridge leg and t is time. To estimate the maximum power dissipation, we set I_{peak} to the sum of the absolute values of the amplitudes of the small and large pulses shown in Figure 3.32. Using the specific on resistance of 15 mΩcm^2 for the p-*i*-n diode and 33 mΩcm^2 for the JBS diode [32], the forward current-voltage characteristics of 3 kV, SiC p-*i*-n, and JBS diodes are approximated by (3.12) and (3.13), respectively.

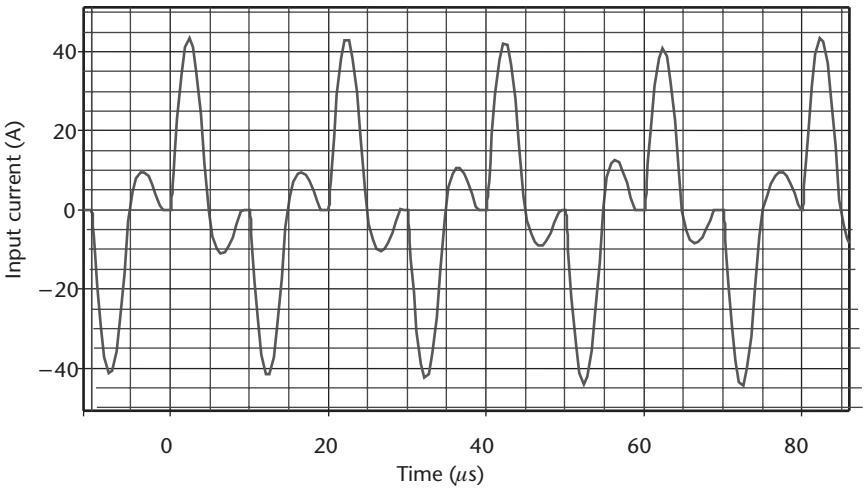


Figure 3.32 Input current waveform to the bridge rectifier. Simulations performed by William Hall, SatCon Applied Technologies, Linthicum, Maryland.

$$V(t) = 3 + 0.2I(t) \quad \text{volts} \tag{3.12}$$

$$V(t) = 0.85 + 0.75I(t) \quad \text{volts} \tag{3.13}$$

The average power dissipated in each diode is calculated by

$$P = \frac{E}{\tau_s} \quad \text{watts} \tag{3.14}$$

where the energy (E) in one pulse is

$$E = \int_0^{5\times10^{-6}} P(t)dt = \int_0^{5\times10^{-6}} I(t)V(t)dt \tag{3.15}$$

and the switching period (τ_s) of the current is 18 μs. Table 3.2 shows the calculated currents and powers in diodes of each rectifier leg as a function of the number of paralleled diodes. In these calculations, power density was calculated using 80% of the 3 mm × 3 mm die area for the p-*i*-n diodes to discount area outside the high-voltage

Table 3.2 Peak and Average Current and Average Power and Power Density of p-*i*-n and JBS Diodes as a Function of the Number of Paralleled Die

Number of Parallel Diodes Per Rectifier Leg	I_{peak} *Per Diode (A)*	I_{avg} *Per Diode (A)*	P_{avg} *Per p-i-n Diode (W)*	P_{avg} *Density Per p-i-n Diode (W/cm²)*	P_{avg} *Per JBS Diode (W)*	P_{avg} *Density Per JBS Diode (W/cm²)*
1	52	9.2	73	1,009	289	6,433
2	26	4.6	25	348	74	1,652
3	17	3.0	**14**	**192**	33	726
4	13	2.3	9.7	135	20	435
5	10	1.8	7.0	97	12	265
6	8.7	1.5	6.7	93	**9.2**	**204**

termination structure and 50% of the same total die area of the JBS diodes to discount the depletion areas that do not contribute to forward conduction. All die were assumed to share current equally.

The diode area was chosen based on the predicted yield and the required number of die. The p-*i*-n implementation requires 12 die per bridge or 96 for the entire system, whereas the JBS implementation requires 24 die per bridge or 192 for the system. The average power loss in the p-*i*-n implementation is estimated to be 1,344W or 0.9% of the output power, and the JBS implementation has a power loss of 1.2%. Clearly, there is a design trade-off that is being driven by the state of SiC technology.

3.4.3 Electrostatic Analysis of a High-Voltage Package for SiC Devices

Recently, there has been a focus on the development of thick epitaxial layers (100 μm) for high-voltage SiC components. Research-grade p-*i*-n diodes and field-effect transistors with 10-kV blocking voltage are being produced now in limited quantities. Packaging these devices, however, is not straightforward and analyses of the die and candidate package are required to ensure the intrinsic SiC blocking voltage is obtained. As an example, the authors performed a series of electrostatic analyses to design a package for a 10-kV SiC p-*i*-n diode. To baseline the development process, an existing package was evaluated experimentally and through finite element modeling. The package technology selected uses a metal base plate on which the die is bonded. A metallized ceramic lead frame is bonded to the base plate and provides both lead and wire bonding surfaces.

As part of the electrostatic analysis, potentials of 10 kV to 15 kV were applied to the metal lead, bond wires, and metallized top surface of the SiC die. In all scenarios, the base plate was maintained at zero potential. The ambient environment was varied among several materials including air, epoxy, Fluorinert, and SF_6 in order to evaluate them as encapsulants. Table 3.3 gives the permittivities and electric field strengths of the package materials and the ambient environments used in the simulations.

To validate the electrostatic finite element analysis procedure, several standard ceramic packages were characterized for high-voltage operation. The results from one of these evaluations are shown in Figure 3.33. The experimental characterization of this package was conducted using a 10-kV power supply and a nitrogen atmosphere. The package failed at 7.8 kV due to arcing between the metal lead and

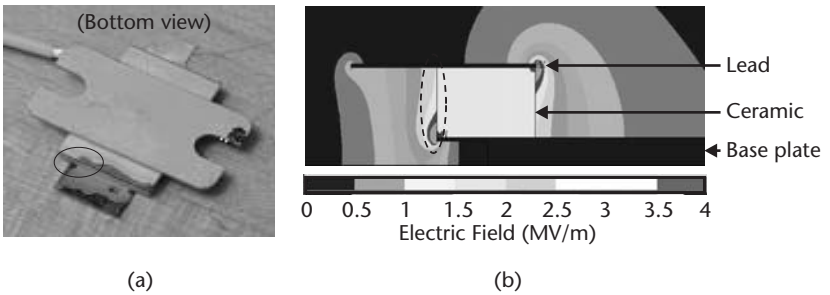


Figure 3.33 Commercial ceramic package: (a) high-voltage failure and (b) electrostatic analysis showing the high-field (3 MV/m) region.

Table 3.3 Material Properties for High-Voltage Package Analyses

Material	*Relative Permittivity*	*Field Strength (MV/m)*
Air	1.0	3
Alumina	9.5	17
Epoxy	4.0	22
Fluorinert	2.0	16
SiC	10.2	300
SF_6	1.0	9

the metallized backside surface of the ceramic ring, as shown in Figure 3.33(a). The corresponding simulation results of Figure 3.33(b) indicate that dielectric breakdown should occur at approximately 8 kV. Breakdown is assumed to occur when a continuous region between two conducting surfaces exceed the critical electric field strength.

An improved high-voltage version of the standard package is shown in Figure 3.34(a). The ceramic body has been extended over the base plate to reduce the electric field intensity and eliminate the breakdown region. In fact, the ceramic body thickness has also been reduced from 0.1 inch to 0.06 inch. The top ceramic ring is not critical in reducing the electric field and serves as a spacer for the package lid.

Unlike the package's exterior regions, the electric fields within the die cavity are too large to be altered significantly by minor changes in the structure. In this case, encapsulants with relatively high field strength (>15 MV/m) are needed for the

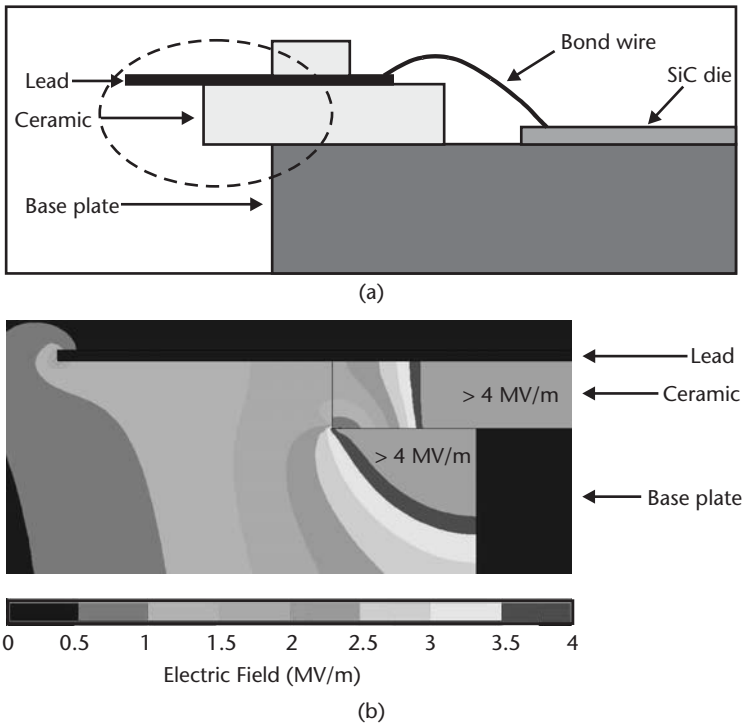


Figure 3.34 (a) Geometry and (b) electrostatic simulation results of the extended-body, high-voltage package.

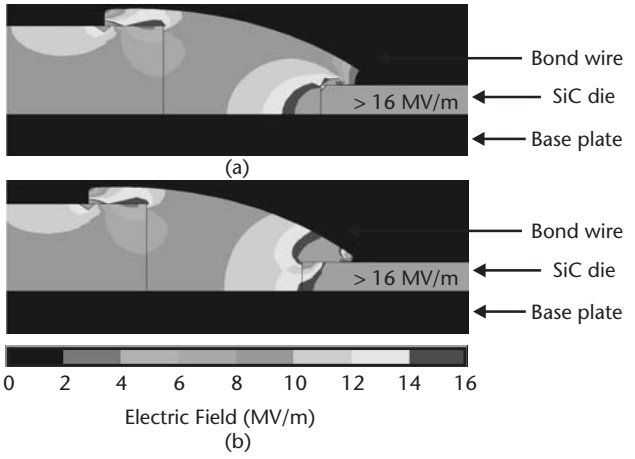


Figure 3.35 Electric field plots showing the performance of Fluorinert under an applied voltage of 15 kV with surface potential terminated (a) 0.2 mm and (b) 0.5 mm from the edge of the die.

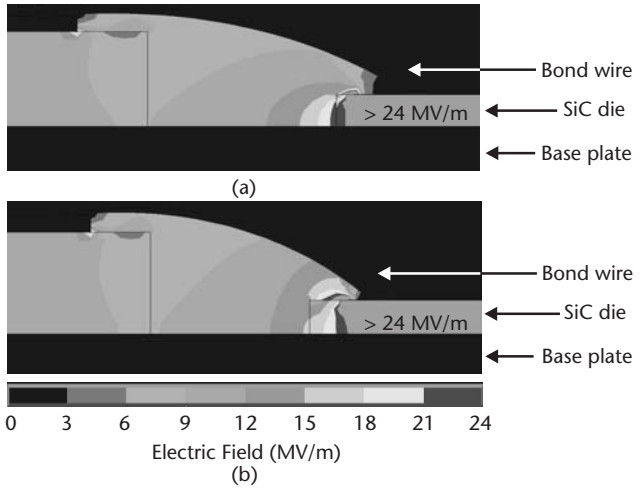


Figure 3.36 Electric field plot showing the performance of the epoxy under an applied voltage of 15 kV with surface potential terminated (a) 0.2 mm and (b) 0.5 mm from the edge of the die.

package to successfully operate at voltages exceeding 10 kV. Figures 3.35 and 3.36 show the electric field near the SiC die using Fluorinert and epoxy, respectively, as encapsulants. Recall that the die's top surface was metallized and the extent of the metal was varied to analyze the electric field as a function of the device's field termination geometry. In Figures 3.35(a) and 3.36(a), the surface potential was terminated 0.2 mm from the edge of the die, whereas in Figures 3.35(b) and 3.36(b) the potential was terminated 0.5 mm from the edge of the die. With Fluorinert's electric field strength of approximately 15 MV/m, the simulation indicates that the potential on the die should be terminated greater than 0.2 mm from the edge to prevent breakdown at 15 kV. At an electric field strength of approximately 22 MV/m, the result indicates that the epoxy provides for a reasonable dielectric breakdown margin at a termination spacing of 0.2 mm.

Figure 3.36(a) shows that when the surface is terminated approximately 0.2 mm from the edge of the die at 15 kV, the epoxy alone can be successfully used as the encapsulant. Fluorinert will also be effective at this voltage if the termination is 0.5 mm or further from the edge of the die. The performance of SF_6 was also investigated at 10 kV. SF_6 is one of the most popular insulating gases with a dielectric breakdown strength of about three times that of air. It is important to note that SF6 is fairly inert at normal temperatures, but it presents hazards at elevated temperatures because it can decompose to form fluorine, which is highly reactive. At a termination spacing of 0.2 mm, SF_6 is not able to protect against breakdown at 10 kV. However, it does provide a reasonable breakdown margin with 0.5-mm termination spacing.

3.5 Summary

This chapter has given several examples of power-conversion applications and the impetus for using SiC technology for improved performance. During the past 2 years, SiC Schottky diodes have appeared in the commercial marketplace and designers have begun to implement new designs using these products. Because the SiC Schottky diode imposes essentially no reverse-recovery loss and may operate to well over 1,000V, the power electronics industry should realize substantial benefit during the next few years. SiC switches are not yet widely available as commercial products; however, a variety of research-grade devices are being demonstrated in "real-world" power-conversion circuits such as inverters for induction motor drives. The technological challenges for SiC switches are the stability of gate oxides, channel mobility, and minority carrier lifetime. Based on known development efforts, we expect that within two years a high-voltage, power SiC FET will be commercially available.

References

[1] Severns, R., "Circuit Reinvention in Power Electronics and Identification of Prior Work," *Proc. 12th IEEE Applied Power Electronics Conference and Exposition 1997*, Vol. 1, February 23–27, 1997, pp. 3–9.

[2] Brown, M., *Practical Switching Power Supply Design*, San Diego, CA: Academic Press, 1990, pp. 18–20.

[3] Erickson, R. W., and D. Maksimovic, *Fundamentals of Power Electronics,* 2nd ed., Norwell, MA: Kluwer Academic Publishers, 2001, pp. 75–76.

[4] Kim, E. -S., and Kim, Y. -H., "A ZVZCS PWM FB DC/DC Converter Using a Modified Energy-Recovery Snubber," *IEEE Trans. on Indust. Elect.*, Vol. 49, No. 5, 2002, pp. 1120–1127.

[5] Dekter, J., N. Machin, and R. Sheehy, "Lossless Active Clamp for Secondary Circuits," *Proc. 20th IEEE Intl. Telecommunications Energy Conf. 1998*, October 4–8, 1998, pp. 386–391.

[6] Sabaté, J. A., et al., "High-Voltage, High-Power, ZVS, Full-Bridge PWM Converter Employing an Active Snubber," *Proc. 6th IEEE Applied Power Electronics Conference and Exposition 1991*, March 10–15, 1991, pp. 158–163.

[7] Caponet, M. C., F. Profumo, and A. Tenconi, "Evaluation of Power Losses in Power Electronic Converters for Industrial Applications: Comparison Among Hard-Switching, ZVS,

and ZVS-ZCS Converters," *Proc. of the Power Conversion Conf. 2002*, April 2–5, 2002, pp. 1073–1077.

[8] Richmond, J., "Hard-Switched Silicon IGBTs: Cut Switching Losses in Half with Silicon Carbide Schottky Diodes," *Cree Inc. Application Note*, CPWR-AN03, 2003.

[9] Mohan, N., T. M. Undeland, and W. P. Robbins, *Power Electronics*, 2nd ed., New York: John Wiley & Sons, 1995, pp. 635–636.

[10] Elasser, A., and P. T. Chow, "Silicon Carbide Benefits and Advantages for Power Electronics Circuits and Systems," *Proc. of the IEEE*, Vol. 90, No. 6, 2002, pp. 969–986.

[11] Hefner, A., et al., "Silicon Carbide Merged PiN Schottky Diode Switching Characteristics and Evaluation for Power Supply Applications," *Conf. Record of the 2000 IEEE Industry Application Conf.*, Vol. 5, October 8–12, 2000, pp. 2948–2954.

[12] Khersonsky, Y., et al., "Evolution of Soft-Switched, High-Frequency, High-Power Isolated DC-DC Converter," *Conf. Record of the 2001 IEEE Industry Application Conf.*, Vol. 3, September 30–October 4, 2001, pp. 1851–1857.

[13] De Doncker, R. W. and J. P. Lyons, "The Auxiliary Resonant Commutated Pole Converter," *Conf. Record of the 1990 IEEE Industry Application Conf.*, Vol. 2, October 7–12, 1990, pp. 1228–1235.

[14] Singh, R., and J. Richmond, "SiC Power Schottky Diodes in Power Factor Correction Circuits," *Cree Inc. Application Note*, CPWR-AN01, 2002.

[15] Zverev, I., "SiC Schottky Diodes Improve Boost Converter Performance," *Power Electronics Technology*, Vol. 29, Issue 3, March 2003, pp. 38–49.

[16] Petterteig, A., J. Lode, and T. M. Undeland, "IGBT Turn-Off Losses for Hard-Switching and with Capacitive Snubbers," *IEEE Industry Applications Society Annual Meeting*, Vol. 2, September 28–October 4, 1991, pp. 1501–1507.

[17] Seshadri, S., et al., "Current Status of SiC Power Switching Devices: Diodes and GTOs," *Mat. Res. Soc Symp. Proc.*, Vol. 572, 1999, pp. 23–32.

[18] Agarwal, A., et al., "2600 V, 12 A, 4H-SiC, Asymmetrical Gate Turn-Off (GTO) Thyristor Development," *Material Science Forum*, Vol. 338–342, 2000, pp. 1387–1390.

[19] Ryu, S. H., et al., "3100 V, Asymmetrical, Gate Turn-Off (GTO) Thyristors in 4H-SiC," *IEEE Electron Device Letters*, Vol. 22, 2001, pp. 127–129.

[20] Singh, R., et al., "4H-SiC Bipolar PiN Diodes with 5.5 kV Blocking Voltage," *Proc. Device Res. Conf.*, 1998, pp. 86–87.

[21] Hefner, A., et al., "SiC Power Diodes Provide Breakthrough Performance for a Wide Range of Applications," *IEEE Trans. Power Electronics*, Vol. 16, 2001, pp. 273–280.

[22] McCluskey, P., et al., "Reliability of Commercial Plastic Encapsulated Microelectronics at Temperatures from 125°C to 300°C," *2000 IEEE Aerospace Conf. Proc.*, Vol. 5, March 18–25, 2000, pp. 445–450.

[23] Blicher, A., *Thyristor Physics*, New York: Springer-Verlag, 1976, pp. 8–11.

[24] Mohan, N., T. Undeland, and W. Robbins, *Power Electronics Converters, Applications, and Design*, New York: John Wiley & Sons, 1995, pp. 613–695.

[25] Ziang, Y. Q., "Instability Compensation of V/Hz PWM Inverter-Fed Induction Motor Drives," *Conference Record of the 1997 IEEE 32nd IAS Annual Meeting*, 1997, pp. 613–620.

[26] Bayne, S. B., et al., "Inductive Switching of 4H-SiC Gate Turn-Off Thyristors," *IEEE Electron Device Letters*, Vol. 23, 2002, pp. 318–320.

[27] Li, X., et al., "Theoretical and Experimental Study of 4H-SiC Junction Edge Termination," *Material Science Forum*, Vol. 338–342, 2000, pp. 1375–1378.

[28] Agarwal, A., et al., "2600 V, 12 A, 4H-SiC, Asymmetrical Gate Turn-Off (GTO) Thyristor Development," *Material Science Forum*, Vol. 338–342, 2000, pp. 1387–1390.

[29] Bayne, S. B., et al., "High Temperature Inductive Switching of SiC GTO and Diode," *Power Modulator Conference and High Voltage Workshop*, Hollywood, CA, June 30–July 3, 2002.

[30] Tipton, C. W., et al., "Half-Bridge Inverter Using 4H-SiC Gate Turn-Off Thyristors," *IEEE Electron Device Letters*, Vol. 23, 2002, pp. 194–196.

[31] Jones, S., and E. Khanishian, "Numerical Thermal Analysis of an Oil-Cooled Hybrid IGBT Switch Module for High-Power Inverter/Converter Applications," *Proc. of the 2003 U.S. Army Collaborative Technology Alliances Conf.—Power and Energy,* April 29–May 1, 2003, pp. 149–153.

[32] Asano, K., et al., "High-Temperature Static and Dynamic Characteristics of 3.7 kV High Voltage 4H-SiC JBS Diode," *Proc. of the 12th Intl. Conf. on Power Semiconductor Devices and ICs*, May 22–25, 2000, pp. 97–100.

CHAPTER 4

Advances in Selective Doping of SiC Via Ion Implantation

A. Hallén, R. Nipoti, S. E. Saddow, S. Rao, and B. G. Svensson

4.1 Introduction

SiC is recognized as one of the prime candidate materials for semiconductor devices operating at high temperatures, high powers and frequencies, and/or in harsh environments. However, to manufacture such devices for commercial use, a processing technology compatible with large-scale industrial production needs to be established. In this context, different key areas have been identified, such as (1) gate dielectrics with low leakage current and low density of interface states, (2) low-resistance ohmic contacts stable at high temperatures, and (3) doping technology. In this chapter, we discuss the last issue, with a focus on selective area doping, but it should be noted that all three areas are closely related. For instance, low-resistance ohmic contacts are strongly dependent on highly doped surface layers with good carrier mobility (i.e., a low concentration of residual defects acting as scattering centers).

SiC can be doped with the same kind of elements used for Si; aluminum and boron are the most common ones for p-type doping, whereas nitrogen, and to some extent phosphorus, are the main ones for n-type doping. The positions of the corresponding acceptor and donor ionization levels in the energy bandgap are given in Table 4.1 for the polytype 4H. It may be noticed that the donor levels are substantially shallower than the acceptor levels, as will be discussed later in more detail. Controlled doping of bulk crystals and epitaxial layers can be performed in-situ during growth using CVD and the concentration of dopants in epitaxial layers is accessible over a wide range [1, 2]. However, for a genuine implementation of SiC devices a planar technology with selective-area doping is required. For Si, such doping can be obtained by ion implantation or thermal diffusion combined with appropriate masking films. For SiC, thermal diffusion is not a viable concept in device processing because of the extremely high temperatures normally required. The high thermal stability of SiC is accompanied by a low atomic mobility and to reach reasonable diffusivities (10^{-13} cm^2/s) temperatures around or in excess of ~1,800°C are needed for most elements. Only light elements with a small atomic radius, like hydrogen, lithium, beryllium, and boron, exhibit a significant diffusion under equilibrium conditions at temperatures below 1,800°C, and here also the level of background doping (Fermi level position) can play a crucial role [3]. Hence, for SiC, ion implantation is very attractive and appears to be the only feasible method to

Table 4.1 Dopant Energy Levels in 4H-SiC

	Hexagonal Site (meV)	*Cubic Site (meV)*
Al	230	230
B	300	300
N	50	100
P	45	100

A range of values for the ionization energies has been reported in the literature and the values given in Table 4.1 represent approximate average ones. For Al and B, no clear distinction has been established between the hexagonal and cubic sites.

accomplish selective-area doping in planar device technology. In fact, in silicon technology selective-area doping is primarily not performed by thermal diffusion but rather by ion implantation because of the restrictions on shallow and abrupt dopant distributions in devices with characteristic dimensions in the deep submicron range.

In principle, ion implantation is ideally suited for introducing dopants in semiconductors because of the possibility to accurately control the dopant concentration and the thickness of the implanted region without any chemical or thermodynamic constraints. However, the major drawback is the generation of damage destroying the crystalline structure of the semiconductor material. The damage can range from point defects caused by single-collision cascades at low ion doses to complete amorphization at high-enough doses. Postimplant annealing is required to restore the crystal structure and electrically activate the implanted dopants by positioning them substitutionally in the lattice. For Si, such annealing processes have been extensively studied and are relatively well understood [4], whereas our knowledge of SiC is severely limited.

SiC is, indeed, a more complicated material than Si, and to understand and control the annealing processes is a major scientific challenge, as illustrated by (but not limited to) the following issues:

1. SiC is a dense and stable material with a short bond length (~1.9Å) and a high binding energy (the atomic density is about twice that of Si). Consequently, intrinsic point defects are anticipated to exhibit a high thermal stability. However, it should be pointed out that partial annealing of implantation-induced defects has recently been shown to take place at temperatures significantly lower than those required for thermal diffusion of dopant atoms [5]. In some cases, defect migration occurs even at (and below) room temperature (RT).
2. In addition to interstitial configurations, implanted atoms can occupy either Si- or C-sites and substitutional incorporation on the correct position to act as shallow dopants is not as straightforward as in Si. Moreover, there are nonequivalent lattice sites of either cubic or hexagonal symmetry in the different polytypes.
3. For the common dopants Al, B, N, and P, high-temperature postimplant annealing (~1,400–1,800°C) is required to reach a significant amount of electrical activation. At such high temperatures, preferential evaporation of Si occurs and the surface morphology deteriorates. Several authors have reported a wave-like surface structure as a result of step-bunching during the annealing

[6, 7]. A poor surface morphology is a major concern in device fabrication and substantial efforts have been made during the last years to resolve this issue. Different concepts have been developed, such as effective encapsulants (primarily AlN) for protection of the SiC surface [8] and annealing in CVD-reactors using Si overpressure [9]. These concepts appear to be quite successful, at least up to 1,700°C, and are reviewed in Section 4.3.1.

4. During recrystallization of amorphous layers polytype transitions can occur (e.g., from 6H-SiC with (0001) orientation to 3C-SiC [10, 11]), which may cause dopant redistribution and deactivation. The polytype transformation is in itself interesting and can be used to obtain unstrained "heterostructures." However, for optimized electrical activation of the dopants during postimplant annealing it appears advantageous to suppress amorphization by implanting at elevated temperatures where the defect annihilation rate ("dynamic annealing") is sufficiently high. On the other hand, using (1–100) and (11–20) oriented SiC, which are less common than (0001) SiC, Satoh et al. [12] recently found indications of epitaxial regrowth of implanted amorphous layers with a high regrowth rate. The rate exceeds that for 3C-SiC from amorphous (0001) oriented samples by two orders of magnitude, suggesting a low postimplant annealing temperature for solid-phase epitaxy and dopant activation. Satoh [12] argues that the epitaxial regrowth for the (1–100) and (11–20) orientations occurs because the atomic stacking sequence is preserved at the amorphous/crystalline interface, whereas it is not for the (0001) orientation.
5. As illustrated in Table 4.1 for 4H-SiC, the shallow donor/acceptor levels of the most common dopant elements are located relatively deep in the energy bandgap (for Al and B, the values are given with respect to the valence band edge, whereas for N and P they refer to the conduction band edge). This holds especially true for the acceptor levels (p-type doping) and, as shown in Figure 4.1, the degree of ionized acceptors (Al and B) amounts to only a few percent (or even less) at RT for dopant concentrations of 10^{18}–10^{20} cm^{-3}. Temperatures above ~500K are typically required to reach an ionized fraction of > 10% and, therefore, operation of SiC-devices containing p-type layers is not ideal at RT. The traditional solution to overcome this obstacle is to introduce a high excess concentration of dopants to compensate for the low ionization. However, this gives rise to low carrier mobility (impurity scattering) and is ultimately limited by the solid solubility. For Al in 4H-SiC and temperatures of 1,700–2,000°C, solid solubility limits in the range of a few times 10^{20} cm^{-3} have been reported [13]. Ideally, an acceptor center with a shallower level position than that of Al (and B) is preferable and recent calculations by Deák et al. [14], based on density-functional theory in the local-density approximation, suggest a $Al_{Si}N_CAl_{Si}$ complex as a promising candidate with good thermal stability. For n-type doping, the donor levels of N and P are sufficiently shallow to allow optimum device operation at RT but a serious limitation may be a relatively low solid solubility. For doping by N, the carrier concentration saturates at ~2×10^{19} cm^{-3} after high-dose implants and high-temperature annealing [15], presumably limited by the solubility of N and formation of N-related precipitates. Hence, it is not

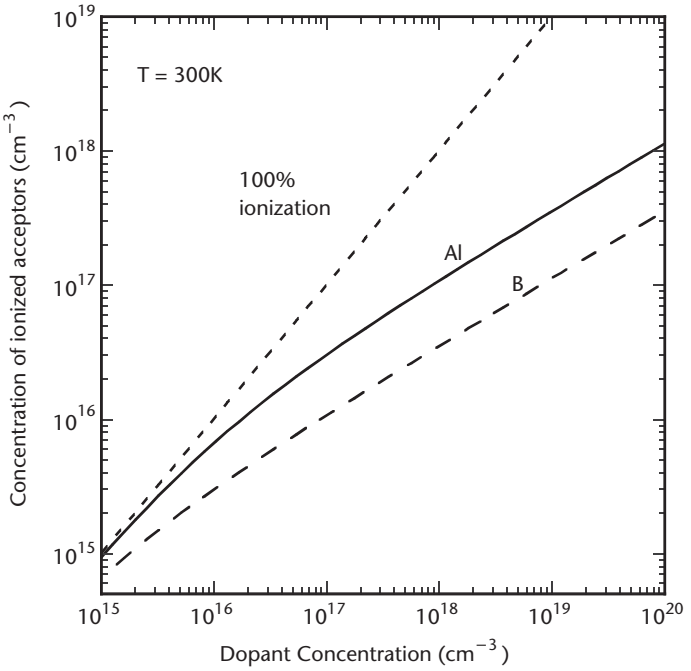


Figure 4.1 Degree of dopant ionization as a function of concentration for boron and aluminum estimated at room temperature. The calculation is based on ionization data from Table 4.1 and an effective hole mass of 1.24 m_e.

straightforward to accomplish highly doped n^+-layers ($\geq 10^{20}$ cm^{-3}) and this issue requires further attention. Moreover, in this context it should also be emphasized that not until recently viable techniques for measuring electrical carrier concentration-versus-depth profiles in the range ~10^{14}–10^{20} cm^{-3} have been demonstrated for SiC; as discussed in Section 4.2.5, scanning spreading resistance microscopy [16] and scanning capacitance microscopy [17] are two promising candidates but some issues still remain regarding the absolute quantification of the carrier concentration values.

6. A concept employed for compound semiconductors to enhance the electrical activation of implanted dopants is coimplantation [18]. The basic idea is to coimplant the dopant element with one target element to promote the activation of shallow acceptors/donors through "site competition." For example, Al (and B) should reside on Si sublattice sites in SiC to act as shallow acceptors and by coimplanting with C, increasing the excess concentration of interstitial C, the probability that Al (and B) is incorporated on the C-sublattice during post-implant annealing is reduced. Interstitial C is anticipated to recombine preferentially with C-vacancies. Conflicting results exist in the literature [19, 20] but several authors have reported substantial improvements by factors up to ~10 for the electrical activation of Al/B when coimplanting with C [20–22]. Hence, the concept is promising, and the best results are obtained using hot coimplants. The atomistic processes for defect recombination and site competition between different elements/defects are, however, not fully elucidated and further work should be pursued to understand and optimize the coimplantation procedure.

7. A characteristic feature of implantation profiles in single crystalline SiC is the pronounced channeling tails and, depending on the crystal orientation, different tilts of the wafers have to be used to minimize the channeling [23]. For 60-keV Al ions in 4H-SiC, channeling along the [11–20] axis yields a maximum penetration depth 45 times larger than the projected range of random implants. In fact, this could be taken advantage of to minimize the generation of damage since for channeled implants a larger fraction of the stopping is electronic and less energy is deposited in elastic (nuclear) collisions, giving rise to atomic displacement. Monte Carlo simulations have predicted that the integral damage for channeled implants of MeV Al ions (3×10^{13} cm^{-2}) into 6H-SiC is reduced by a factor of four compared with random implants, and, perhaps even more important, the maximum concentration of generated defects is lowered by one order of magnitude [24].
8. Until now, most efforts to reveal the nature and evolution of implantation-induced damage in SiC have been devoted to investigate the influence of ion energy, ion mass, fluence (dose), coimplantation, crystal orientation, ion channeling, substrate temperature, and post-implant annealing procedures. Little attention has been paid to the ion flux (dose rate), which is anticipated to be of vital importance. Since the late 1960s, it is known that the damage accumulation in Si and Ge hinges strongly on the ion flux [4]; this was also later demonstrated to hold for GaAs, InP, and GaN. During implantation, annihilation of defects takes place, so-called dynamic annealing, and a competition exists between the rates of defect generation and annihilation. At low-enough fluxes, the annihilation rate can exceed the generation rate and the accumulated defect density may never reach the critical value for amorphization. As schematically illustrated in Figure 4.2, the substrate temperature plays a crucial role for the dynamic annealing because the

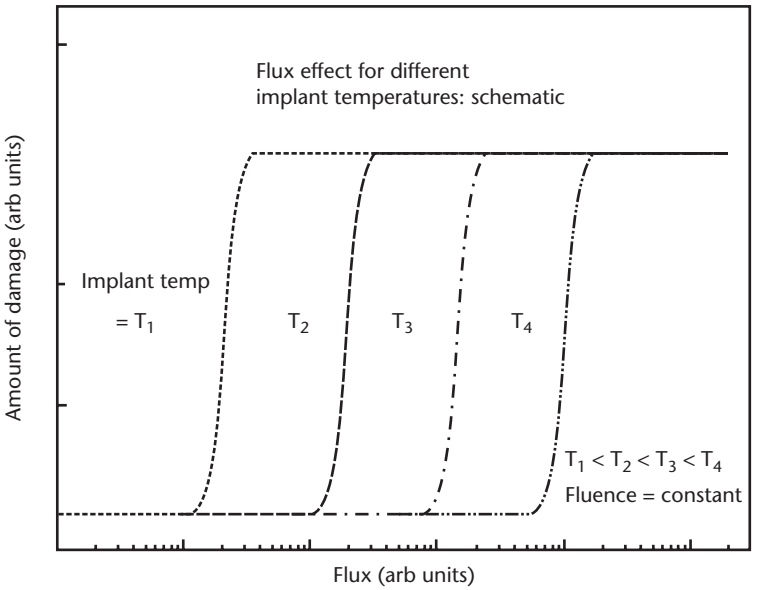


Figure 4.2 Schematic illustration of the flux effect at four different implant temperatures for a constant fluence.

annihilation process(es) is thermally activated. Increasing the substrate temperature implies a higher annihilation rate and hence a higher ion flux can be tolerated while still suppressing amorphization. This is, of course, a simplified view of the temperature dependence for the dynamic annealing since the nature of the resulting/stable defects depends strongly on the implant temperature. Some first reports on the ion flux dependence for implantation into 4H-SiC have recently appeared in the literature [25, 26] but large efforts remain to fully understand and explore the ion flux effect in SiC.

In this chapter, we review the current status of doping of SiC by ion implantation. Section 4.2 examines as-implanted depth profiles with respect to the influence of channeling, ion mass, ion energy, implantation temperature, fluence, flux, and SiC-polytype. Experiments and simulations are compared and the validity of different simulation codes is discussed. Section 4.3 deals with postimplant annealing and reviews different annealing concepts. The influence of diffusion (equilibrium and nonequilibrium) on dopant profiles is discussed, as well as a comprehensive review of defect evolution and electrical activation. Section 4.4 offers conclusions and discusses technology barriers and suggestions for future work.

4.2 As-Implanted Profiles

In this section we will review the current knowledge of ion damage accumulation and chemical profiles in as-implanted single-crystal SiC. We will investigate the effects of the postimplant annealing process in Section 4.3. Results for the 4H- and 6H-SiC polytypes will also be presented.

4.2.1 Diagnostic Techniques

Several analysis techniques are used for the structural and chemical investigation of the as-implanted SiC layers. Among these, SIMS, light ion Rutherford and non-Rutherford backscattering spectrometry in channeling geometry (RBS-C), nuclear reaction analysis (NRA-C) in channeling alignment, and cross-section transmission electron (TEM) are used for depth profile measurements. Studies about the application of the SIMS spectrometry to SiC can be found in [27–29]. The lower detection limit for various n- and p-type doping species are 10^{13} cm^{-2} for B, 10^{17} cm^{-2} for N, and 10^{14} cm^{-2} for Al. In [30–33] the application of the light ion beam analysis techniques to as-implanted SiC to evaluate the amount of displaced atoms is discussed and it is shown that a number of displaced atoms as low as 2% can be observed by RBS-C. The use of the TEM technique in the high-resolution mode allowed the authors of [34, 35] to identify extended defects as small as 2 nm and the onset of vacancy or interstitial condensations in as-implanted 4H-SiC. Among the many others techniques used for the characterization of as-implanted SiC, confocal micro-Raman, positron annihilation spectroscopy (PAS), and deep level transient spectroscopy (DLTS) are also used extensively for ion-implanted SiC, as shown in [36–41]. For the study of the radiation damage due to ion doses in the range 10^{8}–10^{10} cm^{-2}, the high sensitivity of the electrical transport properties with respect to weak

modification of the semiconductor has to be used. Preliminary examples of such a type of analysis are presented in [42] for Si and in [43] for SiC.

4.2.2 Random Implants

4.2.2.1 Basic Considerations

The implantation process of a crystal is said to be "random" when the direction of the ion beam with respect to the crystal is such that the swift ions experience the same amount of energy loss and collisions as they would in a material with the same chemical composition but of amorphous structure. In spite of any attempt to have a random implantation of a crystal, there is always a nonzero probability that some energetic ions are scattered along major axial or planar directions, giving origin to channeled trajectories. In the case of SiC the choice of a random implantation geometry can be even more critical because of the still-poor knowledge about ion channeling phenomena in the different SiC polytypes and because of the lack of a common convention among the material suppliers for giving the SiC crystal orientation with respect to the wafer flat. In fact, the usual convention to identify implantation geometry is to give the tilt and twist angles with respect to the wafer normal and the wafer flat. The tilt angle corresponds to a rotation of the wafer normal with respect to the ion beam direction within the plane of the wafer flat. The twist angle is the angle by which the wafer is rotated around the wafer normal while remaining within its own plane. A correct random implantation of a SiC single crystal can be achieved if all the following constrains are taken into account. The SiC wafers are miss-oriented with respect to the (0001) plane. The amount of this off-angle differs for the 4H-SiC and the 6H-SiC polytypes. The material suppliers give the wafer flat orientation and the off-angle value with ±5° uncertainty. Some preferential directions for axial and planar trajectories in 4H- and 6H-SiC can be unintentionally selected because of the crystal symmetry, as shown in [44, 45]. Because of all this, it must be concluded that in the case of SiC wafers the usual convention to fix tilt and twist angles with respect to the wafer normal and the wafer flat does not guarantee the desired control and reproducibility of the implantation geometry. The laboratories where the real orientation between implantation beam and SiC crystal structure is taken into account are few and all of them process SiC wafers at research level. The fact that the relative orientation between ion beam and SiC crystals often does not minimize the probability of channeled implants explains the large spread of the published data regarding the shape and depth of implanted tails, as demonstrated in [23, 46]. Intentionally channeled implants will be discussed in Section 4.2.3.

4.2.2.2 Damage Profiles After Implantation

This section analyzes the ion damage produced by random implants. Figure 4.3 shows three examples of light ion beam analysis applied to the evaluation of the damage in as-implanted 4H-SiC and 6H-SiC samples. The damage caused by the probing light ions themselves was also investigated. In [47, 48], the upper limit for the MeV He^+ current (i.e., dose rate) and integrated charge (i.e., dose) was experimentally determined and the results presented here all respect those limits. Figure 4.3(a) shows the 2 MeV <0001> He^+ RBS-C spectra of 6H-SiC samples implanted by

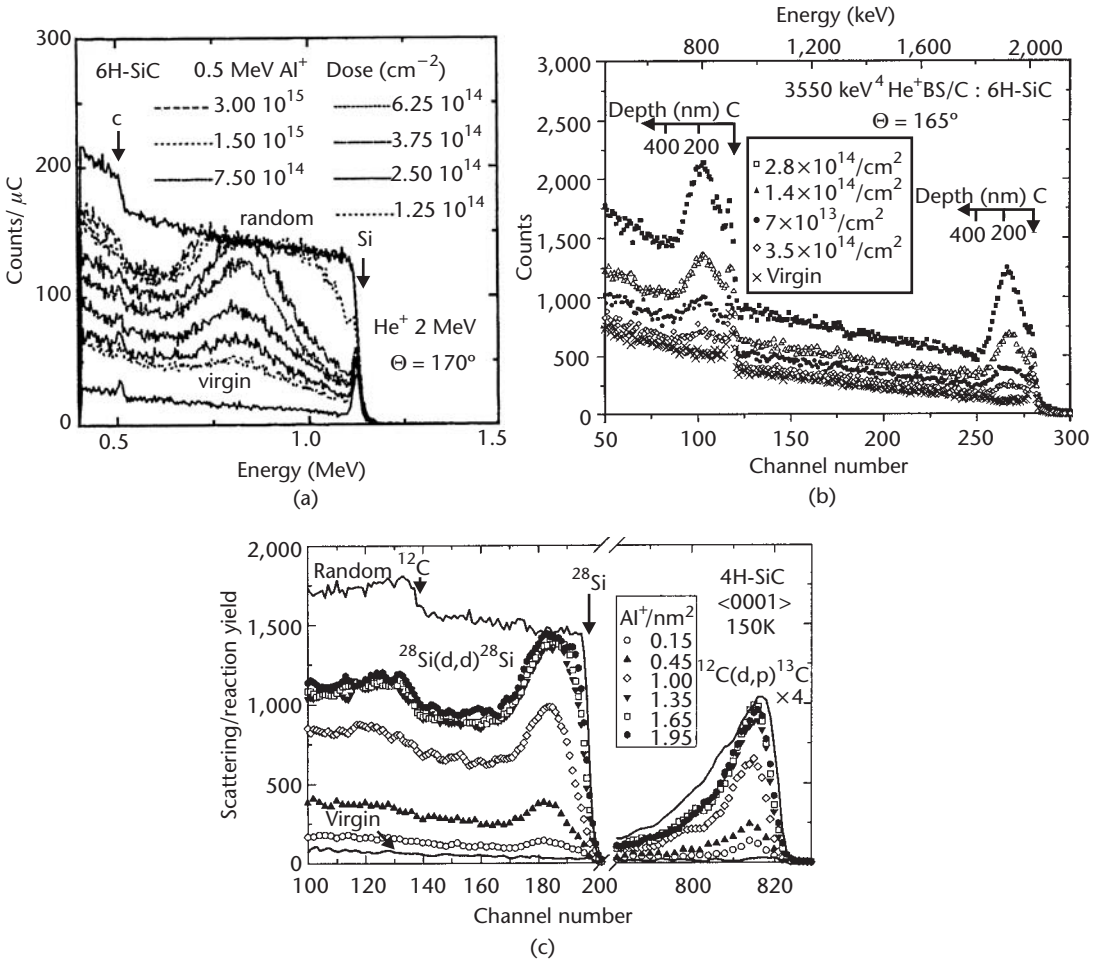


Figure 4.3 Examples of light ion backscattering channeling spectra of SiC crystals that were randomly implanted with a range of parameters such to produce damage levels extended from low values up to the total disorder. (a) 2 MeV He^+ Rutherford backscattering. (*From:* [48]. © 2000 American Institute of Physics. Reprinted with permission.) (b) 3.550 MeV He^+ backscattering. (*From:* [31]. © 2002 Elsevier B.V. Reprinted with permission.) (c) 0.94 MeV D^+ Rutherford backscattering and $^{12}C(d,p)\ ^{13}C$ nuclear reaction. (*From:* [50]. © 2002 Elsevier B.V. Reprinted with permission.)

0.5 MeV Al^+ at various doses. The implantation dose rate and temperature were, respectively, 10^{10} cm^2sec^1 and 27°C. Random implantation was obtained by setting the ion beam direction 8° from the <0001> axis within a plane at 22° from the (10–10) plane. The random and aligned spectra of unimplanted 6H-SiC are also shown for comparison. Two count edges are clearly visible in the random spectrum that corresponds to the edges of the Si and C signal, but the counting yield is significant only for the Si signal. Due to this fact, RBS-C analyses are primarily used to measure the disorder accumulation only in the Si sublattice. To characterize the crystal disorder in the C sublattice the He^+ beam energy can be increased up to an energy region where the elastic collision with the C atoms is resonant (i.e., higher than the Rutherford cross section), as shown in [31, 49]. At 3.55 MeV the He^+ cross section for C is about six times that at 2.0 MeV and the enhanced count statistic for C is sufficient to study the disorder evolution in the C sublattice. Figure 4.3(b) shows 3.55 MeV He^+ backscattering <0001> channeling spectra of 3.5° off-axis 6H-SiC wafers

implanted with 200 keV Al^+ at various doses. The implantation dose rate was about 4×10^{10} $cm^{-2}sec^{-1}$ and implantations took place at RT. The implantation geometry was defined with the ion beam aligned 7° off the sample normal, but no information about the plane containing this tilt rotation was reported. A further approach to increase the count statistic for the C signal is to use nuclear reactions. In particular, the use of 0.94 MeV D^+ produces backscattering channeling spectra where the D^+ RBS-C spectra and the product of the $^{12}C(d,p)^{13}C$ reaction fall in energy windows that do not overlap, as shown in [32, 33]. Further, the statistics of the $^{12}C(d,p)^{13}C$ reaction is such that it permits the study of the disorder evolution in the C sublattice but the depth resolution is too poor to permit the accurate evaluation of the damage profiles. Figure 4.3(c) shows 0.94 MeV D^+ spectra of 4H-SiC wafers implanted with 1.1 MeV Al_2^{+2} at various doses. The implantation dose rate and temperature were, respectively, about 2×10^{12} $cm^{-2}sec^{-1}$ and 150K. The implantation geometry was defined by a 60° tilt angle off the sample normal with respect to the ion beam.

The results discussed in the following come from analyses of spectra like those shown in Figure 4.3. We will also review the status of damage measurements in crystalline SiC. Before doing so, however, we will discuss a premise about the problem of the computation of damage profiles in implanted SiC from backscattering channeling measurement because such a subject is linked to that of ion damage in SiC. The analysis of light ion backscattering channeling spectra is generally done under the hypothesis of a linear dechanneling approximation, assuming that channeled He^+ ions experience a random stopping power and assuming the SiC density of the implanted layer is constant and equal to that of the crystalline SiC. Neither one of these assumptions is true. Further, the quantitative knowledge about the slowdown of energetic light ions along channeling directions in single-crystal SiC is lacking experimental data. In fact, the stopping power reduction along the <0001> direction in 4H-SiC and 6H-SiC with respect to the random direction for MeV He^+ was just published in 2003 [51]. Moreover, consensus about the amount of the reduction of the SiC density because of the disorder introduced by the ion damage has not yet been reached. This last point refers to the so-called "swelling" phenomenon and, also in this case, only since 2003 has a molecular dynamic (MD) computational approach been able to account for the various experimental data published in the mid-1990s [49, 52, 53] by modeling the relaxation of a volume of single-crystal SiC versus a variable fraction of totally displaced atoms. This work is presented in [54]. Finally, to take into account the channeling stopping power reduction and material density variation, a simulation tool for channeling backscattering spectra is necessary and only a few research groups have such a tool for SiC. A Monte Carlo—binary collision approximation (MC-BCA) code for the simulation of channeling RBS spectra is described in [47].

The accumulation of disorder in the C and Si sublattices increases for increasing ion doses (i.e., fluence value for both 4H-SiC and 6H-SiC) and is shown in Figure 4.4. The use of the unit "dpa" (displacements per atoms) for the implanted dose [see Figure 4.4(a, b)] will be discussed in the next paragraph. The disorder increases versus dose with a sigmoidal trend at both the Si and C sublattices, as shown in Figures 4.4(a). The experimental data are fitted by an analytical function that accounts for the contemporaneous presence of weak and heavy (i.e., amorphous) damaged volumes, as explained in [55]. Several models for damage accumulation can account for

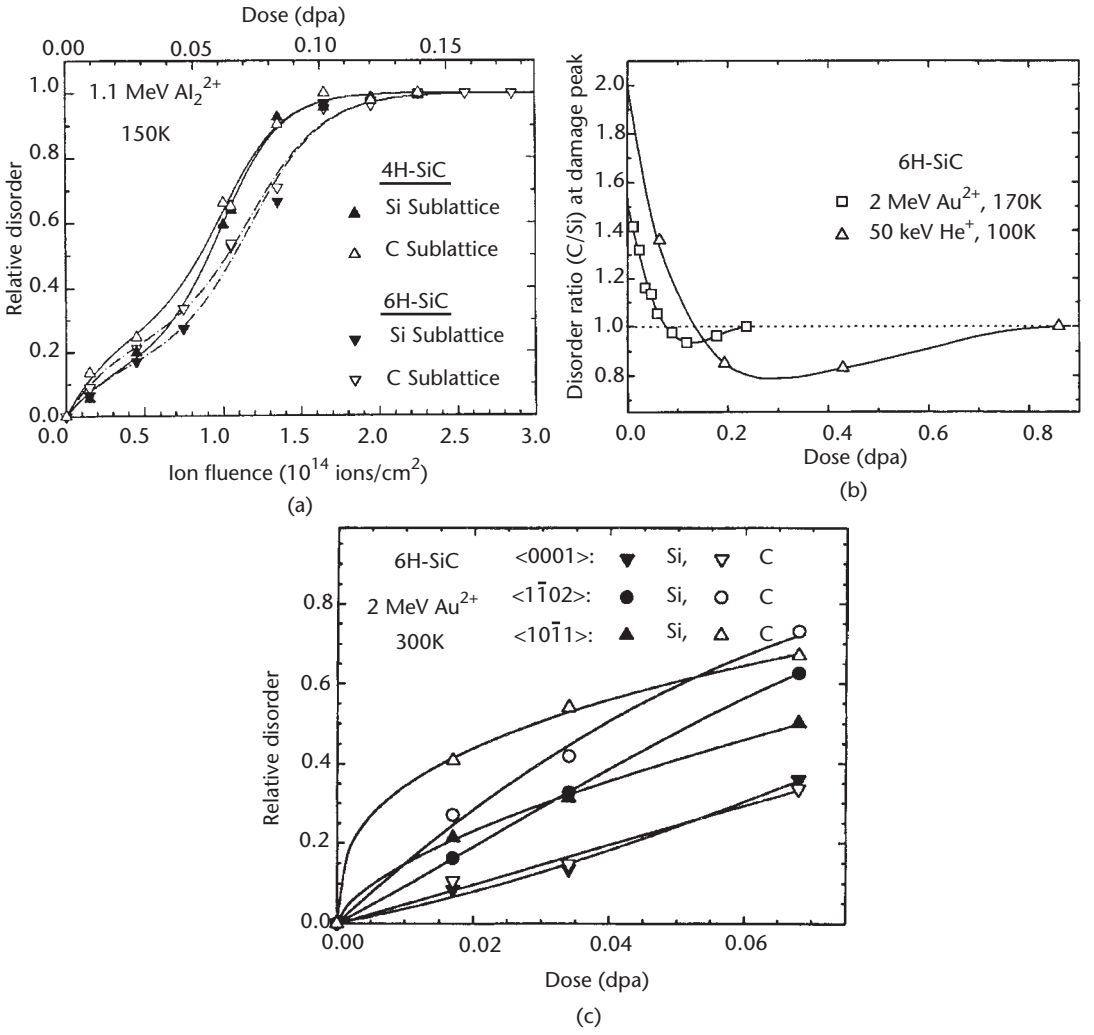


Figure 4.4 Evolution of the damage in the C and Si sublattices versus the ion dose (i.e., fluence) at the peak damage position. (a) From the early damaging up to the amorphous state. (*From:* [55]. © 2000 Elsevier B.V. Reprinted with permission.) (b) Low damage level (*From:* [59]. © 2001 American Institute of Physics. Reprinted with permission.) (c) Very early damage. (*From:* [60]. © 2001 American Physical Society. Reprinted with permission.)

such a sigmoidal trend and a review of them can be found in [56, 57]. The simulation of heavy ion damage accumulation in SiC by MD methods also gave such a sigmoidal trend, as shown in [58] for the 3C-SiC polytype. The curve of damage accumulation for the 3C-, 4H-, and 6H-SiC do not overlap [in Figure 4.4(a), only the 4H and 6H cases are reported]. At weak ion damage the defect configuration might differ from one SiC polytype to the other. Because the RBS-C yield is dependent on the microscopic structure of the defects, it can be understood that for the same dpa, the disorder density was polytype-dependent. Figure 4.4(b) shows the ratio between displaced C and Si atoms versus dose for different implanted ions. It can be noticed that even if the trend for damage accumulation is similar for the C and Si sublattices, the absolute magnitude of disorder at the two sublattices differs. In fact, for low crystal damage the number of displaced atoms is larger for C than for Si. But, as the damage increases

the C to Si ratio first decreases to become lower than one, goes through a minimum and then increases toward the saturation value 1 (i.e., an equal fraction of displaced C and Si atoms). Both resonant backscattering measurements and nuclear reaction analyses reported, respectively, in [31, 59], agree on this result. Figure 4.4(c), taken from [60], shows the measured fraction of C and Si displaced atoms along three different crystal orientations. These results refer to implantation experiments performed at RT and confirm the trend about the relative ratio among C and Si displaced atoms at low damage levels. Moreover, they show that defects formed during the very early stage of the damage accumulation are highly anisotropic. It can be noticed that MD simulations of collision cascade in 3C-SiC, reported in [61], show that the displacement energy (E_d) is different for the C and Si sublattice and is also strongly dependent on the crystallographic orientation.

SRIM is the simulation code for implantation of amorphous materials that is primarily used and it can be downloaded for free from the Web site cited in [62]. This code also computes the "damage" profile as the number of atoms displaced from their original position and the number of atom positions left vacant per impinging ion. These profiles are assumed to approximate the disorder profiles in crystalline materials, although no model for dynamic damage recovery is assumed in SRIM. The energy threshold for atomic displacement E_d is an input of the simulation code that, in the case of SiC, differs for Si and C atoms as predicted by the MD computation of ion damage cascade in crystalline 3C-SiC presented in [61]. Figure 4.5(a) shows that simulated and measured disorder profiles can fit under the hypothesis that E_d varies with the ion fluence (i.e., with the damage level). In particular, Figure 4.5(b) shows that for increasing doses and fixed ion fluxes and energy values, E_d increases for the C sublattice and decreases for the Si one. This result is coherent with those presented about the ratio of the disorder between the C and Si sublattices for increasing doses. The results presented in Figure 4.5(c) show that by decreasing implantation temperature and ion fluence, the E_d values seem to approach a value independent of the ion species. E_d = 35 eV for the Si sublattice seems a reasonable asymptotic value and corresponds to the output of the MD collision cascade simulation reported in [61]. Even if no experimental measurement exists for the C case, the E_d values for Si and C obtained by MD cascade simulation are the most frequently used to evaluate the number of displaced atoms in the absence of dynamic recovery. These E_d values are 35 eV for Si and 20 eV for C, as published in [61], and they are used for all incident ion species. The number of displaced atoms normalized to the SiC atomic density is the dpa (i.e., the unit measurement so often used for the relative ion dose). In so doing, the results corresponding to a huge range of implantation parameters can be readily compared over the same dose scale.

Figure 4.6 shows data that summarize the current knowledge about damage accumulation in SiC versus ion mass and implantation temperature. Almost all the experimental data that will be discussed from here on concerns the Si sublattice. In a first approximation, they can be considered representative of the whole SiC network because it has been observed that damage accumulations on the Si and C sublattices are rather similar (see Figure 4.4). The data in Figure 4.6 refer to both 3.5° off-axis 6H-SiC and 8° off-axis 4H-SiC wafers implanted at 60° off the wafer normal. The dose rate was in the range 1×10^{12} $cm^{-2}sec^{-1}$ to 8×10^{12} $cm^{-2}sec^{-1}$, but

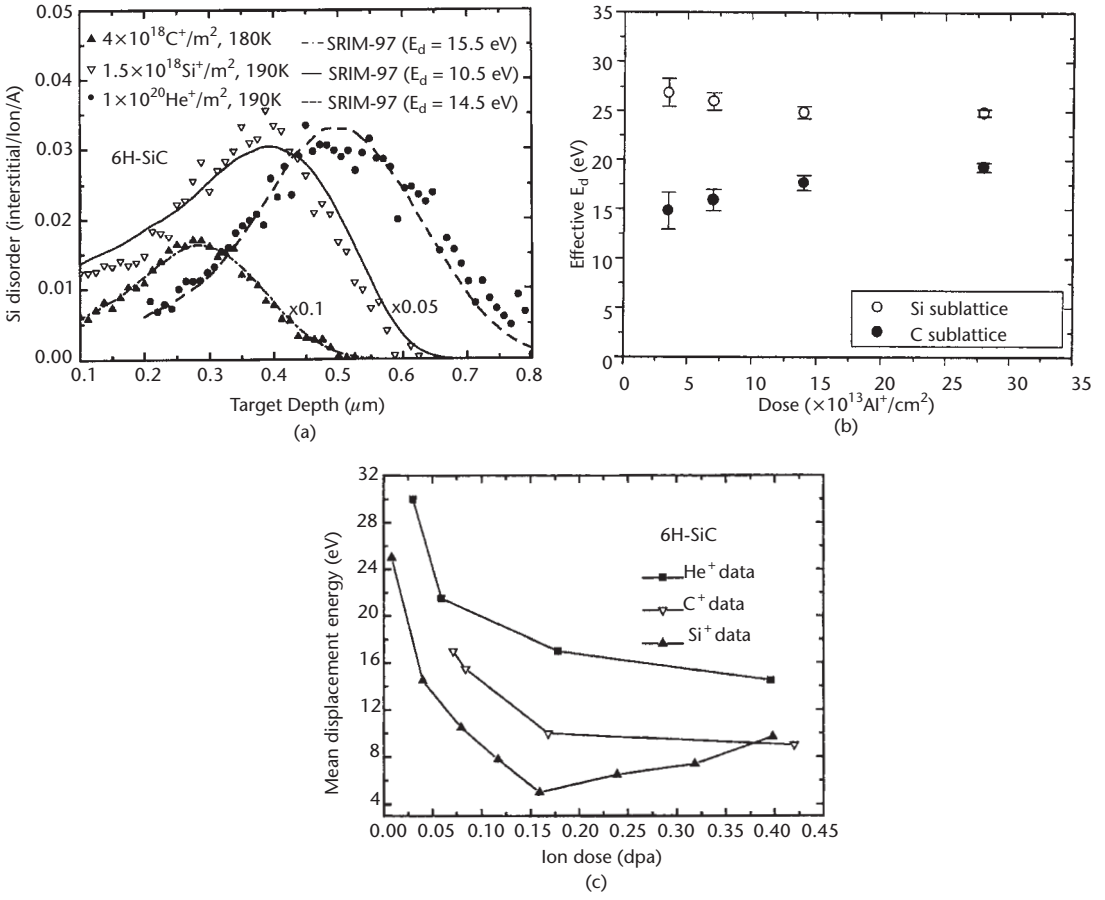


Figure 4.5 (a) Comparison between the computed and measured displaced profiles: SRIM-97 simulation versus experimental data. (*From:* [63]. © 1999 Elsevier B.V. Reprinted with permission.) (b) E_d values for the C and Si sublattices in 6H-SiC versus ion dose for 300K implantation temperature. (*From:* [31]. © 2002 Elsevier B.V. Reprinted with permission.) (c) E_d for the Si sublattice in 6H-SiC versus ion dose and ion mass for 180–190K implantation temperature. (*From:* [63]. © 1999 Elsevier B.V. Reprinted with permission.)

here this parameter will be assumed constant. Figure 4.6(a) shows that the disorder accumulation at the damage peak increases both for increasing ion mass and ion dose. Figure 4.6(b), taken from [5], shows the disorder accumulation at the damage peak versus implantation temperature for increasing ion dose and fixed ion mass. The disorder still increases with increasing dose, but the rate of disorder accumulation decreases with increasing implantation temperature. The dose necessary to amorphize SiC increases with increasing implantation temperature, as shown in Figure 4.6(c) up to a so-called critical temperature. At and above this temperature, the dynamic balance between damage accumulation and damage generation is such that the SiC amorphization may never occur even at very high doses. In such a balance an added contribution to an ion-induced defect recovery cannot be excluded. Studies in this field and at the temperatures of interest for implantation processing are only at a preliminary stage and one of these can be found in [64].

Figure 4.7, taken from [26], presents the role played by the ion dose rate on damage formation and accumulation. Studies of this type can be found in [26, 35].

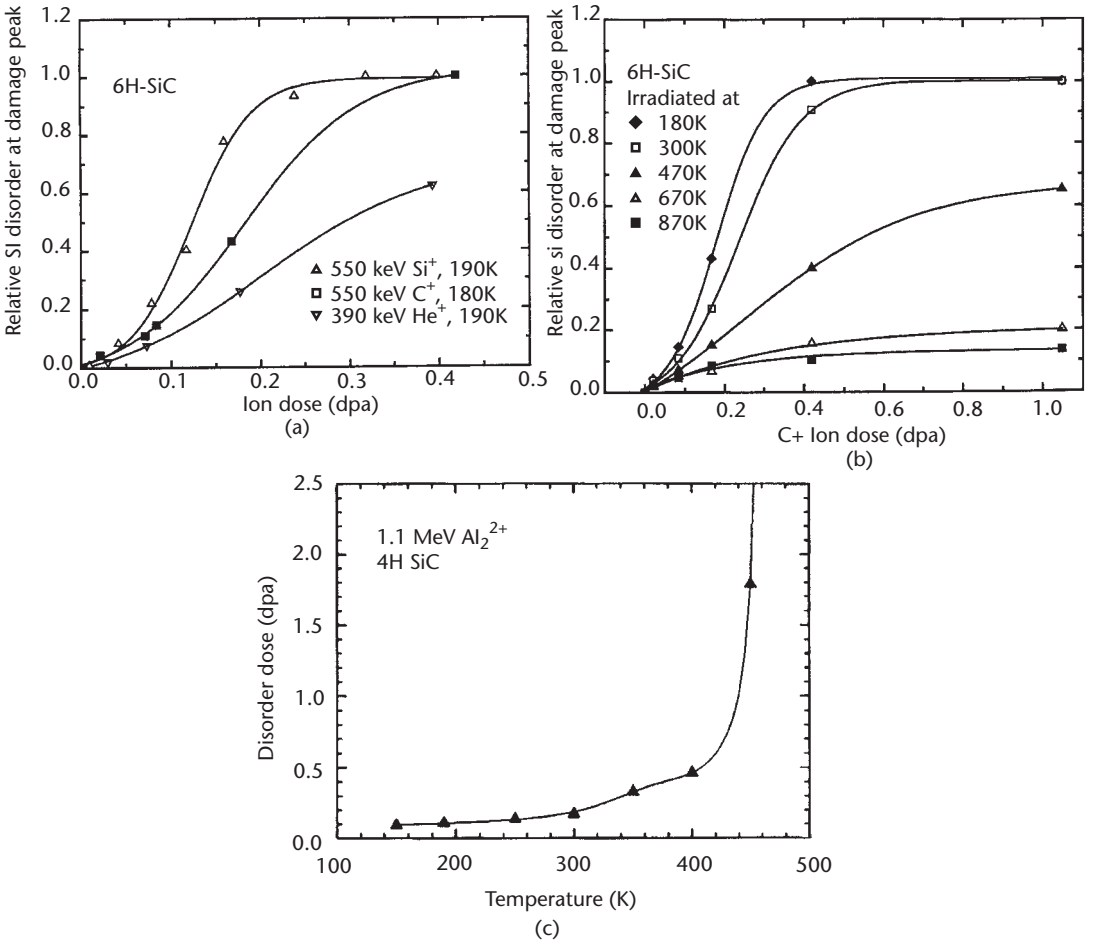


Figure 4.6 Disorder at the damage peak for the Si sublattice versus (a) the ion mass (*From:* [63]. © 1999 Elsevier B.V. Reprinted with permission.) and (b) the implantation temperature (*From:* [5]. © 1999 Elsevier B.V. Reprinted with permission.) Part (c) shows the increase of the dose for amorphization versus increasing implantation temperature (*From:* [35]. © 2003 American Institute of Physics. Reprinted with permission.).

Figure 4.7(a) shows the values of the disorder at the Si damage peak versus implantation temperature for various dose rate values and constant dose (5×10^{14} cm^{-2}). The implantation temperature was varied in the range RT-240°C. The dose rate (i.e., the flux) varied in the range $1.9 \times 10^{10} - 4.9 \times 10^{13}$ cm^{-2}sec^{-1}. The samples were 8° off-axis 4H-SiC wafers. The implantations were done with a 100 keV Si^{+} beam parallel to the wafer normal. For this wafer such a beam to crystal orientation corresponds to a random implant (see Section 4.2.3). The data in Figure 4.7(a) show that the transition from total disorder to "no" disorder shifts toward higher temperatures with increasing ion dose rate and the same is true for the critical amorphization temperature. The authors fitted the data by an exponential function of the type "relative damage yield" $= a + b\,[1+\exp(\delta(T-T_c))]^{-1}$ where T is the implantation temperature, δ is the amplitude of the order-disorder transition that can be derived from the experimental data, and a and b are constant parameters. T_c is the only free parameter to optimize the fitting between experimental and computed trends. Such T_c might be assumed as representative as the order-disorder transition at a given

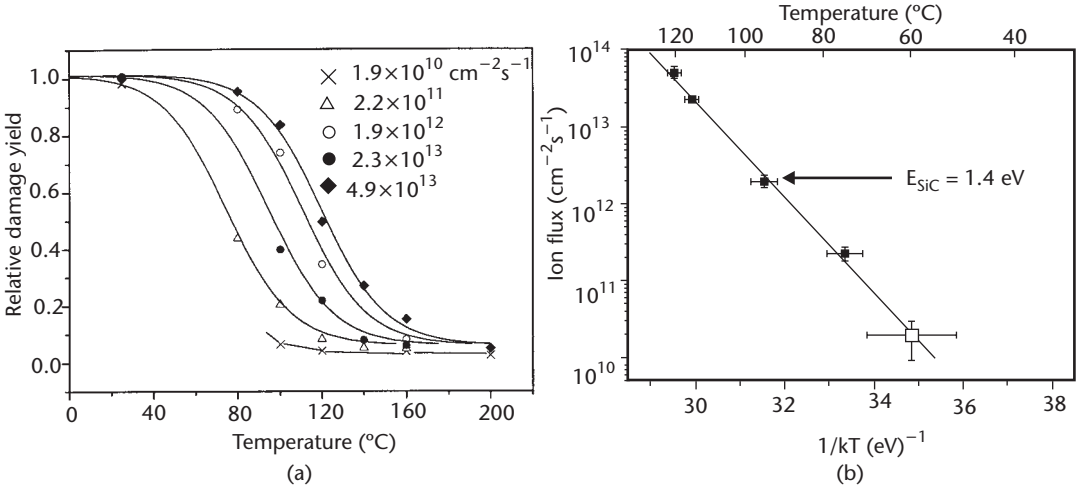


Figure 4.7 Influence of the dose rate on damage accumulation in 4H-SiC for fixed ion mass and ion energy: (a) damage at the peak of the Si sublattice versus increasing dose rate and increasing implantation temperature; (b) evaluation of the energy activation for the phenomenon responsible of the shift versus temperature shown in part (a). (*From:* [26]. © 2003 American Institute of Physics. Reprinted with permission.)

dose rate. Once the T_c values and their corresponding dose rates are depicted in an Arrhenius plot, as shown in Figure 4.7(b), the activation energy for the mechanism(s) responsible for the curve shift in Figure 4.7(a) can be estimated. This energy was computed to be equal to 1.4 eV. Such a value is one order of magnitude higher than that obtained by the Arrhenius analysis of the onset of the SiC amorphization produced by Xe^+ ions reported in [65] and equals the energy barrier theoretically predicted for the annihilation of C interstitials in a neutral charge state reported in [66, 67]. Taking into account that MD simulations of ion damage cascades predict an excess of C interstitials as a final product of the collision cascade (see [58, 67]) and that such a configuration seems to be still present in the SiC crystals also for damage yield as high as 0.5 (see Figure 4.4 and related references), it seems reasonable to hypothesize that the annealing of C interstitial defects plays a vital role for the dynamic balance between damage accumulation and damage recovery in the temperature range 60–120°C. Such a temperature range is quite near to the experimental anneal temperature of C interstitials in a split configuration, for which a range of 150–200°C is mentioned in [68]. Furthermore, calculations based on density functional theory suggest an activation energy of ~1.4 eV for the migration of Si interstitials (split interstitial configuration) in n-type SiC with only a minor barrier for the annihilation process ($Si_i + V_{Si} \rightarrow \emptyset$) [66, 67]. Hence, Si interstitials are also likely candidates to be involved in controlling the dynamic annealing process.

During postimplantation annealing, extended defects can be formed in the implanted layers, but the onset of such defects may already be present after the implantation process depending on the damage accumulated in the implanted layer. Figure 4.8 compares disorder profiles and dark field cross-section TEM images of the same samples. These samples were implanted with the same dose (2.7×10^{15} cm^{-2}) but with different dose rates (100% and 60%) so as to obtain different damage levels at the damage peak. The samples were 8° miscut 4H-SiC wafers implanted with 1.1 MeV Al^+ ions along a direction 60° off the wafer normal. The implantation temperature was 450K. The implantation dose rates of these two samples varied by a

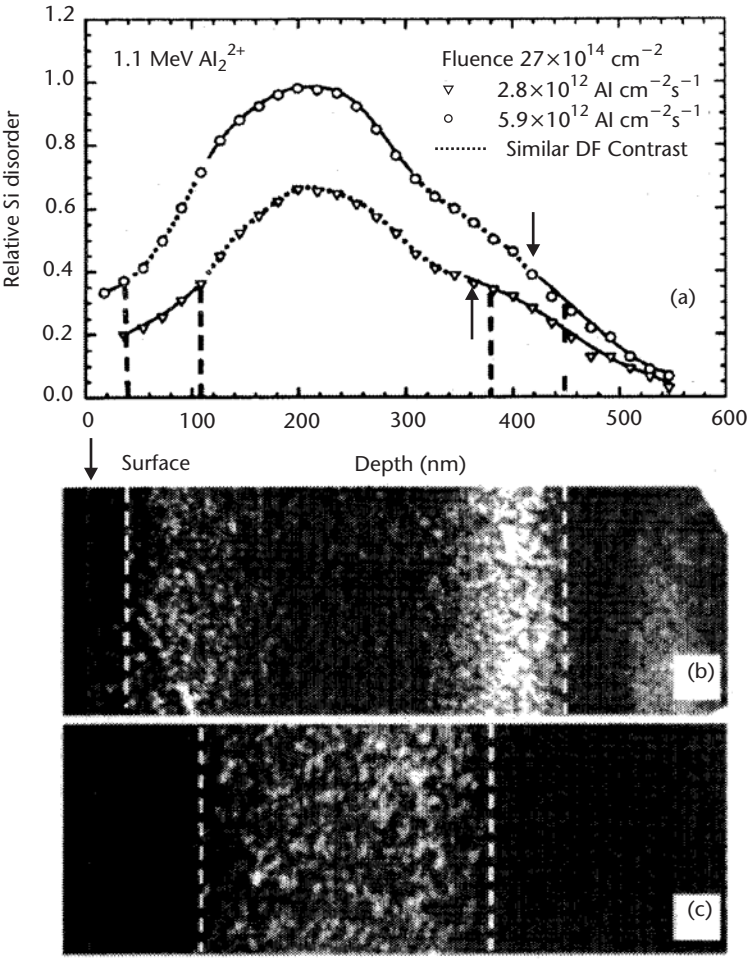


Figure 4.8 Comparison between (a) disorder profiles and (b, c) dark field cross-section TEM images of the same samples. TEM image (b) refers to the sample with the higher disorder level at the damage peak, whereas TEM image (c) refers to the sample with the lower disorder level at the damage peak. The vertical dotted lines indicate the depth of outer boundaries of the high-contrast regions in the cross-sectional TEM images. (*From:* [35]. © 2003 American Institute of Physics. Reprinted with permission.)

factor of two and thus the implantation time differed by the same factor. Both samples were thermally treated after implantation at the same implantation temperature for durations longer than the maximum implantation time with the aim to ensure that the differences in the features of the damage profiles were only due to the dynamics of damage accumulation during hot implantation. Measurements of the disorder profiles before and after this postimplantation annealing confirmed that the features of the disorder profile were independent of the low-temperature post-implantation annealing. Stretching the TEM images with respect to the depth scale of the disorder profiles a correspondence between equal TEM contrast regions and an equal level of disorder was hypothesized. This is evidenced by the dotted lines in Figure 4.8 that indicate the disorder profiles at the outer boundaries of the high-contrast regions of the cross-sectional TEM images. Such a comparison is only qualitative but it could be quantitatively exploited, as already done in the case of

implanted Si in [69]. Selected area diffraction and high-resolution images of the area corresponding to 40–60% disorder level showed that in these regions the SiC is highly strained but still crystalline with no extended defects. Similar investigations made in the region with 100% disorder showed that the SiC contains many small amorphous inclusions within a crystalline matrix full of planar defects, such as extra planes and onsets of vacancy and interstitial condensations.

4.2.2.3 Chemical Depth Profiles

The correct prediction of the profile of the implanted ion within the SiC crystal will be treated in Section 4.3 concerning random implants. SRIM, the code primarily used for ion implantation simulation processes in amorphous materials (see [62]), contains predictions that reasonably fit with experimental SIMS data for ions in the low (tens) to medium (hundreds) ion keV energy range. At higher MeV energy values this is no longer the case, probably because the algorithms used in SRIM to evaluate the ion energy loss is not valid. Empirical ion implantation simulators using Pearson frequency functions can be constructed as described in [70], where a large number of measured SIMS profiles were used to determine the best fit of the analytical functions necessary to describe the first four moments of the implanted profiles versus implantation energy. The good agreement between the experimental and the Pearson distribution profiles obtained by the authors of [70] can be seen in Figure 4.9. Monte Carlo codes in the frame of the binary collision approximation (MC-BCA) or MD codes have also been proposed to simulate the random implantation process in crystalline SiC, as described in [46, 71]. The outputs of these codes show a very good agreement with the experimental data, as shown in Figure 4.10, which was reproduced from [72, 73] and refers to the results of the MC-BCA code described in [46, 73]. This code takes into account the progressive increase of the crystal disorder with increasing doses and the consequent reduced probability for channeled trajectories and also accounts for depth-scale correction due to the swelling phenomenon when the crystal is heavily damaged. Simulated and measured damage and implanted ion profiles are shown Figure 4.10. The shift toward larger depth of the chemical profiles for increasing fluence values is the consequence of the decrease of the material density because of the increased material disorder. The measured disorder profiles of Figure 4.10(a) were computed from the RBS channeling spectra shown in Figure 4.3(a) in the frame of the linear de-channeling approximation. Moreover, He^+ stopping power reduction in the channeling direction and the change of material density proportional to the damage increase were taken into account.

4.2.3 Channeled Implants

Random and channeled implanted profiles in 6H-SiC are shown in Figure 4.11(a). These profiles correspond to implants performed at RT with 1.5 MeV Al^+ to a low fluence (~ 10^{13} cm^{-2}). The flux is not accurately defined because of the experimental constraints, as explained in [74]. In fact, most of the studies concerning channeled implants make use of ion beams in single- spot configurations and have to face the problems related to nonhomogeneous flux distribution within the beam spot. The

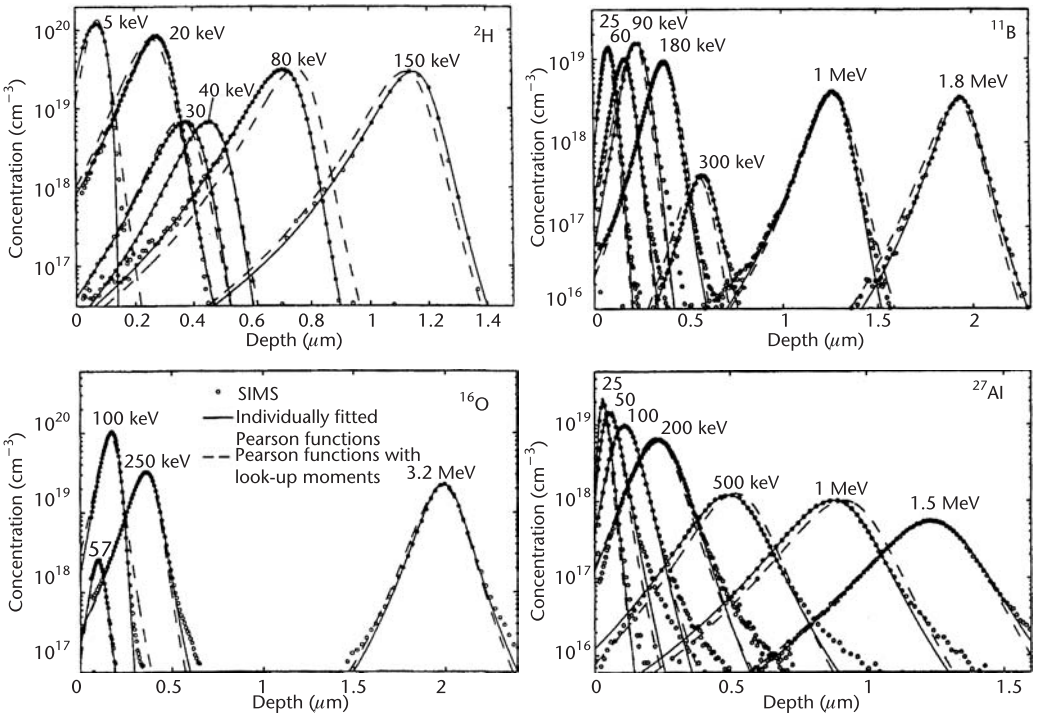


Figure 4.9 Comparison between SIMS measured profiles (dotted line) and computed profiles using the Pearson frequency functions with the first four moments determined for each individual profile (solid line) or computed via analytical functions obtained through the best fit of the individual moments (long dashed line). (*From:* [70]. © 2003 American Institute of Physics. Reprinted with permission.)

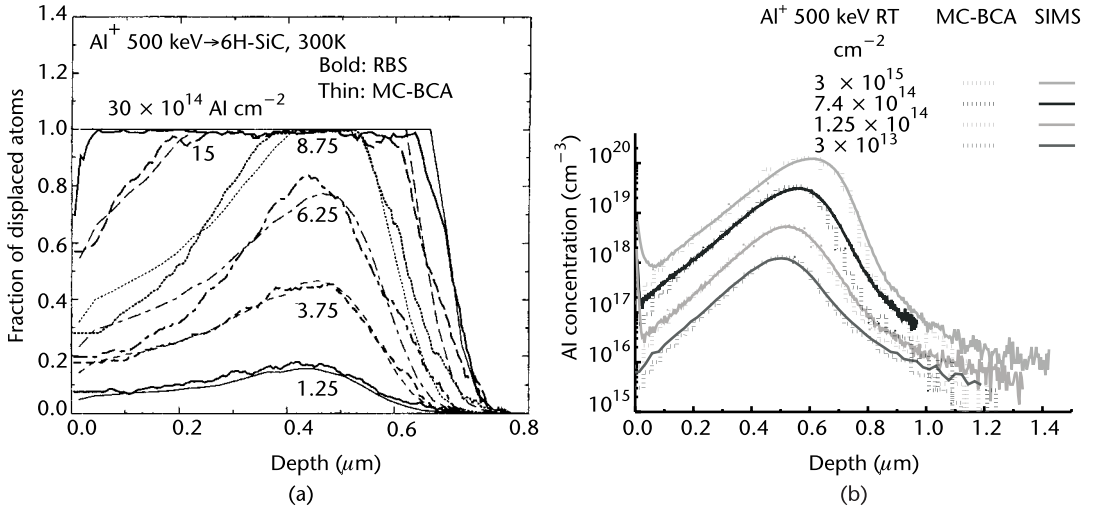


Figure 4.10 Damage and doping profiles for the same set of random as-implanted 6H-SiC samples. (a) Comparison between RBS-C measured and MC-BCA simulated damage profiles. (*From:* [73]. © 1999 Elsevier B.V. Reprinted with permission.) (b) Comparison between SIMS measured and MC-BCA simulated chemical profiles. (*From:* [72]. © 2001 Material Science Forum. Reprinted with permission.)

channeled profile is deeper than the random one and has a trapezoidal shape, whereas that of the random profile is almost Gaussian. These differences are due to the fact that channeled ions experience lower electronic energy loss and less nuclear

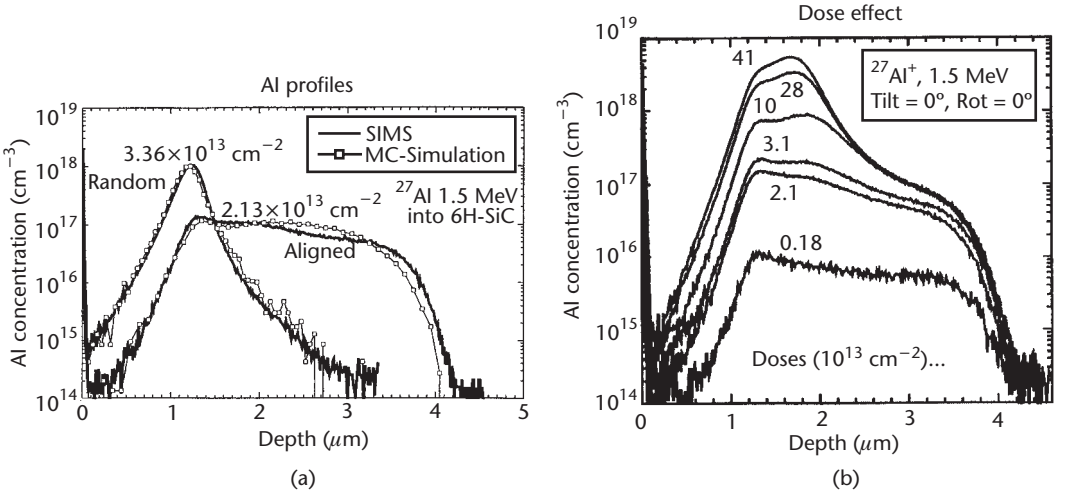


Figure 4.11 Random and channeled doping profiles in 6H-SiC. (a) Comparison between SIMS measurements and MD simulations for a low fluence value. (*From:* [74]. © 2000 Material Science Forum. Reprinted with permission.) (b) Evolution of the SIMS profiles for channeled implants at increasing fluence values. (*From:* [24]. © 1999 American Institute of Physics. Reprinted with permission.)

collisions than the random ions. Nuclear collisions are responsible for the atom displacements (i.e., the buildup of disorder in the crystal). As the damage increases the number of de-channeled ions in channeled implants increases and the doping profiles modify accordingly, as shown in Figure 4.11(b). The deepest edge of the channeled profile saturates with increasing ion fluence, and the profile shape progressively resembles that of random implants. In between the two extreme cases (i.e., full channeled and full random), there is a configuration that appears to be highly probable, as shown by the presence of a peak at intermediate depth between the random peak and the channeled front edge. The MC simulation of these channeled implantations, presented in [71], accounts for the shape of the profiles as shown in Figure 4.11(a). Increasing the fluence, the qualitative trend of the chemical profile is reproduced but not the quantitative ones. This means that improvements in the modeling of the ion damage formation and accumulation or in the modeling of the scattering efficiency for channeled implants are required. Here it should be pointed out that experimental data for the damage buildup during channeled implants are crucial for the modeling but until now such data are scarce and the only published ones are those in [75].

A recent experimental study about channeled implants, published in [23], has shown the interesting features of axial- and planar-channeled implants in 4H-SiC, presented in Figure 4.12. This data refer to 60 keV Al^+ implantation in <0001> and <11–20> oriented 4H-SiC wafers. Each profile corresponds to a different orientation of the ion beam with respect to the crystalline network, as reported in the inset of the figure. All of them are shown on a concentration scale normalized to the implantation dose. The profiles of axial implants show an ion penetration progressively deeper for the <0001>, the <11–23>, and the <11–20> axes, with a factor equal to 45 between the two extreme cases. The profiles of the planar implants show that a not-negligible channeling tail can be present at certain tilt angles with respect to the wafer axis. These angles depend on the crystal plane and the SiC polytype, for

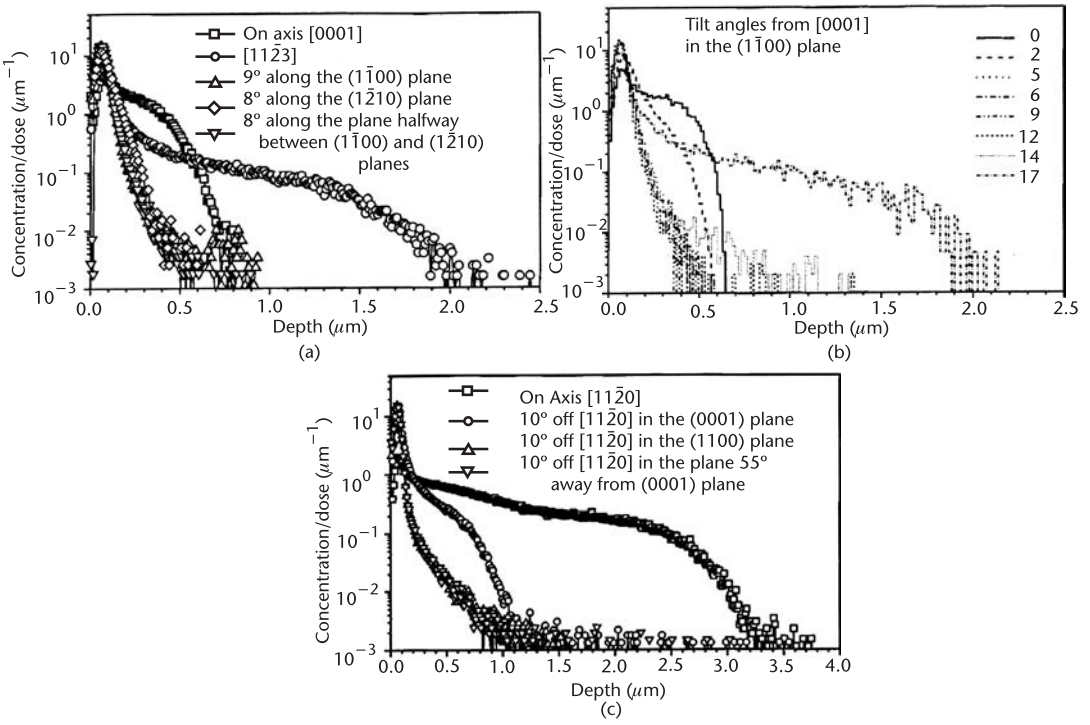


Figure 4.12 Doping profiles of 60 keV Al^+ ions implanted in 4H-SiC with different alignments of the beam direction with respect to the crystalline network. Parts (a) and (b) refer to wafers and part (c) refers to the –20 ones. The beam-to-crystal alignment per profile is given in the inset of each picture. Parts (a) and (c) are SIMS measurements and part (b) is an MC-BCA simulated profile. The concentration scale is normalized to the implantation dose. (*From:* [23]. © 2003 American Institute of Physics. Reprinted with permission.)

example the <11–23> axis within the plane (1–100) is placed at 17° from the axis in the 4H-SiC structure but at 11.6° in 6H-SiC. When positioning a wafer for implantation the presence of these channeled directions should be taken into account. Figure 4.12(b) shows MC-BCA simulations of the (1–100) planar implants at various tilt angles with respect to the <0001> axis. The qualitative agreement between these simulations and the experimental data of Figure 4.12(a) is very good.

The huge differences in the penetration depth between different crystallographic axes and the fact that a certain level of damage is necessary to inhibit channeled trajectories raise the issue of the stochastic channeling trajectories at the early stage of any implantation process. Unfortunately, experimental data are not available, but MD and MC-BCA simulations allow us to appreciate how important such a phenomenon may be at the mask border and for very low fluence values like those used for junction terminations. As an example, Figure 4.13 shows the results published in [76] for a fluence of 10^{13} cm^{-2}. This figure is a cross-section view of the simulation results in the (10–10) plane, where the directions vertical and parallel to the wafer surface are, respectively, the <0001> and <11–20> axes. To minimize the channeling effects, the implantation beam was directed 7° away from the wafer normal within a plane at 15° from the (10–10) plane (i.e., halfway between the (10–10) and (11–20) planes). Despite the fact that this is a good random implantation geometry, substantial doping tails are present next to the sample surface along the

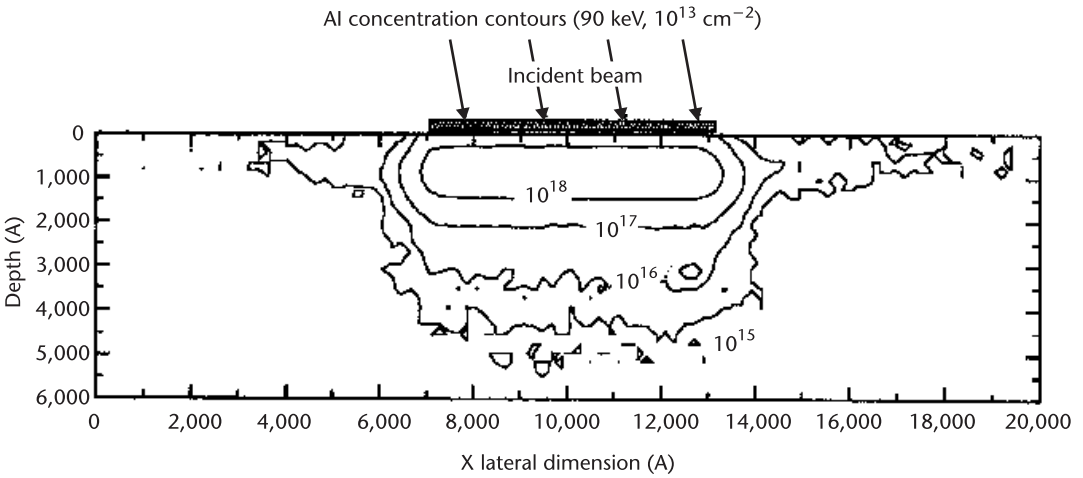


Figure 4.13 Concentration contours in on-axis 6H-SiC for 90 keV Al^+ implanted at 7° from the wafer normal within a plane halfway from the (10–10) and (11–20) family of planes. The implantation dose is 10^{13} cm^{-2}. The picture is a cross section of the sample in the plane (10–10), thus the parallel and the normal to the wafer surface are, respectively, the <11–20> and <0001> axes. (*From:* [76]. © 1999 Elsevier B.V. Reprinted with permission.)

direction parallel to the <11–20> axis. The experimental data shown in Figure 4.12(c) gives strong support to these simulations results.

4.3 Implant Annealing

The thermal annealing normally performed after ion implantation processing serves the dual purpose of removing defects and activating dopants. The electrical activation of the implanted ions (i.e., the incorporation of dopants on proper lattice sites) is therefore a process intimately linked to the presence of defects. In order to understand the activation process, it is also necessary to investigate the evolution of lattice damage or even follow the history of individual defects during the annealing.

Although a substantial part of the implantation-induced damage can be removed by 1,200°C annealing, to achieve reasonable electrical activation annealing at temperatures in excess of 1,500°C should be performed because of the high bonding strength of the SiC lattice [9, 77]. At such elevated temperatures the SiC crystal surface may decompose due to selective out-diffusion of Si from the SiC lattice. Hence some means to permit high-temperature annealing of SiC implants while suppressing the out-diffusion of Si from the surface is required. However, higher annealing temperatures also cause extended defects, such as dislocation loops, to appear, similar to the end-of-range defects seen in implanted and annealed Si. This imposes further limits on the annealing temperature/time window that can be used in processing ion-implanted SiC.

4.3.1 Annealing Concepts

M. A. Capano et al. performed B implantation on 4H-SiC and B and Al implantations on 6H-SiC [6]. The implanted samples were annealed in a resistively heated furnace for various temperatures between 1,500–1,800°C. Most of the samples

were annealed for 40 minutes without the use of a SiC wafer cap, which is a technique whereby a second SiC wafer is clamped to the implanted wafer so that Si surface out-diffusion is suppressed by the cap wafer. The samples were annealed at 5 μTorr pressure of Ar. Implant annealing was also performed with the SiC cap, where the cap was separated from the implanted wafer by a distance of 250 μm. The annealed samples were characterized via atomic force microscopy (AFM), C-V measurements of capacitors formed by patterning Ni on to the implanted surface, and finally with the use of transmission line method (TLM) measurements. It was observed that temperatures in excess of 1,650°C were required to reach high activation levels for boron implants in 4H-SiC and complete activation was finally reached at 1,750°C. The sheet resistances of the Al-implanted 6H-SiC samples that were annealed at 1,800°C were measured to be 32.2kΩ/□. There was an increase in the surface roughness after implant annealing of the samples in the Ar ambient. According to a model that was proposed in this work to explain the observed surface roughness, SiC sublimation and highly mobile species enable the surface to reconfigure itself. Thus it was proposed that annealing performed in an ambient that prevents desorption of Si-containing molecules would suppress the mechanism that leads to roughening of the implanted/annealed SiC samples. Indeed, Saddow et al. have used a silane overpressure process to achieve this very goal [9, 77], which will be discussed in more detail in Section 4.3.2.1.

D. Kawase et al. investigated Si regrowth from the amorphous phase caused by Al implantation; recrystallization of the specimens when annealed at temperatures between 800–1,600°C in Ar flow for 30 minutes was achieved [78]. The damage induced by the implantation and the damage reductions by the subsequent annealing were determined by electron spin resonance (ESR) and TEM.

K. A. Jones et al. have used an AlN capping layer to prevent Si evaporation during activation of n-type dopants up to a temperature of 1,600°C [79]. After annealing the AlN cap must be stripped off, which adds processing complexity. In addition pinholes in the AlN cap can form, especially at temperatures above 1,600°C, thus limiting the utility of this approach. This is especially true in the case of complete activation of p-type dopants, which require annealing temperatures above 1,700°C. Hence L. B. Ruppalt et al. proposed a dual BN/AlN capping layer for performing annealing on implanted SiC up to a temperature of at least 1,700°C [80]. The AlN was used as a protective layer on SiC as it is chemically inert to the material, whereas the BN layer on top of the AlN cap would prevent the AlN from evaporating at temperatures in excess of 1,600°C. Both layers were deposited by pulsed laser deposition (PLD). After performing high-temperature annealing, the BN layer cap was removed by ion milling and the AlN was selectively etched with a warm KOH etch. The surface structure after etching off the cap layers was examined with SEM, X-ray diffraction (XRD), AFM, and high-resolution TEM (HRTEM). They observed that the surface of the film remained unchanged and there were no cracks or hexagonal thermal pits that had been observed when only AlN cap layer was used due to the exposed AlN. An Auger electron spectroscopy (AES) analysis of the surface showed no evidence of Al or N contamination. However, the processing steps involved using this method are daunting for production. First, large-area cap deposition using PLD is difficult as the deposition footprint is normally limited to a few cm in diameter. Second, the two-step process to remove the dual-level cap is both time-

consuming and can lead to processing errors, such as ion-milling through the BN cap into the AlN cap or, worse, through both caps and into the underlying SiC surface.

C. Dutto et al. performed laser annealing (LA) as an alternative to the classical thermal annealing processes for activation of ion-implanted dopants in SiC [81]. They used powerful-pulsed excimer laser beams of nanosecond duration to deposit large amounts of energy in a short time into the near-surface region, while maintaining the substrate essentially at RT. They demonstrated the possibility to anneal Al implant-induced damage out of 4H-SiC by single-shot laser processing in the solid phase using an XeCl excimer source of 200-ns pulse duration. The surface study revealed that this process kept the surface stoichiometry (Si:C) near unity and prevented any strong surface degradation. The electrical activation of the Al dopant was confirmed by I-V measurements, which were performed on mesa pn junction diodes. Unfortunately they did not report on the dopant activation percentage so it is difficult to assess the usefulness of this technique. In addition, while laser annealing is an attractive research approach, for high-volume device production the suitability of this approach is in doubt.

Several other types of annealing processes have been used, such as furnace annealing and rapid thermal annealing (RTA). Main differences are heating ramp or/and annealing time, respectively, which are faster and shorter for RTA than for furnace annealing. The strong thermal gradients present in the RTA case might induce an undesired warp of the wafers. Moreover, during RTA for annealing temperatures in excess of 1,400°C Si out-diffuses from the sample surface and causes the step-bunching phenomenon [82]. Such a phenomenon is much less pronounced in the case of furnace-annealed SiC samples. In fact, in this case, temperatures as high as 1,800°C were successfully employed [83].

4.3.2 Silane Overpressure Annealing Process

The development of a silane-based overpressure annealing process is a critical step forward for SiC technology and is not only cost-effective compared with other methods, but has been shown to result in high-quality material suitable for device applications. The basic operating principle of this method is simple: a sufficient overpressure of Si, in the gas phase above the sample, prevents the selective out-diffusion of Si from the SiC lattice at the surface. Provided the Si overpressure is below the level where Si droplets can form (i.e., gas-phase nucleation of Si, which then adsorb onto the SiC surface), this technique is effective. Empirical calculations have been performed to assist in the transfer of this atmospheric pressure process to low pressure, which is important for several reasons. First, many SiC reactors operate at low pressure and this would permit a silane overpressure process to be most rapidly used by these systems. Second, and most importantly, is a shift in gas phase equilibrium that occurs at a low pressure, which helps to suppress Si cluster formation in the gas during sample annealing. Hence a serious defect in SiC, Si droplets, can be avoided during implant annealing if the process is transferred to low-pressure process conditions. Indeed, at the University of South Florida this exact process transition to low pressure, based on the atmospheric pressure process described here, is underway. Results of this work will be published at a future date.

Although the SiC lattice is inherently stable at lower temperatures, Si can out-diffuse at elevated temperatures, leading to a severe degradation in the surface morphology known as step bunching [82]. Much research has been reported on implant annealing of SiC with various encapsulations that suppress this out-diffusion of Si during high-temperature annealing, as outlined in Section 4.3.1. The most common process gas for implant annealing is argon, due to its inert nature. As previously mentioned, some of the research indicated that annealing SiC in an Ar ambient results in surface roughness, especially for annealing temperatures greater than 1,500°C. S. E. Saddow et al. developed an implant annealing process using silane gas to provide an overpressure of Si vapor during annealing [9, 84]. In this process, silane gas provides a partial pressure of Si, which helps to suppress surface migration of Si in the SiC lattice, resulting in a reduced surface roughness. AFM data shown in Figure 4.14 compares the surface morphology of two identically processed wafers on which LD MOSFETs (see Chapter 5) were fabricated with different implant annealing conditions [84]. The wafer annealed in an Ar ambient (T = 1,550°C) exhibited step bunching, as can be seen in the figure. These types of surface features have a negative impact on inversion layer charge transport and affect the reliability of the gate oxide [84]. However, when the silane overpressure process was used to anneal an identical implanted wafer (T = 1,600°C), no step bunching was observed (see Figure 4.14).

The basic principle behind the silane overpressure annealing process is as follows. When the SiC wafer is annealed at high temperatures (≥ 1,600°C), Si atoms on the surface of the SiC wafer may be exchanged with Si atoms provided by the silane gas in the vapor phase. Chemical process calculations were performed for various pressures and silane flow rates as a function of temperature. These calculations,

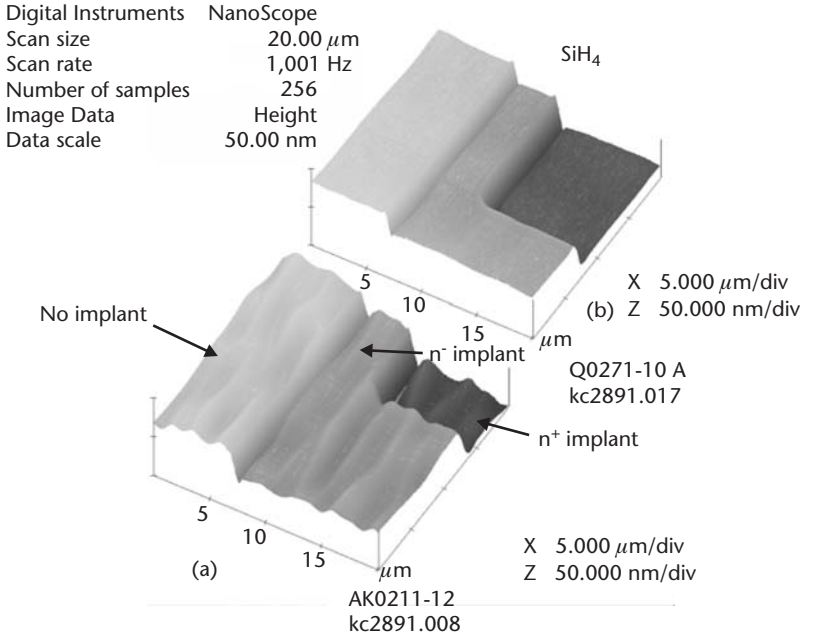


Figure 4.14 AFM images of the LDMOS structures. (a) Sample annealed at 1,600°C in the presence of Silane. (b) Sample annealed at 1,600°C in the presence of Ar.

which support the working model of the silane overpressure process, and the experiments conducted based on these calculations are presented in the following sections.

4.3.2.1 Silane Overpressure Model

This model is based on a very simple premise: if the partial pressure of Si atoms above the SiC surface during annealing is greater than the vapor pressure Si in the SiC matrix, then out-diffusion of Si from the lattice will be suppressed. To theoretically obtain the most suitable conditions for Silane overpressure annealing, a model was constructed by J.T. Wolan at the University of South Florida to calculate both the vapor pressure of Si in SiC and the partial pressure of Si as a function of annealing temperature and gas pressure [85].

Calculations performed by Wolan et al. of the calculated values of vapor pressure of SiC for temperatures of interest for implant annealing have been reported in the literature and the reader is referred to these calculations for completeness [85]. From these calculations it was determined that the required vapor pressure of SiC at lower temperatures (< 1,600°C) is very small, as expected. The relationship between vapor pressure, V_p, and temperature, T, is exponential. Hence an exponential curve fit was applied for vapor pressure calculations for temperatures less than 2,500°C. To optimize the process, the silane flow rates were calculated for various annealing temperatures and process pressures. The partial pressure of silane and the vapor pressure of SiC obtained in Section 4.3.2 under atmospheric pressure (AP) conditions are used here as the reference values. All of the calculations were performed based on initial annealing experiments conducted at 1,600°C with silane (20 sccm) and argon (6 slm) as the process gases. (These experimental conditions will be discussed next.)

It can be observed from Figure 4.15 that the predicted flow rate of silane increases exponentially as the anneal temperature is increased, as expected. This is due to the exponential increase in Si vapor pressure as a function of temperature, which was previously discussed. Similarly, calculations were performed to determine silane flow rates for different process pressures starting from 10 Torr to atmospheric pressure (760 Torr) as a function of annealing temperature. The partial pressure of silane at 1,600°C was recalculated at different pressures and then substituted into our empirical model to determine the partial pressure at different

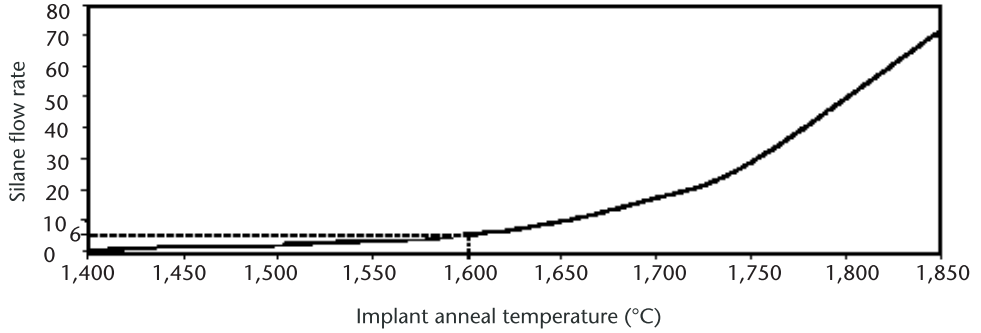


Figure 4.15 Plot of calculated silane flow rate versus implant annealing temperature for various temperatures in the range of 1,400–1,850°C. Dotted line indicates the empirical reference value of 6 sccm at 1,600°C.

temperatures [85]. The flow rate of silane was calculated by equating the calculated partial pressure of silane to the ratio of the flow rates of the process gas and the obtained values are plotted in Figure 4.16. From Figure 4.16 it can be seen that as the pressure is reduced there is a considerable decrease in the required flow rate of silane over an annealing temperature range of 1,400–1,850°C.

4.3.2.2 Implant Annealing Experimental Results

A silane-based CVD reactor suitable for performing high-temperature anneals in an Si- rich ambient was used for these experiments [86]. The samples were placed on a SiC-coated graphite susceptor and an RF induction coil used to heat the susceptor to temperatures on the order of 1,600–1,800°C. Silane and argon were the two process gases used, where Ar not only serves as a dilutant gas but also as a carrier gas to transport silane molecules to the crystal surface. All the implant annealing experiments were performed at atmospheric pressure.

Several 4H-SiC samples with n-type and p-type epitaxial layers of approximately 5 μm in thickness and doping densities in the mid-10^{15} cm^{-3} range were ion-implanted with Al and C, respectively. The Al ion-implantation profile used in these experiments is shown in Figure 4.17. Implants were carried out at 700°C through a 110-nm Mo mask layer in order to implant the near-surface regions of the SiC epilayers. Following the ion implantation, the Mo mask layer was etched away and the samples cleaned. The samples were characterized using RBS and AFM, as shown in Figure 4.18. From the AFM micrograph [see Figure 4.18(b)] it can be seen that the surface of the epilayer grown on top of the SiC samples was degraded after implantation. However the bulk crystalline quality was preserved, as indicated by the RBS ion channeling spectra shown in Figure 4.18(a).

The annealing process was experimentally optimized using Silane in Ar [3% Silane in 97% ultra-high purity (UHP) Ar)]. Initial experiments were conducted with palladium-purified hydrogen as the carrier gas. Unfortunately, this method

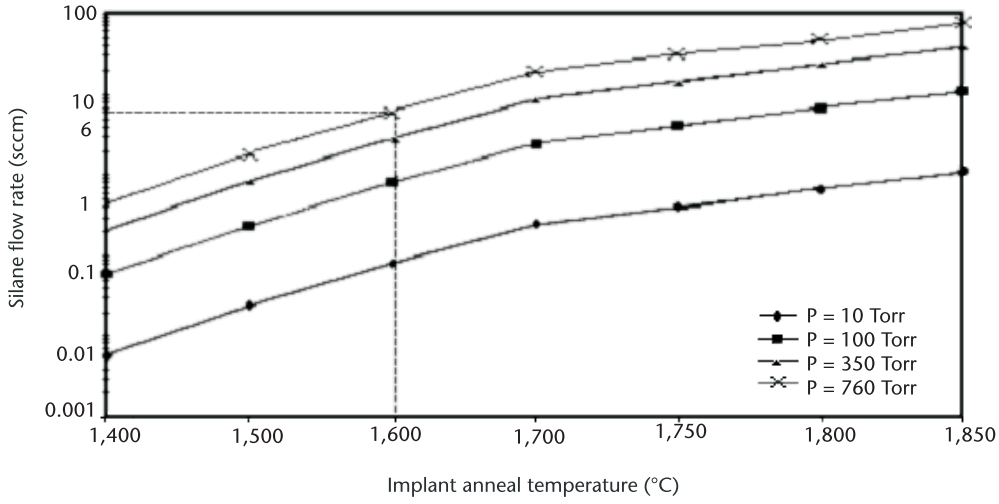


Figure 4.16 Plot of calculated silane flow rate versus implant annealing temperature as a function of process pressure. Dotted line indicates the empirical reference point of 1,600°C, 6 sccm, and 760 Torr.

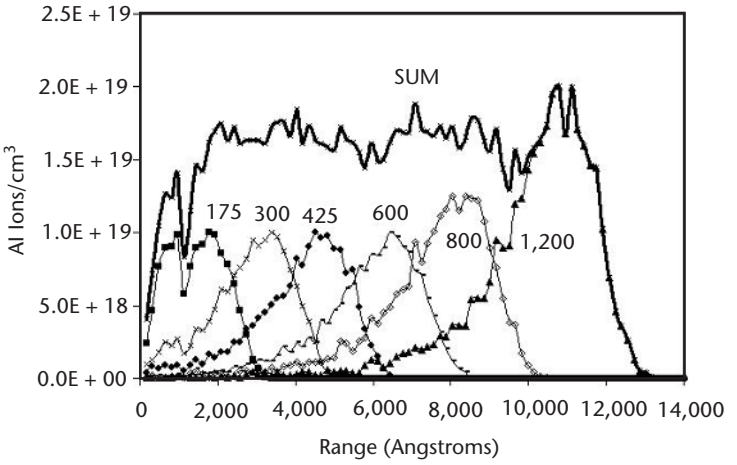


Figure 4.17 Ion implantation depth profile as calculated by SRIM. Al was implanted at 700°C. Multiple implants starting at 175 keV were used to achieve the box profile. (*From:* [87]. © 2000 Trans Tech Publications Inc. Reprinted with permission.)

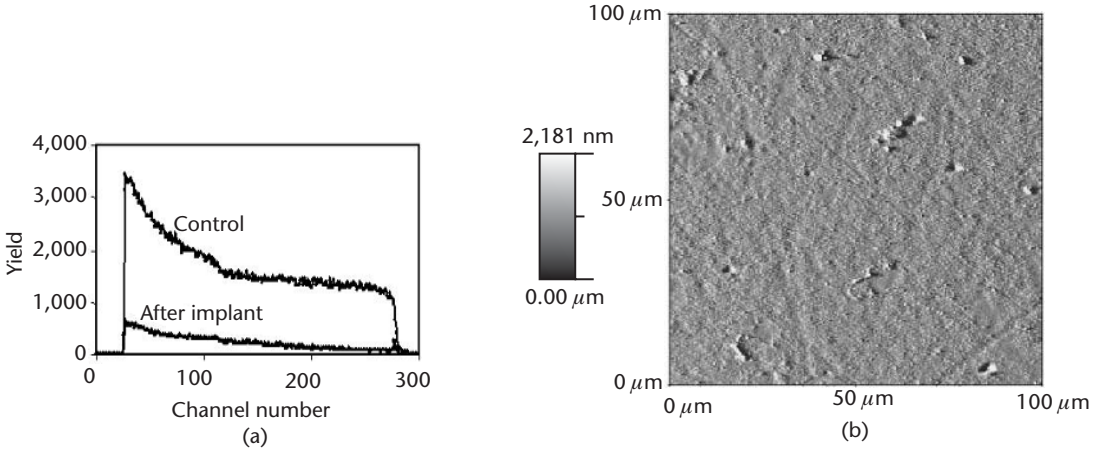


Figure 4.18 (a) RBS and (b) AFM data of 4H-SiC implanted with Al at 700°C. Note the crystal quality is degraded due to implant damage, as expected. RBS and AFM data are courtesy of, respectively, Dr. Tami Isaac-Smith from the group under Professor John Williams at Auburn University and Dr. A. J. Hsieh of the Army Research Laboratory.

proved to not be repeatable, as H_2 is known to etch SiC at temperatures required to anneal the implants [9]. Due to this enhanced etching of the off-axis substrate surface, severe step bunching was observed after annealing in hydrogen, as shown in [9]. Since Ar does not etch SiC, it was used instead of H_2 as the carrier/dilutant gas, since it is capable of transporting Si atoms to the crystal surface without simultaneously etching the surface. This Ar-based process proved to be very stable and robust.

The final implant annealing process schedule developed during this research is shown in Figure 4.19. A 6-slm UHP Ar flow is first established in the reactor. When the RF generator is turned on, the susceptor is heated to the annealing temperature (typically 1,600°C) using a controlled thermal ramp. To avoid the formation of Si droplets, silane is not introduced into the reactor until a substrate temperature of 1,490°C is reached. At that time the premixed silane in Ar gas is introduced into the Ar carrier flow at a flow rate of 20 sccm. All flows are controlled using calibrated

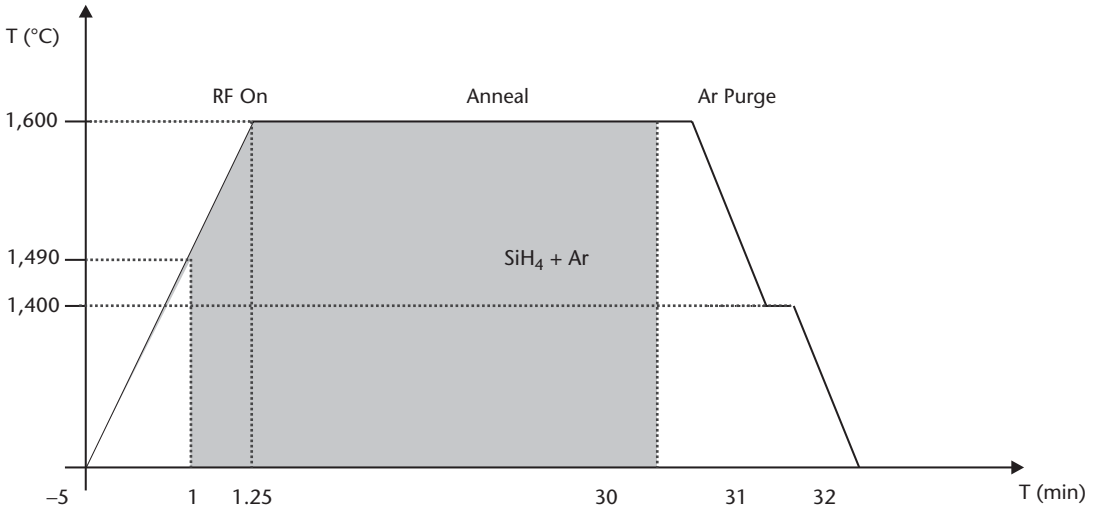


Figure 4.19 Implant annealing process schedule indicating gas flow timing versus sample temperature.

mass flow controllers to ensure process repeatability. Once the desired temperature is reached, the annealing begins. After 30 minutes at the anneal temperature the premixed Silane in Ar is turned off and the set point temperature is changed to 1,400°C (6 slm UHP Ar flow remains on). After one minute of Ar flow at 1,400°C, the RF generator is turned off and the sample is cooled down to RT under continuous Ar flow. This same process was used for both the Al and C implanted samples to ensure process stability.

After annealing the samples were characterized using channeling RBS and AFM. Figure 4.20 shows that the surface morphology of the Al-implanted n-type 4H-SiC samples was not affected during the annealing process. This indicated that a sufficient overpressure of Si was likely present during annealing. The surface chemistry of air-exposed samples after annealing was also evaluated with the help of XPS, as shown in Figure 4.21. From the figure it can be seen that, with the exception of oxygen, which is a form of SiO_2 at the surface, elemental surface and near-surface species are exclusively composed of Si and C, indicating that after the annealing process the bulk species were preserved [87].

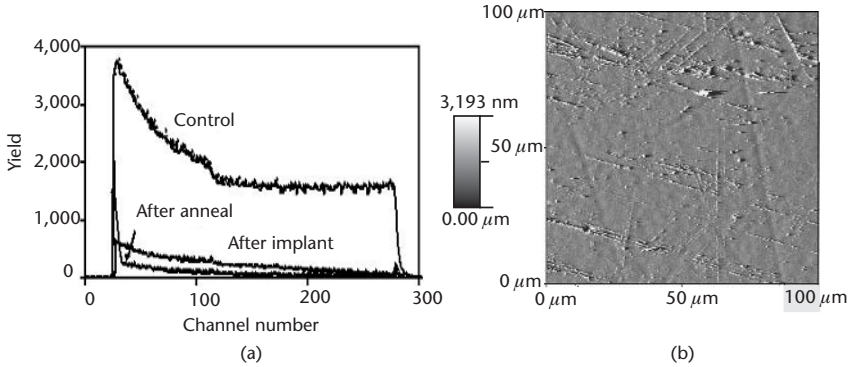


Figure 4.20 (a) RBS and (b) AFM data of 4H-SiC implanted with Al, annealed using Silane/Ar process. Note crystal damage from implant has been repaired.

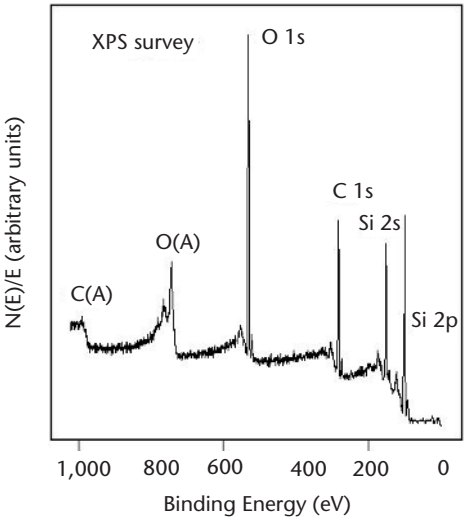


Figure 4.21 XPS survey obtained from a C-implanted p-type 4H-SiC epitaxial layer after a 1,600°C anneal. Besides the presence of O in the form of SiO_2, the surface consists primarily of Si and C. The XPS data and analysis are courtesy of Dr. J. T. Wolan at the University of South Florida.

4.3.3 Implanted Ion Profiles After Annealing

This section reviews the published data about diffusion phenomena of implanted species in SiC upon annealing treatments and the processes proposed to control such diffusion phenomena.

Depending on the implanted species, high-temperature thermal treatments might modify the profile shape of the as-implanted atoms and produce an important out-diffusion of these atoms from the implanted region. In particular, the SiC literature agrees on the formation of very deep tails in the unimplanted bulk region for B implantations, independent of SiC polytype and implantation temperature [88–90]. B redistribution within the implanted region and out-diffusion from the sample surface has been measured by some authors [88, 90] but it is not always seen [89, 91]. Important diffusion phenomena were also measured at the trailing edge of the N profiles for implantation processes in p-type B doped wells produced by ion implantation in 4H-SiC [91]. No diffusion was ever measured for N implanted in p-type Al-doped SiC crystals [92], nor for Al or P implanted in 4H- or 6H-SiC samples and thermally treated at 1,700°C for 30 minutes [88, 93, 94].

Figure 4.22 presents some recent results concerning the diffusion of implanted B in 4H-SiC as a function of annealing temperature and doping type and density of the nonimplanted 4H-SiC. Similar results for the 6H-SiC polytype can be found in the literature [88, 93]. Depending on the annealing temperature, the samples shown in Figure 4.22 were thermally treated in a vacuum furnace (base pressure 10^{-7} Torr), in an inductively heated furnace within an Ar ambient, or in a vapor phase reactor system with a controlled SiH_4 flux. The SIMS B profiles shown in Figure 4.22 were measured for two different sets of samples. One set was treated by a single-energy implantation process at RT [3] and the SIMS spectra are shown in Figure 4.22(a, d). The other set of samples was processed with a multiple-energy implantation process at 500°C [90] and the SIMS profiles are shown in Figure 4.22(b, c). These last samples were also implanted with Al over a depth half that of the implanted B [90].

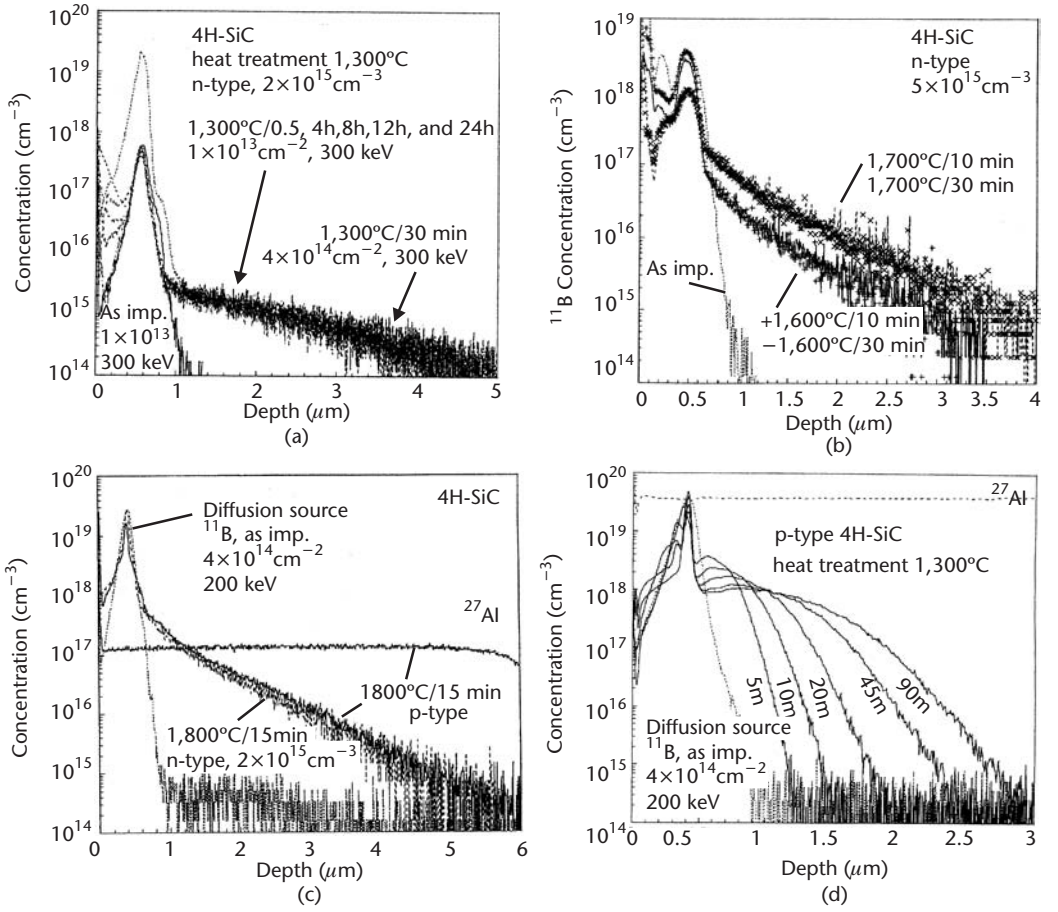


Figure 4.22 Comparison between as-implanted and annealed B chemical profiles in 4H-SiC measured by SIMS spectrometry. (a) n-type 4H-SiC crystals and shows the evolution of single-energy B profiles versus 1,300°C annealing for various times; samples implanted with two fluency values that differ more than one order of magnitude are taken into account. (b) n-type 4H-SiC crystals and shows the evolution of the same multiple-energy B implantation profile versus annealing at 1,600°C and 1,700°C for two different annealing times. (c) A single-energy implantation process and shows the B diffusion versus equal annealing processes but different doping type in the 4H-SiC crystal. (d) A p-type heavy-doped 4H-SiC and shows the diffusion of single-energy B implanted profiles versus 1,300°C annealing temperature and various annealing time. Details about the implantation and annealing parameters as well as the as-grown doping density values of the 4H-SiC material are shown in the inset of the figure. (*From:* [3]. © 2003 Material Research Society. Reprinted with permission.)

Despite such differences in sample preparation, the trend of the B profile is confirmed by several other publications [88]. The redistribution and loss of B within the implanted region strongly depends on the annealing temperature and time, as is very evident in Figure 4.22(b). The B out-diffusion from the implanted layer toward the unimplanted crystals is an enhanced process with a transient component, as shown in Figure 4.22(a–c), but normal (i.e., Fickian, B diffusion) as shown in Figure 4.22(d) also occurs. In the temperature range 1,300–1,800°C, the transient phenomenon gives B profiles with exponential shape, as deep as 5–6 μm in the nonimplanted 4H-SiC crystal, and a B peak concentration that decreases for increasing annealing temperature [Figure 4.22(a–c)]. For much higher (2,000°C) annealing temperatures, the B tails have a Gaussian shape [3]. The presence of an Al p-type

doping in the 4H-SiC crystal changes the B diffusion behavior depending on the annealing temperature and on the Al concentration. In particular, for p-type doping in the range of 10^{17} cm^{-3}, the deep exponential diffusion is seen for 1,800°C [Figure 4.22(c)] but not for 1,300°C [3]. In 4H-SiC crystals Al-doped with a concentration $\geq 4 \times 10^{19}$ cm^{-3}, the enhanced diffusion is not effective at temperatures in the range of 1,220–1,600°C, as results described in [3] demonstrate. One of those results is shown in Figure 4.22(d), where it should be compared with the B diffusion profiles of Figure 4.22(a), also a 1,300°C annealing. Out-diffusion phenomena like those in Figure 4.22(d) have a Gaussian shape and, within the sensitivity of the SIMS technique, contain a constant B amount for increasing annealing time, at least in the temperature range 1,300–1,600°C. The analysis of the temperature and time evolution of these B diffusion tails in the frame of Fick's second law was presented in [3]. The temperature dependence of the extracted diffusion coefficient contains an activation energy equal to –5.3 eV, in the case of p-type 4×10^{19} cm^{-3} 4H-SiC. Such a value is comparable with those derived by Mokhov and coauthors in experiments done in the 1980s [94–97], although the pre-exponential term in the diffusion coefficient expression derived for B-enhanced diffusion is a few orders of magnitude higher with respect to those derived in Mokhov's experiments [95–97]. In conclusion, the out-diffusion of B from the implanted layer toward the nonimplanted SiC crystal is a combination of transient (i.e., out of equilibrium) and enhanced diffusion mechanisms and may in n-type SiC be classified as a transient enhanced diffusion (TED) process similar to what has been reported for B diffusion in Si.

The TED of B in SiC is believed to depend on a nonequilibrium concentration of native point defects produced by the ion implantation process. Taking inspiration from the deep knowledge of B TED in Si [98], the following hypothesis was made that B atoms might diffuse in SiC by substituting Si atoms kicked out from their sites. If this would be the case, interstitial Si would be the native defect controlling the B TED in SiC. With the aim to suppress the oversaturation of Si interstitials during annealing, B-implanted SiC samples were coimplanted with C ions [99] or were preannealed at low temperature (900°C) for a long time (2 hours) [100]. In fact, C atoms may also diffuse in SiC by a kick-out mechanism controlled by Si interstitials [101], as they do in Si [98]. The annealing at 900°C should favor the recombination of Si interstitials and Si vacancies, assuming that also in 6H- and 4H-SiC such native defects recombine at 800°C as they are known to do in 3C-SiC [101]. In both cases it is expected that the thermal equilibrium concentration and the diffusion coefficient of interstitial atoms in SiC would be controlled. Even if such a mechanism has not yet been confirmed, both C coimplantation and 900°C preannealing reduced the B out-diffusion from the sample surface and the B TED tail in the nonimplanted SiC crystal, as can be seen in the SIMS spectra shown in Figure 4.23. These figures refer to both 4H- and 6H-SiC crystals and show the modification of the B as-implanted profile versus annealing at 1,700°C when the B implantation is the only process performed [Figure 4.23(a)], when C and B are coimplanted with equal and overlapping profiles [Figure 4.23(b)] and when the sample is preannealed at 900°C for 2 hours [Figure 4.23(c)]. The comparison between Figure 4.23(a) and Figure 4.23(b, c) shows that C coimplantation actually reduces the B out-diffusion from the sample surface and eliminates the B TED tail, whereas the 900°C preannealing mostly limits the B out-diffusion from the sample surface but a TED tail is still present, the

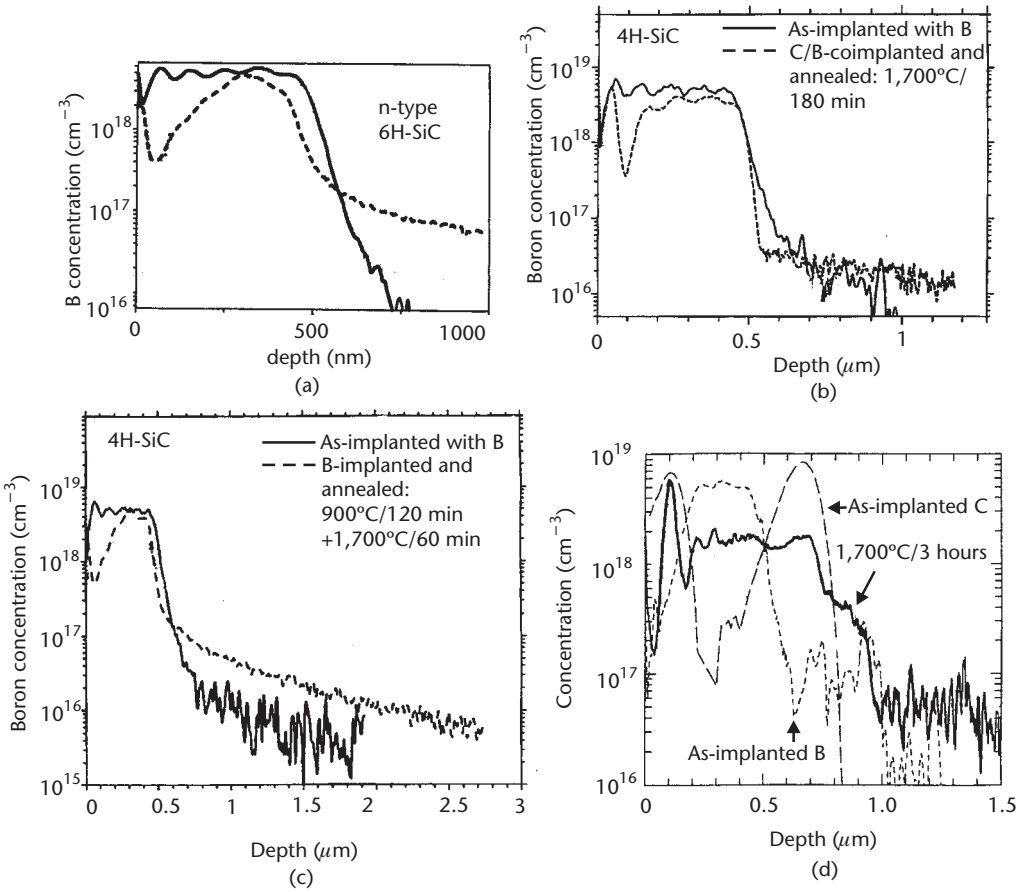


Figure 4.23 Comparison between SIMS as-implanted and 1,700°C annealed B profiles. (a) 6H-SiC, multiple-energy B implantation and 30-minute annealing. (*From:* [99]. © 2000 Material Science Forum. Reprinted with permission.) (b) 4H-SiC, multiple-energy C and B coimplantation and 30-minute annealing time. (*From:* [100]. © 1999 American Institute of Physics. Reprinted with permission.) (c) 4H-SiC, multiple-energy B implantation, 900°C 2-hour preannealing and 60-minute annealing. (*From:* [100]. © 1999 American Institute of Physics. Reprinted with permission.) (d) 6H-SiC, multiple-energy B buried implanted profile sandwiched between two C single-energy implanted profiles and 180-minute annealing. (*From:* [102]. © 2001 Material Science Forum. Reprinted with permission.)

magnitude of which is comparable with those shown in Figure 4.22(b). The diffusion of a buried B implanted profile sandwiched between two C implanted profiles is shown in Figure 4.23(d); after 3 hours of annealing at 1,700°C, most of the implanted B is redistributed across the depth defined by the as-implanted sandwich profiles.

In Figure 4.24(a), the SIMS profiles measured for as-implanted and for 1,600°C 10-minute annealed 4H-SiC samples coimplanted with N and B ions are shown [91]. These N and B profiles correspond to the case of an n-type region embedded in a p-type one, both of them produced by ion implantation. For increasing temperature and/or annealing time the B TED tail does not change, with respect to that shown in Figure 4.24(a), but the N tail dramatically increases approaching the trailing edge of the B profile, as described in [91]. The same authors also showed that reference samples implanted with only N present a negligible diffusion tail in the

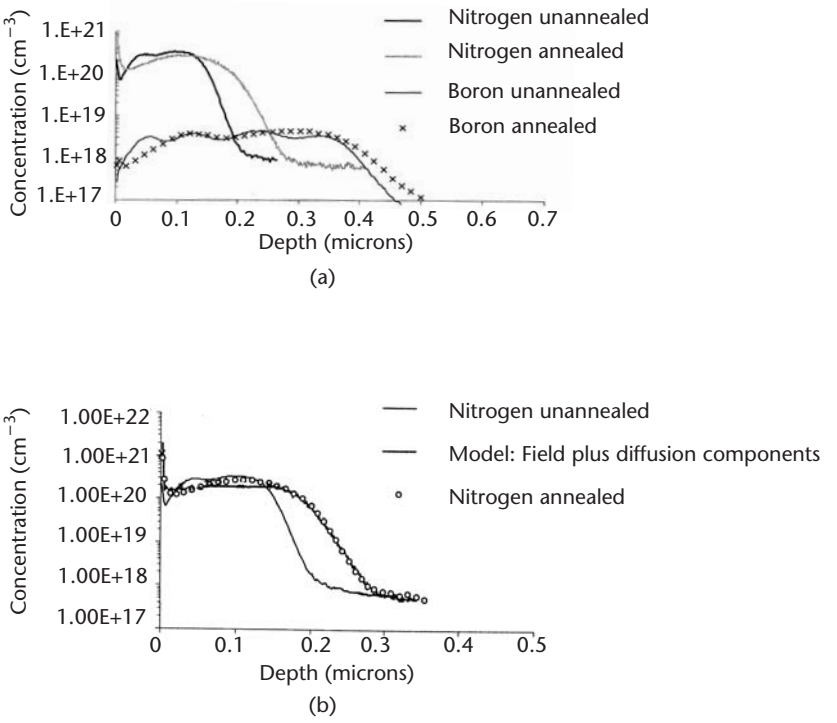


Figure 4.24 N and B coimplanted in 4H-SiC and annealed in an inductively heated furnace at 1,600°C for 10 minutes within a SiC crucible and high-purity Ar atmosphere. (a) Comparison between as-implanted and annealed N and B profiles. (b) Comparison between the N annealed and simulated profile; these were computed under the hypothesis of an N FED diffusion. (*From:* [91]. © 2002 Material Science Forum. Reprinted with permission.)

unimplanted n-type 4H-SiC [91]. Such a result is in agreement with all previously published N SIMS data in the SiC literature. The same authors hypothesized that such huge N tails might be explained by the presence of an electric field across the trailing edge of the N profile and by charged mobile defects. The electric field would be due to the ionized donor and acceptor profiles present in the sample, which were assumed to be the N and B profile concentration that, as can be seen in Figure 4.24(a), are always higher than the bulk doping concentration in 4H-SiC at any annealing temperature in the 1,600–1,700°C range ($\cong 10^{17}$ cm^{-3}). The same ionized donors and acceptors were assumed to be the mobile defects. The N diffusion in the static field from charged donors and acceptors was solved and the N profile was simulated with very good precision, as shown in Figure 4.24(b). In conclusion, these recent results about diffusion of implanted species in SiC show that electric field components also have to be taken into account to model the implanted dopant diffusion in SiC during electrical activation annealing. This phenomenon is called field-enhanced diffusion (FED).

4.3.4 Defect Evolution

As described in Section 4.2.1, ion implantation damage is conveniently investigated by RBS-C and a substantial body of results is now available for SiC. From these data

it is clear that amorphization of the SiC should be avoided, since it is very difficult or even impossible to anneal such highly damaged crystals [103]. Instead, the damage level caused by the implantation should be kept low, for instance by using a proper combination of elevated temperatures and ion flux during the process, or perhaps also by using channeled implants. When annealing of sub-amorphous damage is studied by RBS-C the damage levels can be seen to approach virgin material already at annealing temperatures of 1,200°C. However, it is important to remember that there is still a considerable amount of damage left, even if it is not possible to resolve it with RBS-C. PAS makes it possible to detect vacancy type defects, in contrast to the interstitial types monitored by RBS-C. With PAS it is also possible to detect vacancy concentrations several orders of magnitude lower than the interstitial concentrations seen by RBS-C and to identify individual defects, such as divacancies. In fact, for a further understanding and improvement of the annealing processes, it is not sufficient to study the integrated damage seen by RBS-C. Instead this damage should be resolved into individual defects with techniques like PAS. An example of PAS results from annealing of He-implanted 4H- and 6H-SiC is given by Kawasuso et al. [104]. Several annealing stages can be clearly resolved by monitoring the so-called S-parameter as a function of annealing temperature and these are assumed to be related to the disappearance of monovacancies between 500–700°C and the formation and annealing of larger vacancy agglomerates between 900–1,500°C. No difference between the polytypes can be seen. Interestingly, the authors of [104] have also been able to correlate the latter annealing stage of the S-parameter with the annealing of deep levels measured by DLTS. Such correlations of different techniques are invaluable for finally identifying the intrinsic point defects in SiC.

4.3.4.1 Dislocation Loops

It has been shown by TEM that interstitial-type of defects are formed upon annealing of implanted SiC [5, 6, 105]. Most of the interstitials and vacancies recombine during annealing, but a part of the self-interstitials form secondary defects in the form of circular planar defects residing on the basal planes of 4H (and also 6H) SiC, surrounded by dislocation loops. The size of these defects is typically 1–10 nm, and it has been suggested by Ohno that several different types exist [105]. The situation is further complicated because these disks have been shown to increase in size with increasing annealing time and temperature until a saturation is reached. After this saturation, which presumably means that most of the remaining interstitials are bound in these basal plane defects, the defects undergo a conservative Ostwald ripening process: The smaller disks tend to become smaller, whereas the larger disks grow even more, keeping the total number of interstitials bound in the loops constant. This is highly undesirable from a device point of view and leads to lattice strain, instability, and inhomogeneous device properties.

The formation of disks appear to be more strongly dependent on Si than C interstitials, since experiments with ions substituting for C, yielding a larger amount of interstitial C, gave smaller and fewer loops, whereas implantations with ions known to substitute for Si gave larger and more prominent loops [106]. In Figure 4.25, we show the evolution of the fractional area covered by disks seen in plain-view TEM as a function of annealing parameters. This 4H epitaxial sample has been implanted

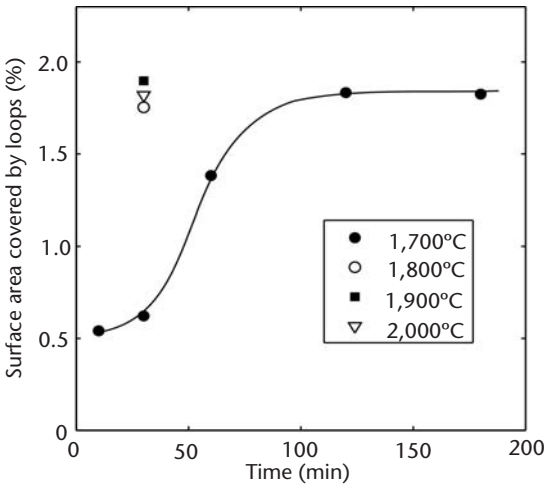


Figure 4.25 Growth of the planar defects (dislocation loops) as a function of annealing conditions. The total area covered by the defects saturates at about 1.8% of the total surface area studied by TEM.

with 180 keV Al ions to a dose of 2.6×10^{14} cm^{-2} and at an implantation temperature of 600°C. The saturation level amounting to 1.8% area coverage for the 1,700°C anneal is clearly seen after 120 minutes. Annealing at 1,800°C, 1,900°C, and 2,000°C for 30 minutes all yield the same saturation level. In the investigated dose interval there was a direct linear relation between the Al dose and the fractional area covered by loops. Assuming that the disks consist of a monolayer of Si with the same area density as the SiC *c*-plane, the number of Si interstitials bound within the loops is about 20–30% of the implanted ions. While there seems to be a remedy for surface decomposition by carefully optimizing the ambient conditions during anneal and/or by capping the surface, as further described in Section 4.3.1, the growth of these extended defects is a problem that presently sets an upper bound for the postimplant annealing process.

4.3.4.2 Precipitates and Dopant Solubility

The solubility of dopant atoms sets an upper limit to how many ions can be incorporated in the SiC lattice as dopants. For higher fluences the dopants tend to form precipitates rather than occupy substitutional sites and this can be a problem, particularly for acceptor doping, since the large ionization energies for common p-type dopants necessitate very high concentrations of implanted atoms. Early work by Mokhov and Vodakhov [107] have recently been upgraded and expanded by work of Linnarsson et al. and solubility for B [3] and Al [13] are now well established in epitaxial material. However, it should be noted that the solubility in implanted material may be very different from epitaxial and the results from epitaxially doped material may be regarded as ideal upper limits. Figure 4.26 shows the solubility limit of Al in 4H-SiC epitaxial layers as a function of reciprocal temperature. The data have been obtained by measuring the out-diffusion of Al from an oversaturated region using SIMS. At a temperature of 1,900°C, the solubility limit is shown to be 2×10^{20} cm^{-3}, which could be compared with the solubility limit for B at

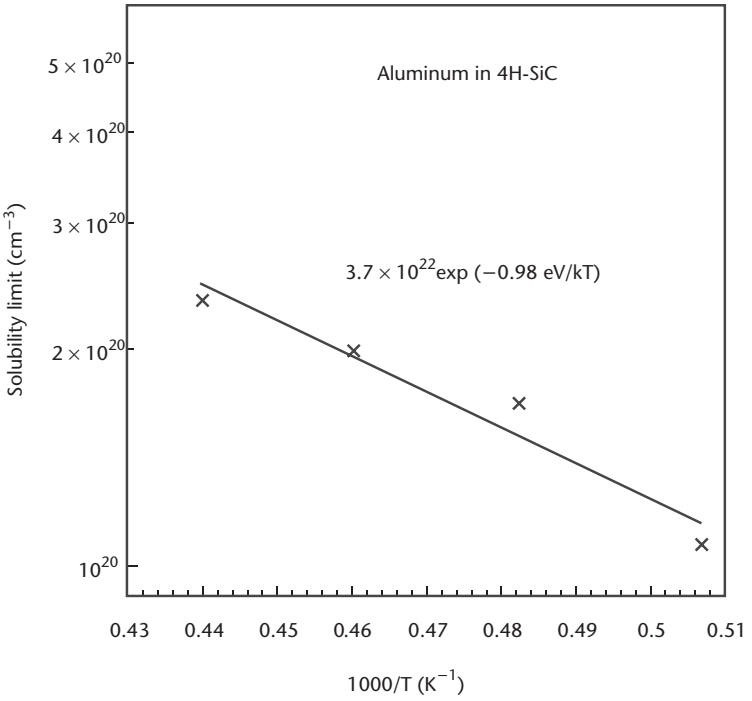


Figure 4.26 The solubility limit for aluminum versus reciprocal temperature as extracted from SIMS measurement of out-diffusion from heavily doped 4H-SiC [13].

this temperature, which is 4×10^{19} cm^{-3} [3]. The region oversaturated with Al has furthermore been shown to contain Al-precipitates, both by using SIMS imaging techniques and TEM. These precipitates are three-dimensional and have a typical extension in the *c*-plane of 30 to 300Å and a thickness of about 40Å. The most likely compositions of the precipitates are the ternary phases Al_4SiC_4 or $Al_4Si_2C_5$.

For donor dopants (i.e., nitrogen and phosphorus), the results are not as clear yet. Nitrogen solubility (at 2,150°C) of 6×10^{20} cm^{-3} has been reported by Vodakhov et al. [108], but Schultz et al. [109] have more recently indicated that already at concentrations higher than 3×10^{19} cm^{-3} nitrogen starts to form electrically inactive precipitates. For phosphorus, the situation is somewhat opposite. Vodakhov has reported very low solubility, 2.8×10^{18} cm^{-3} at 2,150°C [108], but more recent measurements have shown that much higher concentrations are actually electrically active, as described next [110]. A common opinion seems to be that nitrogen is ideally suited for implantations up to concentrations of ~10^{19} cm^{-3} because of its low mass, which gives low damage levels and consequently requires lower anneal temperatures. For higher doping concentration N seems to be difficult to activate and P implantation may then offer an alternative, but clearly more work is needed before an understanding of these phenomena is at hand.

4.3.5 Results of Electrical Activation

One problem, when evaluating dopant activation, is that we can only measure secondary effects of the electrically active dopants. The chemical concentration of

dopants can readily be monitored by SIMS, but the activated fraction of the dopants is best monitored by their contribution to the electrical properties of the material. Either the ionized acceptors or donors are accessed by, for instance, capacitance-voltage measurements, or the mobile electron or hole concentrations are studied by Hall effect or resistivity measurements. To obtain the concentration of activated dopants from these electrical measurements we then need to know parameters such as ionization energy, deep states/compensating charges, effective masses in various directions, and charge carrier mobilities. Many of these parameters have not yet been established even for the most common polytypes of SiC.

The evaluation of activation in implanted material introduces two additional difficulties in comparison to grown samples with homogeneous dopant concentrations. First, many of the measurement techniques are not directly applicable to the highly graded dopant concentrations resulting from ion implantation. The analysis therefore tends to become very complicated, or even impossible to use. Second, the implantation will introduce defects that may compensate the acceptors or donors and also affect the mobility. One remedy for the strong-concentration gradients is to implant so-called box profiles consisting of implantations with several energies where the fluence is adapted for each energy value to give a constant peak concentration. By closely spacing the different implantation energies it is possible to create a nearly constant dopant concentration from the surface to a depth sufficient for the measurement. The second problem is more difficult to deal with in an adequate way and normally we need to make assumptions about the defects still present after the annealing and their influence on the electrical properties of the material.

In some applications very high doping levels are needed. For instance, to form ohmic contacts, or source and drain regions of transistors, doping concentrations above 10^{20} cm^{-3} may be required. In such situations the semiconductor becomes degenerate and a number of additional effects will occur that make the charge carrier statistics very complicated. In addition, other types of conductivity may contribute to the charge transport and standard evaluation tools are no longer applicable.

Making comparisons between literature data using different measurement techniques is therefore many times not possible. In addition, there is the problem with surface decomposition at higher annealing temperatures, discussed in Section 4.3.1, that may strongly affect the formation and reproducibility of electrical contacts produced on implanted and annealed material. In this section we will nevertheless try to evaluate and compare recent achievements in this important field and describe a selected number of recent results on activation studies on both donors and acceptors.

4.3.5.1 Donors

Donor ions have been somewhat neglected and one reason may be that the considerably smaller ionization energies reduce the importance of having full activation of implanted donor atoms; research has therefore been concentrated on the acceptors. Another reason may also be that many of the expected SiC bipolar power-device applications require a thick low-doped n-type drift region grown by CVD in combination with a p-type emitter preferably manufactured by implantation. However, many transistor applications and also contacts to n-type material benefit from

n-type implants and recently there has been a renewed interest in nitrogen and phosphorus implantations.

Hall measurements on low-dose nitrogen-implanted n-type 6H layers have been shown by Saks et al. to yield nearly ideal characteristics already at annealing temperatures of 1,400°C [111]. The implanted nitrogen concentration was about 10^{17} cm^{-3} and the compensation level due to residual defects was only 1.5% of the donor concentration. Although attempts with 4H-SiC were not as promising [112], these results clearly show that implantation of donors at low concentrations are today not a major problem for SiC device applications. It is when the donor concentrations approach the 10^{19} or 10^{20} cm^{-3} ranges that problems with poor activation and high concentration of compensating defects start to appear. One interesting example of how to cope with these difficulties at higher donor concentrations is implantation of phosphorus ions into the *a*-planes of 4H-SiC crystals. The benefit, compared with the more standard implantations at a few degrees off of the *c*-axis, is that considerably lower damage levels are reached, and also that surface decomposition could be avoided. In a letter by Negoro et al. [113] P implantations along the [11–20] and [0001] directions are compared. It is reported that implantation along the former direction gives a sheet resistivity at RT as low as 27 Ω/□ after annealing up to 1,700°C for 30 minutes. This was three times lower resistivity than the similarly treated samples implanted in the c-plane. Schmidt et al. [114] also reports on phosphorus implantation in 4H Al-doped SiC epilayers employing the same two different directions for the implant. He also uses box profiles with a maximum concentration in the 10^{20} cm^{-3} range and reports a nearly complete activation of the implanted P ions for 1,700°C annealing over 30 minutes. The best resistivity values obtained in this study are in fact nearly identical with the previous report, 29 Ω/□, but a key point is that the same value is reached for implants in both the [11–20] and [0001] directions. Unfortunately, none of the authors comment about channeling effects or give enough details about the sample orientation during the implantation to make it possible to estimate this effect. According to what has been discussed in Section 4.2.3, channeling may explain why the two groups obtained different values for the "on-axis" implants, but the low resistivity values and high activation are nevertheless important achievements.

It is generally accepted that nitrogen forms a donor state when substituting for carbon in the SiC lattice. Phosphorus, on the other hand, seems to form a donor on substitutional Si sites [115]. This opens up an interesting application of coimplantation using N- and P-implantations to reach higher concentrations of free electrons; nitrogen donors on C-sites and phosphorus donors on Si-sites. This idea was tried by Gardner et al. [116] with some success, but more recently Laube et al. [110] showed that even lower resistivity values are obtainable with this method. However, Laube also showed that a still higher degree of activation could be achieved by phosphorus implantation alone. Both authors compared N, P, and (N + P) implanted box profiles with mean concentrations in the range of 10^{18}, 10^{19}, and 10^{20} cm^{-3}, all annealed at the frequently used conditions of 1,700°C for 30 minutes. Using Hall effect measurements, Laube showed that while phosphorus reached full activation even above 10^{20} cm^{-3}, the nitrogen activation saturated below 3×10^{19} cm^{-3}. Sheet resistivity value at RT for the highest phosphorus concentration was reported to be 35 Ω/□, which is also in agreement with what has been reported in [113, 114].

4.3.5.2 Acceptors

For implanted acceptor activation there have been several reviews during the last few years since Troffer et al.'s often-cited paper on boron and aluminum from 1997 [88]. Aluminum is now the most-favored choice of acceptor ion despite the larger mass, which results in substantially more damage compared with implanted boron. Mainly it is the high ionization energy for boron that results in this choice, as well as its low solubility. In addition, boron has other drawbacks, such as an ability to form deep centers like the D-center [117] rather than shallow acceptor states and, as shown in Section 4.3.2, boron ions also diffuse easily at the annealing temperatures needed for activation. The diffusion properties may be used in a beneficial way, although it is normally more convenient if the implanted ion distribution is determined by the implant conditions alone.

That the effective hole masses, or the density of states, is a complicated matter in SiC is well described in a review by Gardner et al. [118]. This article treats in some detail the valence band and estimates the contribution from the three top-most bands to the density of states, including the temperature dependence. Using the estimated effective mass the authors attempt to calculate the activation (i.e., the ratio of implanted and electrically active Al ions), and they achieve an activation of 37% of the implanted Al concentration of 10^{21} cm^{-3} after an anneal at 1,670°C for about 10 minutes.

Heera et al. compare a number of reported resistivity values for Al and conclude that although Al is superior to boron in most applications, it is still not possible to reach resistivity values lower than 0.05 Ω-cm at RT as long as thermally stimulated hole conduction is the dominating process [119]. The limitations are set by the ionization energy and the mobility of holes in SiC. In Figure 4.1, the ionized fraction of Al and B on substitutional (Si) sites is shown as a function of dopant concentration at RT. For the figure, the ionization energies given in Table 4.1 have been used together with an effective hole mass of 1.24 m_e. The advantage with Al can easily be seen, although it should be pointed out that boron may still be useful for applications using SiC devices at high temperatures or under reverse bias.

Two novel measurement techniques, which both belong to the scanning probe microscopy (SPM) family of analysis tools developed from the atomic force microscopy technique, have recently been used for doping measurements in SiC. These are scanning capacitance microscopy (SCM) [120, 121] and scanning spreading resistance microscopy (SSRM) [122, 123]. These techniques are very promising, but they require calibration to yield absolute values of free carrier concentration. SPM is particularly suited for characterization of implanted dopant distributions, since two-dimensional maps with a spatial resolution better than 30 nm is possible. However, it is also more difficult to obtain reproducible results from annealed implanted doping distributions compared with epitaxially grown samples, probably due to implantation damage affecting the surface states and contact properties affected by the annealing process. In Figure 4.27, we show the SIMS profile of an Al multiple-energy implantation as well as the SSRM-measured current. The sample is a 4H-SiC epilayer implanted at 700°C with Al ions using several energies and then annealed at different temperatures. By calibrating the SSRM signal with epitaxial samples with known hole concentration we conclude that the activation of this particular implant is about 2%, although differences in mobility and trap concentration between the

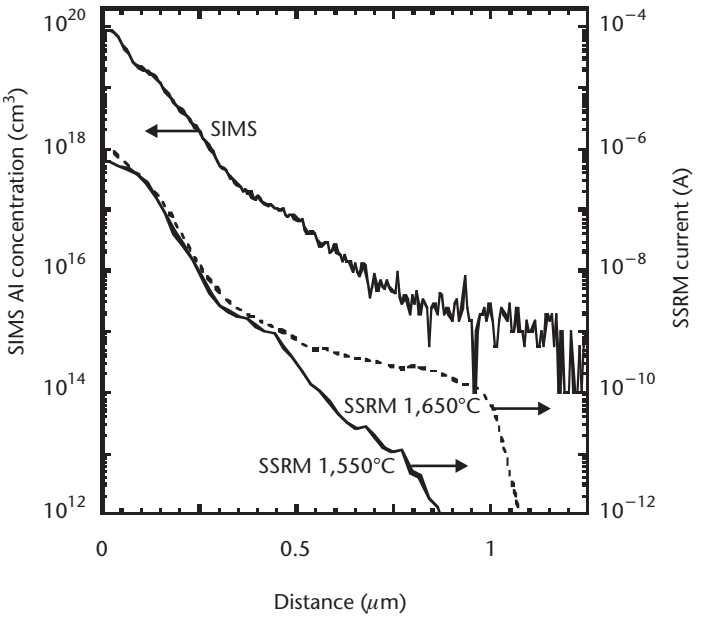


Figure 4.27 Measured SIMS and SSRM current profiles of a multiple-energy implanted 4H-SiC sample. The implanted dopant ion is Al and the activation after two annealing temperatures is shown. (*From:* [122]. © 2003 Material Science and Engineering B. Reprinted with permission.)

epilayer and the implanted sample can affect this value. Two SSRM curves are shown from samples annealed at 1,550°C and 1,650°C for 30 minutes each. The difference is quite small, but a slight improvement in activation can be seen for the higher temperature anneal. This result is in reasonable agreement with other reports on activation in implanted 4H-SiC [118].

A recent result on Al-implanted 4H-SiC, which is in sharp contrast to the common opinion that amorphization should be avoided, has been reported by E. Kalinina from the Ioffe Institute in St. Petersburg [124]. She showed that very good activation could be achieved by RT implantation of Al at doses in excess of 10^{16} cm^{-2}. This completely amorphized material is shown to be fairly well recrystallized by an RTA process that also causes some of the Al to diffuse into the low-doped n-type epilayer, forming the p$^+$n junction at a larger depth than the highly defective implanted area. Nearly ideal forward IV-characteristics were also shown for current densities of several kA cm^{-2}. Even if the stability of such heavily implanted devices may be questioned this result shows that there is still a long way to go before a fully optimized implantation technology is at hand.

4.4 Technology Barriers and Suggestions for Future Work

Ion implantation appears as the only feasible method to accomplish selective area doping of SiC in planar device technology. As described in this chapter, substantial progress has been made during recent years but several fundamental issues and technology barriers remain before the implantation process is fully developed and can be truly implemented in SiC device processing. For instance, mesa-etched p$^+$n-diodes

made by in situ doping during epitaxial growth still exhibit superior current-voltage characteristics compared with most of the ion-implanted p^+n diodes.

Highly doped n^+- and p^+-layers, with a low concentration of residual defects acting as recombination/trapping or scattering centers for charge carriers, are of vital importance for most device structures. For n^+-layers, the major obstacle is to reach dopant concentrations in the 10^{20} cm^{-3} range; here, the recent and promising work on P implantation, instead of the more commonly used N implantation where the maximum carrier concentration obtained is only in the low 10^{19} cm^{-3} range, should be intensified. For p^+-layers it is even more important to reach high concentration of active dopants. Al is found to be superior relative to B, primarily because of a higher solid solubility limit and a shallower acceptor position in the energy bandgap. However, even for Al the ionization energy is relatively large and the fraction of ionized dopants at RT amounts to only a few percent. In addition, residual electrically active defects and poor electrical activation are serious constraints that need to be resolved. Further, a reduction of the postimplant annealing temperature required for the electrical activation is highly desirable to preserve a flat-surface morphology and make the doping process more compatible with other device-processing steps. In this context, issues like coimplantation, implant flux, channeled implants, and multistage postimplant annealing should be explored. Whether channeled implants are viable in SiC device processing or not remains to be seen, but we certainly need to learn more about the fundamentals of scattering cross sections and defect accumulation for channeling conditions.

References

[1] Matsunami, H., et al., "VPE Growth of SiC on Step-Controlled Substrates," *Springer Proc. Phys.*, Vol. 34, 1989, pp. 34–39.

[2] Larkin, D. J., et al., "Hydrogen Incorporation in Boron-Doped 6H-SiC CVD Epilayers Produced Using Site-Competition Epitaxy," *J. Electron. Mater.*, Vol. 24, 1995, pp. 289–294.

[3] Linnarsson, M. K., et al., "Aluminum and Boron Diffusion in 4H-SiC," *Mat. Res. Soc. Symp. Proc.*, Vol. 742, 2003, pp. 291–301.

[4] Poate, J. M., and J. S. Williams, in *Ion Implantation and Beam Processing*, J. S. Williams and J. M. Poate, (eds.), Sydney, Australia: Academic Press, 1984, p. 13.

[5] Jiang, W., et al., "Damage Formation and Recovery in C^+-Irradiated 6H-SiC," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 148, 1999, pp. 562–566.

[6] Capano, M. A., et al., "Dopant Activation and Surface Morphology of Ion-Implanted 4H- and 6H-Silicon Carbide," *J. Electron. Mater.*, Vol. 27, No. 4, 1998, pp. 370–376.

[7] Senzaki, J., et al., "Electrical Characteristics and Surface Morphology for Arsenic Ion-Implanted 4H-SiC at High Temperature," *Mater. Sci. Forum*, Vol. 338–342, 2000, pp. 865–868.

[8] Jones, K. A., et al., "AlN as an Encapsulate for Annealing SiC," *J. Appl. Phys.*, Vol. 83, No. 12, 1998, pp. 8010–8015.

[9] Saddow, S. E., et al., "High Temperature Electrical Activation in 4H and 6H-SiC in a Silane Ambient to Reduce Step Bunching," *Mater. Sci. Forum,* Vol. 338–342, 2000, pp. 901–904.

[10] Petzold, J., et al., "Polytype Transition Ion-Implanted Silicon Carbide," *Nucl. Instrum. Meth. Phys. Res. B*, Vol. 80/81, 1993, pp. 943–948.

[11] Wesh, W., et al., "Investigation of Radiation Damage in Ion-Implanted and Annealed SiC Layers," *Nucl. Instrum. Meth. Phys. Res. B*, Vol. 106, 1995, pp. 339–345.

[12] Satoh, M., "Annealing of Implanted Layers in (1–100) and (11–20) Oriented SiC," *Mater. Sci. Forum*, Vol. 389–393, 2002, pp. 773–778.

[13] Linnarsson, M. K., et al., "Solubility Limit and Precipitate Formation in Al-Doped 4H-SiC Epitaxial Material," *Appl. Phys. Lett.*, Vol. 79, No. 13, 2001, pp. 2016–2018.

[14] Deák, P., et al., "A Shallow Acceptor Complex in 4H-SiC: AlSiNCAlSi," *Mater. Sci. Forum,* Vol. 433–436, 2003, pp. 523–526.

[15] Kimoto, T., et al., "The Effects of N^+ Dose in Implantation into 6H-SiC Epilayers," *J. Electron. Mater.*, Vol. 24, No. 4, 1995, pp. 235–240.

[16] Österman, J., et al., "Carrier Concentration in Implanted and Epitaxial 4H-SiC by Scanning Spreading Resistance Microscopy," *Mater. Sci. Forum,* Vol. 389–393, 2002, pp. 663–666.

[17] Nipoti, R., A. Carnera, and V. Raineri, "Comparison Between Chemical and Electrical Profiles in Al^+ and N^+ Implanted and Annealed 6H-SiC," *Mater. Sci. Forum,* Vol. 389–393, 2002, pp. 811–814.

[18] Moll, A. J., et al., "The Effect of Coimplantation on the Electrical Activity of Implanted Carbon in GaAs," *J. Appl. Phys.,* Vol. 74, No. 14, 1993, pp. 7118–7123.

[19] Rao, M. V., et al., "Al, Al/C and Al/Si Implantation in 6H-SiC," *J. Electron. Mater.*, Vol. 25, No. 1, 1996, pp.75–80.

[20] Zhao, J. H., et al., "Evaluation of Ohmic Contacts to p-Type 6H-SiC Created by C and Al Coimplantation," *IEEE Electron Device Lett.*, Vol. 18, No. 8, 1997, pp. 375–377.

[21] Tone, K., and J. H. Zhao, "A Comparative Study of C Plus Al Coimplantation and Al Implantation in 4H- and 6H-SiC," *IEEE Trans. on Electron Devices*, Vol. 46, No. 3, 1999, pp. 612–619.

[22] Itoh, H., T. Troffer, and G. Pensl, "Coimplantation Effects on the Electrical Properties of Boron and Aluminum Acceptors in 4H-SiC," *Mater. Sci. Forum,* Vol. 264–268, 1998, pp. 685–688.

[23] Wong-Leung, J., M. S. Janson, and B. G. Svensson "Effect of Crystal Orientation on the Implanted Profile of 60 keV Al into 4H-SiC Crystals," *J. Appl. Phys.*, Vol. 93, No. 11, 2003, pp. 8914–8917.

[24] Morvan, E., et al., "Channeling Implantations of Al^+ into 6H Silicon Carbide," *Appl. Phys. Lett.*, Vol. 74, No. 26, 1999, pp. 3990–3992.

[25] Ohno, T., and K. Amemiya, "Influence of Implantation Temperature and Dose Rate on Secondary Defects Formation in 4H-SiC," *Mater. Sci. Forum,* Vol. 389–393, 2002, pp. 823–826.

[26] Kuznetsov, A. Y., et al., "Dose-Rate Effect in 4H-SiC Implanted with Si^+ Ions," *J. Appl. Phys,* Vol. 94, 2003, pp. 7112–7115.

[27] Linnarson, M. K., A. Hallèn, and B. G. Svensson, "Depth Profiling of Ion- Implanted SiC," *Proceedings of the 12th Intl. Conference on Secondary Ion Mass Spectrometry*, Brussels, Belgium, September 5–11, 1999, pp. 643–646.

[28] Ya Ber, B., et al., "Determination of Nitrogen in Silicon Carbide by Secondary Ion Mass Spectroscopy," *Appl. Surf. Sci.*, Vol. 203–204, 2003, pp. 184–188.

[29] Kudriavtsev, Y., et al., "Quantitative SIMS Analysis of SiC," *Surface Interface Anal.*, Vol. 35, 2003, pp. 491–495.

[30] Nipoti, R., and M. Servidori, "Rutherford Backscattering Studies of Ion-Implanted Semiconductors," in *Semiconductors and Semimetals*, G. Ghibaudo and C. Christophides, (eds.), San Diego, CA: Academic Press, 1997, Vol. 45, pp. 239–260.

[31] Zolnai, Z., et al., "Investigation of Ion Implantation Induced Damage in the Carbon and Silicon Sublattices of 6H-SiC," *Diamonds and Related Materials*, Vol. 11, 2002, pp. 1239–1242.

[32] Nashiyama, I., et al., "Deuteron Channeling for Defect Analysis of Silicon Carbide," *Nucl. Instr. and Meth. in Phys. Res. B,* Vol. 33, 1988, pp. 599–602.

[33] Jiang, W., et al., "Deuterium Channeling Analysis for He^+-Implanted 6H-SiC," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 161–163, 2000, pp. 501–504.

[34] Wang, C. M., et al., "Microstructural Features of Al-Implanted 4H-SiC," *J. Mater. Res.*, Vol. 18, 2003, pp. 772–779.

[35] Zhang, Y., et al., "Effects of Implantation Temperature and Ion Flux on Damage Accumulation in Al-Implanted 4H-SiC," *J. Appl. Phys.*, Vol. 93, No. 4, 2003, pp. 1954–1960.

[36] Nakashima, S., and H. Harima, "Raman Investigation of SiC Polytypes," *Phys. Stat. Sol*, Vol. 162, 1997, pp. 39–64.

[37] Campos, F. J., et al., "Confocal Micro-Raman Scattering and Rutherford Backscattering Characterization of Lattice Damage in Aluminum-Implanted 6H-SiC," *Diamond and Related Materials*, Vol. 9, 1999, pp. 357–360.

[38] Nipoti, R., A. Carnera, and G. Mattei, "Structural, Optical and Chemical Characterization of 300°C, MeV Ion Implanted and 1700°C Annealed 6H-SiC," *Mat. Res. Soc. Symp. Proc.*, Vol. 640, 2001, pp. H5.28.1–H5.28.6.

[39] Uedono, A., et al., "Oxygen-Related Defects in O^+ Implanted 6H-SiC Studied by Monoenergetic Positron Beam," *J. App. Phys.*, Vol. 86, No. 10, 1999, pp. 5392–5398.

[40] Janson, M. S., et al., "Vacancy Type Defects Distribution of ^{11}B-, ^{14}N-, and ^{27}Al-Implanted 4H-SiC Studied by Positron Annihilation Spectroscopy," *Mater. Sci. Forum,* Vol. 433–436, 2003, pp. 641–644.

[41] Fung, S., et al., "Aluminum Implantation Induced Deep Levels in n-Type 6H-SiC," *J. App. Phys.*, Vol. 84, No. 2, 1998, pp. 1152–1154.

[42] Nipoti, R., et al., "A Study of He^+ Ion-Induced Damage in Silicon by Quantitative Analysis of Charge Collection Efficiency Data," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 136–138, 1998, pp. 1340–1344.

[43] Åberg, D., et al., "Nitrogen Deactivation by Implantation-Induced Defects in 4H-SiC Epitaxial Layers," *Appl. Phys. Lett.*, Vol. 78, No. 19, 2001, pp. 2908–2910.

[44] Satoh, M., et al., "Site Identification of 6H-SiC Using RBS-Channeling Technique," *Mater. Sci. Forum,* Vol. 264–268, 1998, pp. 441–444.

[45] Nipoti, R., and A. Carnera, "4H- and 6H-SiC Rutherford Backscattering Channeling Spectrometry: Polytype Finger Printing," *Mater. Sci. Forum,* Vol. 335–356, 2001, pp. 279–282.

[46] Albertazzi, E., and G. Lulli, "Monte Carlo Simulation of Ion Implantation in Cristalline SiC," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 120, 1996, pp. 147–150.

[47] Bianconi, M., et al., "RBS-Channeling Analysis of Virgin 6H-SiC: Experiments and Monte Carlo Simulations," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 136–138, 1998, pp. 1267–1271.

[48] Khánh, N. Q., et al., "He Ion Beam Density Effect on Damage Induced in SiC During Rutherford Backscattering Measurement," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 161–163, 2000, pp. 424–428.

[49] Nipoti, R., et al., "Ion Implantation Induced Swelling in 6H-SiC," *Appl. Phys. Lett.*, Vol. 70, No. 25, 1997, pp. 3425–3427.

[50] Battistig, G., et al., "High-Sensitivity Ion Beam Analytical Method for Studying Ion-Implanted SiC," *Mater. Sci. Forum,* Vol. 433–436, 2003, pp. 625–628.

[51] Weber, W. J., et al., "Damage Evolution and Recovery in 4H and 6H Silicon Carbide Irradiated with Aluminum Ions," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 191, 2002, pp. 514–518.

[52] Nipoti, R., and F. Letertre, " Channeling Stopping Power of MeV He^+ Ions in 4H- and 6H-SiC," *Mat. Res. Soc. Symp. Proc.*, Vol. 742, 2003, pp. 115–119.

[53] Bolse, W., et al., "Ion-Beam-Induced Amorphization of 6H-SiC," *Surf. Coat. Technol*, Vol. 74–75, 1995, pp. 927–931.

[54] Romano, A., et al., "Modeling SiC Swelling Under Irradiation: Influence of Amorphization," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 202, 2003, pp. 100–106.

[55] Zhang, Y., et al., "Damage Evolution and Recovery on Both Si and C Sublattices in Al-Implanted 4H-SiC Studied by Rutherford Backscattering Spectroscopy and Nuclear Reaction Analysis," *J. Appl. Phys.*, Vol. 91, No. 10, 2002, pp. 6388–6395.

[56] Henkel, T., et al., "In-Situ Laser Reflectometry Study of the Amorphization of Silicon Carbide by MeV Ion Implantation," *J. Appl. Phys.,* Vol. 84, No. 6, 1998, pp. 3090–3097.

[57] Weber, W. J., "Models and Mechanisms of Irradiation-Induced Amorphization in Ceramics," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 166–167, 2000, pp. 98–106.

[58] Weber, W. J., et al., "Fundamental Nature of Ion-Solid Interaction in SiC," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 206, 2003, pp. 1–6.

[59] Jiang, W., et al., "Accumulation and Recovery of Disorder on Silicon and Carbon Sublattices in Ion-Irradiated 6H-SiC," *J. Nucl. Mater.*, Vol. 289, 2001, pp. 96–101.

[60] Jiang, W., and W. J. Weber, "Multiaxial Channeling Study of Disorder Accumulation and Recovery in Gold-Irradiated 6H-SiC," *Phys. Rev. B,* Vol. 64, 2001, pp. 125,206–125,216.

[61] Gao, F., W. J. Weber, and R. Devanathan, "Defect Production, Multiple Ion-Solid Interactions and Amorphization in SiC," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 191, 2002, pp. 487–496.

[62] http://www.srim.org/SRIM.

[63] Jiang, W., et al., "Displacement Energy Measurements for Ion-Irradiated 6H-SiC," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 148, 1999, pp. 557–561.

[64] Devanathan, R., W. J. Weber, and F. Gao, "Atomic Scale Simulation of Defect Production in Irradiated 3C-SiC," *J. Appl. Phys.*, Vol. 90, No. 5, 2001, pp. 2303–2309.

[65] Weber, W. J., L. M. Wang, and N. Yu, "The Irradiation-Induced Crystalline-to-Amorphous Phase Transition in α-SiC," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 116, 1996, pp. 322–326.

[66] Bockstedte, M., et al., "The Nature and Diffusion of Intrinsic Point Defects in SiC," *Mat. Sci. Forum*, Vol. 389–393, 2002, pp. 471–476.

[67] Son, N. T., P. E. Hai, and E. Janzén, "Carbon Vacancy-Related Centers in 4H and 6H SiC," *Phys. Rev. B,* Vol. 63, 2001, pp. 201,201–201,204.

[68] Itoh, H., et al., "Electron Spin Resonance Study of Defects in CVD-Grown 3C-SiC Irradiated with 2 MeV Protons," *J. Electron. Mater.*, Vol. 21, 1992, pp. 707–710.

[69] Lulli, L., et al., "Damage Profiles in High-Energy As Implanted Si," *J. Appl. Phys.*, Vol. 88, No. 7, 2000, pp. 3993–3999.

[70] Janson, M. S., et al., "Ion Implantation Range Distribution in Silicon Carbide," *J. Appl. Phys.*, Vol. 93, No. 11, 2003, pp. 8903–8909.

[71] Morvan, E., et al., "Monte Carlo Simulation of Ion Implantation into SiC-6H Single Crystal Including Channeling Effect," *Mat. Sci. Eng.*, Vol. B46, 1997, pp. 218–222.

[72] Lulli, G., et al., "The Monte Carlo Binary Collision Approximation Applied to the Simulation of the Ion Implantation Process in Single-Crystal SiC: High-Dose Effects," *Mater. Sci. Forum,* Vol. 335–356, 2001, pp. 599–602.

[73] Lulli, G., et al., "Binary Collision Approximation Modeling of Ion-Induced Damage Effects in Crystalline 6H-SiC," *Nucl. Instr. and Meth. in Phys. Res. B*, Vol. 148, 1999, pp. 573–577.

[74] Morvan, E., "Damage Reduction in Channeled Ion-Implanted 6H-SiC," *Mater. Sci. Forum*, Vol. 338–342, 2000, pp. 893–896.

[75] Zolnai, Z., et al., "Damage Distributions Induced by Channeling Implantation of Nitrogen into 6H Silicon Carbide," *Mater. Sci. Forum*, Vol. 433–436, 2003, pp. 645–648.

[76] Morvan, E., et al., "Lateral Spread of Implantation Ion Distribution in 6H-SiC: Simulation," *Mater. Sci. Ing.*, Vol. B61–B62, 1999, pp. 373–377.

[77] Inoue, N., et al., "Hot Implantation of N^+ into α-SiC Epilayers," *Inst. Phys. Conf. Ser. No. 142*, 1996, pp. 525–528.

[78] Kawase, D., et al., "Amorphization and Recrystallization of Al-Implanted 6H-SiC," *Inst. Phys. Conf. Ser. No. 142*, 1996, pp. 513–516.

[79] Jones, K. A., et al., "The Properties of Annealed AlN Films Deposited by Pulsed Laser Deposition," *J. Electronic Materials*, Vol. 29, No. 3, 2000, pp. 262–267.

[80] Ruppalt, L. B., et al., "Using a PLD BN/AlN Composite as an Annealing Cap for Ion-Implanted SiC," *Sol. St. Electron.*, Vol. 47, 2003, pp. 253–257.

[81] Dutto, C., et al., " Long Pulse Duration Excimer Laser Annealing of Al^+ Ion-Implanted 4H-SiC for pn Junction," *Appl. Surf. Sci.,* Vol. 208–209, 2003, pp. 292–297.

[82] Capano, M. A., et al, "Surface Roughening in Ion-Implanted 4H-Silicon Carbide," *J. Electronic Materials*, Vol. 28, No 3, 1999, pp. 214–218.

[83] Pankin, D., et al., "High Concentration Doping of 6H-SiC by Ion-Implantation: Flash Versus Furnace Annealing," *Mat. Sci. Forum,* Vol. 338–342, 2000, pp. 877–880.

[84] Sakin, I., et al., "On the Development of 6H-SiC LDMOS Transistors Using Silane Ambient Implant Anneal," *Solid State Electronics*, Vol. 45, 2001, pp. 1653–1657.

[85] Kumar, V., "Implant Annealing of SiC in a Silane Ambient," Master's Thesis, Mississippi State University, Starkville, MS, May 2001.

[86] Saddow, S. E., et al., "Effects of Substrate Surface Preparation on Chemical Vapor Deposition Growth of 4H-SiC Epitaxial Layers," *J. of Electronic Materials*, Vol. 30, No. 3, 2001, pp. 228–234.

[87] Saddow, S. E., et al., "High Temperature Implant Activation in 4H and 6H-SiC in a Silane Ambient to Reduce Step Bunching,"*Mat. Sci. Forum,* Vol. 338–342, 2000, pp. 901–904.

[88] Troffer, T., et al., "Doping of SiC by Implantation of Boron and Aluminum," *Phys. Stat. Sol.(a)*, Vol. 162, 1997, pp. 277–298.

[89] Seshadri, S., G. W. Eldridge, and A. K. Agarwal, "Comparison of the Annealing Behavior of High-Dose Nitrogen-, Aluminum-, and Boron-Implanted 4H-SiC," *Appl. Phys. Lett.*, Vol. 72, No. 16, 1998, pp. 2026–2028.

[90] Janson, M. S., et al., "Transient Enhanced Diffusion of Implanted Boron in 4H-Silicon Carbide," *Appl. Phys. Lett.*, Vol. 76, No. 11, 2000, pp. 1434–1436.

[91] Phelps, G.J., et al., "Enhanced Dopant Diffusion Effects in 4H Silicon Carbide," *Mater. Sci. Forum,* Vol. 389–393, 2002, pp. 855–858.

[92] Kimoto, T., N. Inoue, and H. Matsunami, "Nitrogen Ion Implantation into α-SiC Epitaxial Layers," *Phys. Stat. Sol.(a)*, Vol. 162, 1997, pp. 263–276.

[93] Rao, M. V., et al., "Phosphorous and Boron Implantation in 6H-SiC," *J. Appl. Phys.*, Vol. 81, No. 10, 1997, pp. 6635–6641.

[94] Schmid, F., et al., "Electrical Activation of Implanted Phosphorous Ions in (0001)/(11–20)-Oriented 4H-SiC," *Mater. Sci. Forum,* Vol. 389–393, 2002, pp. 787–790.

[95] Mokhov, E. N., E. E. Goncharov, and G. G. Ryabova, "Diffusion of Boron in p-Type Silicon Carbide," *Sov. Phys. Semicond.*, Vol. 18, 1984, pp. 27–29.

[96] Mokhov, E. N., E. E. Goncharov, and G. G. Ryabova, "Constant-Concentration Diffusion of Boron in Silicon Carbide," *Sov. Phys. Solid State*, Vol. 30, 1988, pp. 140–141.

[97] Vodakov, Y. A., E. N. Mokhov, and V. G. Oding, "Interstitial Diffusion of B and Be in SiC," *Inorg. Mater.*, Vol. 19, 1984, pp. 979–981.

[98] Jain, S. C., et al., "Transient Enhanced Diffusion of Boron in Si," *J. Appl. Phys.*, Vol. 91, No. 11, 2002, pp. 8919–8941.

[99] Laube, M., and G. Pensl, "Transient-Enhanced Diffusion of Boron in SiC," *Mater. Sci. Forum,* Vol. 338–342, 2000, pp. 941–944.

[100] Laube, M., G. Pensl, and H. Itoh, "Suppressed Diffusion of Boron in 4H-SiC," *Appl. Phys. Lett.,* Vol. 74, No. 16, 1999, pp. 2292–2294.

[101] Itoh, H., et al., "Photoluminescence of Radiation-Induced Defects in 3C-SiC Epitaxialy Grown on SiC," *J. Appl. Phys.*, Vol. 77, No. 2, 1995, pp. 837–842.

[102] Bracht, H., et al., "Modeling of Boron Diffusion in Silicon Carbide," *Mater. Sci. Forum*, Vol. 353–356, 2001, pp. 327–330.

[103] Heera, V., and W. Skorupa, "Ion Implantation and Annealing Effects in Silicon Carbide," *Mat. Res. Soc. Symp. Proc.*, Vol. 438, 1997, pp. 241–252.

[104] Kawasuso, A., et al., "Vacancies in He-Implanted 4H- and 6H-SiC Epilayers Studied by Positron Annihilation," *Physica B*, Vol. 308–310, 2001, pp. 660–663.

[105] Ohno, T., and N. Kobayashi, "Structure and Distribution of Secondary Defects in High-Energy Ion-Implanted 4H-SiC," *J. Appl. Phys.*, Vol. 89, No. 2, 2001, pp. 933–941.

[106] Persson, P. O. Å., et al., "On the Nature of Implantation-Induced Dislocation Loops in 4H-Silicon Carbide," *J. Appl. Phys.*, Vol. 92, No. 5, 2002, pp. 2501–2505.

[107] Persson, P. O. Å., et al., "Dislocation Loop Evolution in Ion-Implanted 4H-SiC," *J. Appl. Phys.*, Vol. 93, No. 11, 2003, pp. 9395–9397.

[108] Vodakhov, Y. A., et al., "Doping Peculiarities of SiC Epitaxial Layers Grown by Sublimation Sandwich-Method," *Springer Proc. Phys.*, Vol. 56, 1992, pp. 329–334.

[109] Schultz, D., et al., "Study of Nitrogen Incorporation in 6H-SiC Single Crystals Grown by PVT," *Mater. Sci. Forum*, Vol. 338–342, 2000, pp. 87–90.

[110] Laube, M., et al., "Electrical Activation of High Concentrations of N^+ and P^+ Ions Implanted into 4H-SiC," *J. Appl. Phys.*, Vol. 92, No. 1, 2002, pp. 549–554.

[111] Saks, N. S., et al., "Low-Dose Nitrogen Implants in 6H Silicon Carbide," *Appl. Phys. Lett.*, Vol. 76, 2000, pp. 1896–1898.

[112] Saks, N. S., S. H. Ryu, and S. V. Suvorov, "Low-Dose n-Type Nitrogen Implants in 4H-SiC," *Appl. Phys. Lett.*, Vol. 81, 2002, pp. 4958–4960.

[113] Negoro, Y., et al., "Remarkable Lattice Recovery and Low Sheet Resistance of Phosphorus-Implanted 4H-SiC (11–20)," *Appl. Phys. Lett.*, Vol. 80, No. 2, 2001, pp. 240–242.

[114] Schmidt, F., et al., "Electrical Activation of Implanted Phosphorus Ions in [0001]- and [11–20]-Oriented 4H-SiC," *J. Appl. Phys.*, Vol. 91, No. 11, 2002, pp. 9182–9186.

[115] Greulich-Weber, S., et al., "On the Microscopic Structures of Shallow Donors in 6H-SiC: Studies with EPR and ENDOR," *Solid State Commun.*, Vol. 93, No. 5, 1995, pp. 393–397.

[116] Gardner, J. A., et al., "Material and n-p Junction Properties of N-, P-, and N/P-Implanted SiC," *J. Appl. Phys.*, Vol. 83, No. 10, 1998, pp. 5118–5124.

[117] Pensl, G., and W. J. Choyke, "Electrical and Optical Properties of SiC," *Physica B*, Vol. 185, 1993, pp. 264–283.

[118] Bluet, J. M., et al., "Activation of Aluminum Implanted at High Doses in 4H-SiC," *J. Appl. Phys.*, Vol. 88, No. 4, 2000, pp.1971–1977.

[119] Heera, V., D. Panknin, and W. Skorupa, "p-Type Doping of SiC by High- Dose Al Implantation-Problems and Progress," *Appl. Surf. Sci.*, Vol. 184, 2001, pp. 307–316.

[120] Schöner, A., et al., "High Energy Implantation of Boron in 4H-SiC," *Mat. Res. Symp. Proc.*, Vol. 512, 1998, pp. 469–474.

[121] Giannazzo, F., et al., "Carrier Concentration Profiles in 6H-SiC by Scanning Capacitance Microscopy," *Mater. Sci. Semicond. Processing*, Vol. 4, No. 1–3, 2001, pp. 195–199.

[122] Österman, J., A. Hallén, and S. Anand, "Carrier Profiling of Al-Doped 4H-SiC by Scanning Spreading Resistance Microscopy," *Appl. Phys. Lett.*, Vol. 81, No. 16, 2002, pp. 3004–3006.

[123] Suda, J., et al., "Scanning Capacitance and Spreading Resistance Microscopy of SiC Multiple pn-Junction Structure," *Jpn. J. Appl. Phys.*, Vol. 41, No. 1A/B, 2002, pp. L40–L42.

[124] Kalinina, E., et al., "High-Dose Al-Implanted 4H-SiC p^+-n-n^+ Junctions," *Appl. Phys. Lett.*, Vol. 77, No. 19, 2000, pp. 3051–3053.

CHAPTER 5

Power SiC MOSFETS

I. Sankin and J. B. Casady

5.1 Introduction

An increasing demand for high-voltage, high-power electronic devices and the fact that traditional silicon technology has come close to its theoretical limits in high-power applications gave birth to a new era of power electronics—an era of wide bandgap semiconductors. Initial poor quality and extremely high cost of new materials made the transition between silicon and wider bandgap semiconductors like SiC and GaN very gradual; however, we are now witnessing dramatic improvements in these areas. The most significant success has been made in the field of SiC power rectifiers. Multikilovolt 4H-SiC PiN and merged pin Schottky (MPS) diodes able to conduct hundreds of amperes of forward current were reported, and 1,200-V, 6-A Schottky diodes were introduced commercially in 2003. A dramatic improvement was also made in the field of high-power SiC switching devices. In the mid-1990s, SiC MOS transistors were projected to replace their silicon analogues in high-voltage applications. Even the recently introduced CoolMOS transistor [1], which was expected to breathe new life into power silicon MOS technology, is unable to exceed the theoretical potential of SiC devices in this field. In this chapter, we will provide a short historic review of SiC power MOSFET development, which will help the reader estimate the speed of SiC MOS developments, and evaluate future trends in this area.

As with Si power MOSFET development, researchers quickly realized that success would not be rapid, but would take focused, carefully planned efforts to optimize the inversion channel mobility, device structure, and reliability. Simply copying design and process approaches from silicon technology would not lead to desired results. First of all, many of the technological processes from the silicon industry are not applicable to SiC because of different material properties. Secondly, and also most important, the poor interface quality between the gate oxide and SiC bulk material suppresses channel mobility to values at least an order of magnitude lower than bulk mobility. These difficulties required new design solutions to minimize the channel resistance without compromising the other components of the device on-resistance. The right choice of material polytype, crystal orientation, gate dielectric, and method of gate formation dramatically improves the device performance. In this chapter, we will discuss different design and technological approaches directed to overcome challenges in achieving the perfect device.

5.2 SiC UMOSFET

The classical U-groove n-channel power MOSFET transistor (UMOSFET) in SiC is a vertical device, which comprises epitaxially grown thick n- drift region and p-type base region. N+ source and p+ body contact regions can be either epitaxially grown or implanted. Dry plasma etch is used to form a trench, and a thin dielectric layer is then thermally grown or deposited followed by metal or polysilicon gate deposition to define a vertical MOS channel. A simplified cross section of n-channel UMOSFET is shown in Figure 5.1.

Potentially, 4H-SiC UMOS transistor structure offers several advantages over other design solutions as follows:

- Vertical configuration,[1] where the absence of JFET region allows for taking maximum advantage from excellent blocking/conductive properties of the SiC drift layer [4];
- Relatively simple structure that can be made using self-aligned fabrication process resulting in a significant increase of channel packing density;
- The doping profiles in the entire device structure can be realized by epitaxial growth.

However, after the first years of great expectations supported by early impressive results reported by Palmour et al. in 1994 [5], it became clear that initial predictions of a revolutionary improvement in power switching by employing vertical SiC MOSFETs are difficult to accomplish due to multiple reasons. In particular, a critical analysis of performance advantages and limitations of 4H-SiC power UMOSFET structure has been made by Agarwal et al. in 1996 [6]. The main issues raised in this work were:

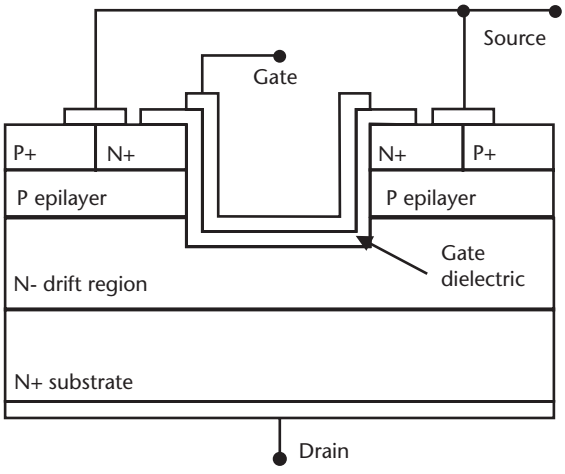


Figure 5.1 Schematic cross section of a classical UMOSFET.

1. Vertical power devices in SiC usually are made on 4H polytype. 4H-SiC exhibits excellent electron mobility along the *c*-axis, which is almost an order of magnitude higher in this direction than that of 6H-SiC [2, 3].

- On-state insulator reliability due to much smaller conduction band offset of SiC to SiO_2 compared with that of silicon [6–8];
- High electric field in the gate insulator under off-condition due to electric field enhancement at the sharp corner of the U-trenches;
- Low inversion channel mobility on a vertical sidewall due to high interface state density at the p-SiC/SiO_2 interface and high fixed charge density in the insulator.

To analyze the issues addressed, let us first consider the relation between blocking capability and specific on-state resistance of the drift region of a vertical SiC MOSFET. For the devices with high blocking requirements, the resistance of the voltage blocking layer, or drift region, becomes one of the dominant components of the total specific on-state resistance. This means that at a fixed forward voltage drop, conduction current density strongly depends on the specific resistance of the drift region R_{dr}, which is defined by its thickness T, and doping profile $N(x)$:

$$R_{dr} = \frac{1}{q}\int_0^T \frac{dx}{\mu(N(x))N(x)} \tag{5.1}$$

where μ is the electron mobility and q is the electronic charge. Assuming a uniform epi doping concentration $N(x) = N$, the previous expression can be simplified as follows:

$$R_{dr}(T,N) = \frac{T}{q\mu N} \tag{5.2}$$

Assuming also that the entire reverse voltage drop occurs over the drift region, the blocking voltage of the device V_b can be expressed in terms of the maximum 1-D electric field under the junction E_b, as well as the doping N and thickness T of the drift region:

$$V_b = E_b T = \frac{qT^2 N}{2\varepsilon_0 \varepsilon_r} = g(T,N) \tag{5.3}$$

where ε_0 and ε_r are the dielectric permittivity of vacuum (8.854×10^{-14} F/cm) and the relative dielectric constant of semiconductor (9.8 for 4H-SiC), respectively. To minimize the specific resistance of the drift layer subject to the constraint $g(T, N)$, one can use the method of Lagrange multipliers:

$$\begin{aligned} &\frac{\partial}{\partial T}\left(R_{dr}(T,N) - \lambda g(T,N)\right) = 0 \\ &\frac{\partial}{\partial N}\left(R_{dr}(T,N) - \lambda g(T,N)\right) = 0 \\ &g(T,N) = V_b \end{aligned} \tag{5.4}$$

The number λ in (5.4) is called the Lagrange multiplier. Solving this equation system with respect to T, N, and λ results in the optimal epi parameters for the drift region:

$$T_{opt}(V_b, E_b) = \frac{3}{2}\frac{V_b}{E_b}$$
$$N_{opt}(V_b, E_b) = \frac{4}{9}\frac{\varepsilon_0 \varepsilon_r}{q}\frac{E_b^2}{V_b} \tag{5.5}$$

Consequently, the optimal epi parameters result in the minimal resistance value:

$$R_{drMIN}(V_b, E_b) = \frac{27}{8}\frac{V_b^2}{\varepsilon_0 \varepsilon_r \mu E_b^3} \tag{5.6}$$

The low-field electron mobility μ in (5.6) for 4H-SiC in the *c*-axis direction can be expressed using Caughey-Thomas mobility formula with fitted parameters [9]:

$$\mu = \frac{1141\left(\frac{T}{300}\right)^{-2.15}}{1+\left(\frac{N}{1.94e17}\right)^{0.61}} \tag{5.7}$$

As can be seen from (5.6), the minimum on-state resistance is reversely proportional to the third power of the maximum one-dimensional electric field in SiC. On the other hand, when returning to UMOSFET structure, Gauss' law ($\nabla \cdot \varepsilon\varepsilon_0 \vec{E} = 0$) requires the product of the relative dielectric constant and the normal field of two materials to be constant at their interface. This implies that the normal field in the gate oxide would be 2.5 times higher[2] than that in the underlying SiC layer. Since the operating electric field in thermally grown SiO_2 is limited to 2 MV/cm [6], the maximum field in the underlying SiC layer must be less then 0.8 MV/cm, which is only 20% of its critical value. Plugging this ratio into (5.6) reveals that this limitation results in the resistance of the drift region of 4H-SiC UMOSFET with SiO_2, since the gate dielectric is *64 times higher* than its theoretical minimum! As shown in Figure 5.2, this issue dramatically suppresses the inherent advantages of SiC UMOS transistors over their silicon counterparts.

An obvious way to resolve the problem is to find an alternative gate dielectric, which satisfies the relation[3]

$$\varepsilon_{0,oxide}\varepsilon_{op,oxide} \geq \varepsilon_{0,SiC} \cong 30\ \text{MV/cm}$$

The discussion of potential benefits and drawbacks of using high-k dielectrics as a gate oxide for power SiC UMOS transistors has been made in several publications [8, 10, 11]. A comparative analysis of different insulating materials suitable as gate

2. Dielectric constants for 4H-SiC and SiO_2 are equal to 10 and 3.9, respectively (see Table 5.1).
3. It should be noted that the original concept of UMOS (or VMOS) transistor came from Si, where the relationship $\varepsilon_{SiO_2} E_{opSiO_2} > \varepsilon_{Si} E_{opSi}$ is held perfectly.

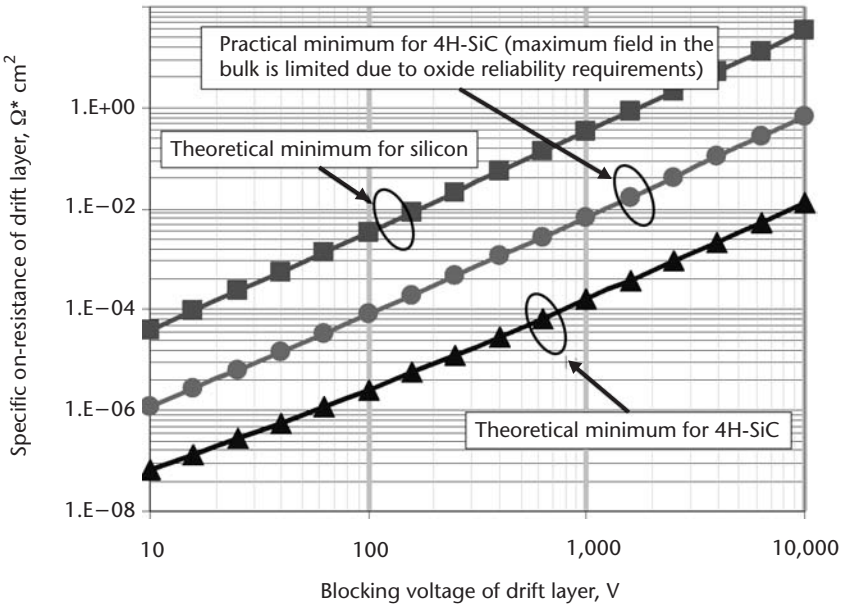


Figure 5.2 Comparison of the practical minimum for a specific drift region on-resistance of 4H-SiC UMOSFET with thermal SiO_2 gate dielectric to the theoretical values calculated for 4H-SiC and Si as a function of blocking voltage. Caughey-Thomas mobility parameters for Si used in this calculation are taken from [12].

dielectric in SiC MOSFETs was done in 1998 by Lipkin and Palmour [11]. In recent years, several emerging high-k dielectrics have attracted enormous attention as potential candidates for gate insulator in the next generation of Si CMOS logic (e.g., [13]). Table 5.1 collects the experimental and theoretical data for several dielectric materials with high dielectric constant, including one of the most promising, HfO_2. For hafnium dioxide (HfO_2), the product of the relative dielectric constant and the operating field is several times higher than that of SiC (Table 5.1), which potentially makes it an ideal gate dielectric in power SiC UMOSFETs. Unfortunately, so far very few attempts of using high-k dielectric materials as gate dielectric of SiC MOSFETs have been published (e.g., [11, 14, 15]).

Another issue related to the design of power SiC UMOS transistors is the junction discontinuity at the sharp corners of the gate trenches. This results in noticeable increase of the maximum electric field in SiC bulk compared with its one-dimensional value. To satisfy oxide reliability requirements, lower doped and thick drift region is required, which results in even more significant increase in the device on-resistance. The deeper the trench is recessed into the n-drift region, the higher the field enhancement at the trench corner. Again, use of high-k gate dielectric can allow for the reduction of the electric field at the corner by minimizing the recess without losing gate control. In addition, using special plasma etch recipe can result in rounded corners of the U-groove reducing in such a way this field enhancement factor.

Two-dimensional numerical simulations of a 1.2-kV 4H-SiC UMOSFET with a 600-Å layer of HfO_2 as gate dielectric confirmed the benefits of using high-k gate dielectric in SiC UMOS transistors. Figure 5.3 shows electric field distribution in

Table 5.1 Experimental and Theoretical Data on High-k Material: Possible Candidates for a Power SiC UMOSFET Gate Dielectric

Material	*Dielectric Constant*	*Critical Field (MV/cm)*	*Operating Field (MV/cm)*	*$\varepsilon_0 E_{op}$ (MV/cm)*	*Conduction Band Offset to Si (eV)**
SiC	10	3	3	30	
SiO_2	3.9	11	2	7.8	3.5
Si_3N_4	7.5	11	2	15	2.4
ONO	6	11	~2	~12	
AlN	8.4	10-12	~3	~30	
BST ($Ba_{1-x}Sr_xTiO_3$)	75–250	2	~0.1	~7.5–25	< 0.1
TiO_2	30–40	6	~0.2	~6–8	
Ta_2O_5	25	10	~0.3	~7.5	0.3
HfO_2	20–40	~5	~2.6	~52–104	1.5

*Calculated conduction band offsets of high-k oxides to Si reported by Robertson [16].
Source: [11].

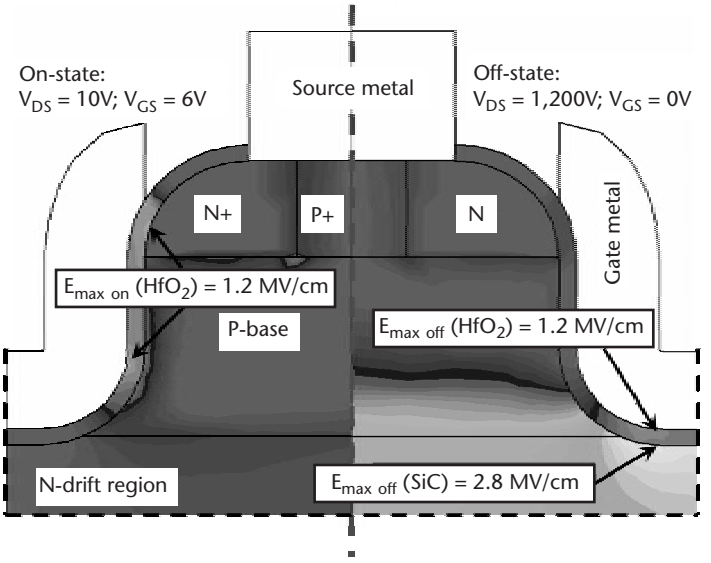


Figure 5.3 Silvaco Atlas simulation of electric field distribution at the trench of 1.2-kV 4H-SiC UMOSFET using HfO_2 (k=25) as a gate dielectric.

close vicinity to the U-groove in both on-state (left side) and off-state (right side) conditions. As expected, the electric field in the HfO_2 gate does not exceed its safe operational value even when the electric field in the underlying 4H-SiC drift region reaches 2.8 MV/cm. Electric field analysis in the simulated structure also proves that electric field enhancement can be eliminated by using a gate trench with rounded corners. Reducing the electric field in the dielectric to its safe value, while at the same time fully employing superior blocking capability of 4H-SiC, allows for the achievement of drift region resistance close to its theoretical minimum value.

So far there has been no published data on inversion channel mobility in metal-HfO_2-SiC structures. However, even assuming extremely poor channel mobility of 0.1 $cm^2/(V \cdot s)$, HfO_2-SiC UMOSFET can offer total specific on-resistance equal to

that of traditional SiO_2-SiC UMOSFET with 200 times higher channel mobility already for 1,700-V blocking voltage (Figure 5.4). When assuming channel mobility of HfO_2-SiC UMISFET being equal to 1 $cm^2/(Vs)$, use of this device becomes beneficial starting from blocking voltages of 400V. Employing HfO_2 in 1,200-V devices with such channel mobility would result in six times smaller specific on-resistance compared with a classical SiO_2-SiC UMOSFET with an inversion channel mobility of 20 $cm^2/(V \cdot s)$.

To protect the transistor from premature gate oxide breakdown, it is highly desirable to have a thick dielectric layer at the bottom of the trench to reduce electric field in oxide. On the other hand, the thickness of the oxide on the sidewalls of the trenches has to be small enough to achieve reasonable threshold voltage. In the case of using thermally grown silicon dioxide as a gate dielectric, however, the situation is rather the opposite. Since the oxidation rate on sidewalls of the trench is almost five times higher than that on the Si-face on the bottom (Figure 5.5), sufficient oxide breakdown strength can be achieved only in expense of threshold voltage, which may reach extremely high values. Figure 5.5 illustrates oxide thickness nonuniformity on the sidewall and Si-face trench bottom of a 4H-SiC, n-type trench transistor structure after steam oxidation at 1,100°C for 45 minutes. To overcome this anisotropic oxidation problem, a thin polysilicon layer can be first deposited and then converted into silicon dioxide, resulting in uniformly thin gate dielectric across the trench [17, 18]. Another way to resolve this problem might be a high-k gate dielectric deposited using spin-on technique. This approach can be highly beneficial, because in this case the corners will be filled with dielectric, providing extra protection in the regions of the highest electric field.

A serious potential problem related to the use of high-k gate dielectrics in SiC power MOSFETs can be encountered due to the much smaller (sometimes-negative) conduction band offsets between SiC and high-k metal oxides compared with silicon dioxide (see Table 5.1). Time-dependent dielectric breakdown (TDDB) and hot

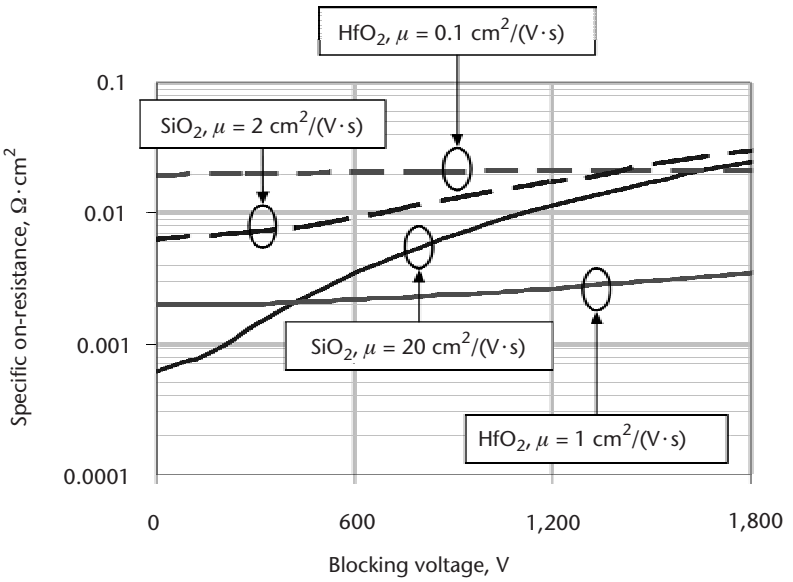


Figure 5.4 Comparison of $R_{ON\text{-}SP}$ of a classical structure 4H-SiC UMOSFET with different gate dielectrics and channel mobilities.

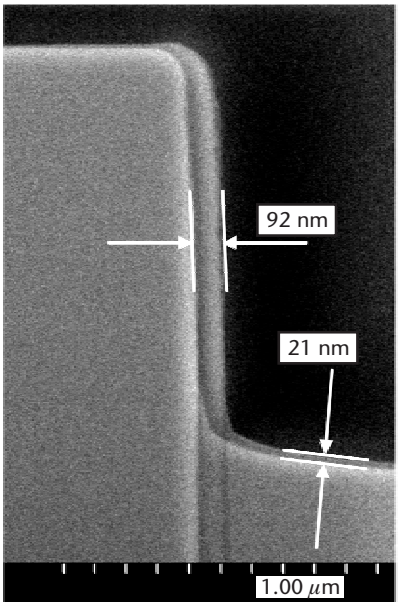


Figure 5.5 In 4H-SiC, an oxidation rate on sidewalls of the trench is almost five times higher than that on the Si-face on the bottom.

carrier injection are expected to be serious reliability issues, especially if high-temperature operation is considered [7].

One of the most important issues preventing commercialization of power SiC MOSFETs so far is MOS channel resistance that results from the extremely low inversion channel mobility in 4H-SiC [19]. This problem may become especially significant in the case of 4H-SiC UMOSFETs, where the oxide-semiconductor interface is severely damaged by plasma etch when the trenches are formed. In general, there are two major approaches to minimize the channel component of on-resistance:

- Improve channel mobility;
- Increase channel packing density.

Increasing channel packing density can be achieved either by use of high-precision lithography or/and by implementing self-aligned fabrication process. Due to today's low production volume of power SiC switches, use of expensive photolithographic equipment may not be economically feasible. On the other hand, unlike double-diffused MOSFET (DMOS) configuration, SiC UMOS transistor structure is ideally suitable for self-aligned fabrication processes that can be adopted from the silicon industry. For example, scaling down a pitch width from today's 15 μm [20] to 1 μm is very realistic. Such increase in the channel packing density would be equivalent to a 15-fold increase in inversion channel mobility, which may not be feasible in the near future. Another benefit that can be realized from downscaling the pitch width is the reduction of the electric field in the gate oxide. It has been shown [21] that by closely spacing the UMOS trenches, the electric field enhancement at the trench corners can be partially eliminated, which allows the use of thinner and

heavier doped drift region. So the increase in the packing density is a powerful tool to reduce the overall resistance of the UMOS structure.

Of course, numerous methods have been employed to increase inversion channel mobility. Significant improvement of channel mobility in lateral 4H-SiC MOSFETs up to 99 $cm^2/(V \cdot s)$ by introducing a normally depleted thin n-type accumulation layer under the gate oxide (buried channel) has been reported by Ogino et al. [22]. In this work, authors used a single energy nitrogen implantation with a dose of 8×10^{12} cm^{-2} that resulted in noncompensated narrow nitrogen profile underneath the gate dielectric. Because of the negligibly low diffusion coefficients in SiC, defining the doping profile in this material can be done by either ion implantation or epitaxial growth. In the case of 4H-SiC UMOSFET, introducing a buried channel on vertical sidewalls of the trenches can be done by angled implantation [23]. To remove the undesirable n-type material from the trench bottoms, this implantation must be followed by short reactive ion etch (RIE) or inductively coupled plasma (ICP) etch. Formation of an n-type accumulation channel by epitaxial regrowth on the side walls of the UMOS trench was reported for the first time in 1997 by Hara [24]. The devices reported in [24] exhibited a blocking voltage of 450V and a specific resistance of 10.9 $m\Omega\text{-}cm^2$, resulting in the figure of merit V_{B2}/R_{ON} of 18.6 MW/cm^2, the highest value reported at that time for SiC MOSFETs.

An efficient approach to protect trench oxide from high electric stress is to introduce a p-n junction at the bottom of the trench by p-type implantation. To screen the electric field effectively, this implanted region must be grounded. This method, however, creates an additional issue by introducing a JFET region and the corresponding component of the total specific on-resistance. To reduce the resistance of this JFET region and facilitate lateral current spreading into the drift region, a thin n-type epilayer can be grown below the p-base. The doping of this current spreading epilayer can be as much as two orders of magnitude higher than that of the n-drift region. A 3-kV 4H-SiC accumulation mode UMOSFET, which utilized all these betterments, has been reported by Li et al. in 2002 [25]. One of the potential benefits of SiC UMOSFET previously discussed is a simple, low-cost and easy-to-manufacture device structure. However, as shown in Figure 5.6, the improvements made in [25] significantly complicate the design and consequently raise the fabrication cost compared with the original UMOSFET concept.

5.3 SiC DIMOSFET

> While the V-groove devices which appeared in the late seventies looked set to find an important place in the market, particularly in the area of high frequency power conversion, the overall dominance of the power bipolar transistor did not seem seriously threatened. However, when the more easily manufacturable vertical DMOS devices appeared in volume in 1978, the scene was set for a revolution. [26]

As previously discussed, silicon dioxide appeared to be a nonideal gate dielectric to be used with silicon carbide in UMOS configuration. Different design solutions used to protect SiO_2 gate dielectric from a high electric field in SiC UMOSFETs resulted in dramatically complicated transistor structure. Because of the problems with SiC UMOSFET, the classical vertical double-diffused MOSFET (VDMOS)

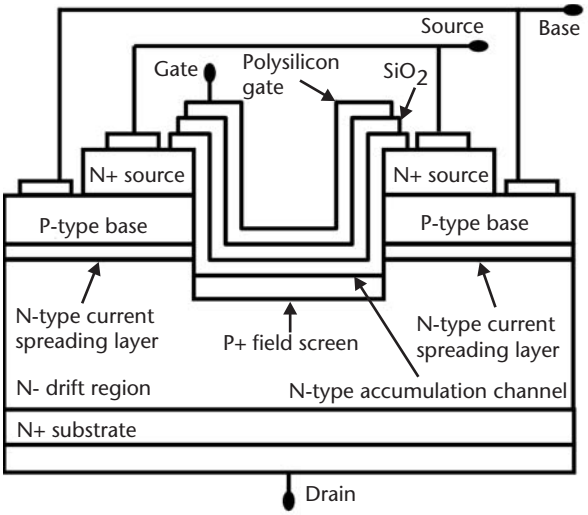


Figure 5.6 Schematic cross-section of an improved high-voltage 4H-SiC accumulation mode UMOSFET. (*From:* [25]. © 1998 IEEE. Reprinted with permission.)

structure first proposed in the 1970s once again attracted researchers' attention. A schematic cross section of a classical Si VDMOS is shown in Figure 5.7. Comprehensive study of this device is given in work [26].

Due to the extremely low diffusion coefficients in SiC, doping profiles in SiC DMOS transistors must be defined by successive implantation of aluminum (boron) for the base region and nitrogen (phosphorus) for the source. This resulted in a new name for a SiC DMOS transistor: double-implanted MOSFET (DIMOSFET).

As shown in Figure 5.8, a typical structure of vertical SiC DIMOSFET comprises both a horizontal inversion channel under the gate oxide (MOS region) and a vertical channel confined between two p-well implanted regions (JFET region). Because of its dual-channel structure, vertical SiC DIMOSFET offers high blocking

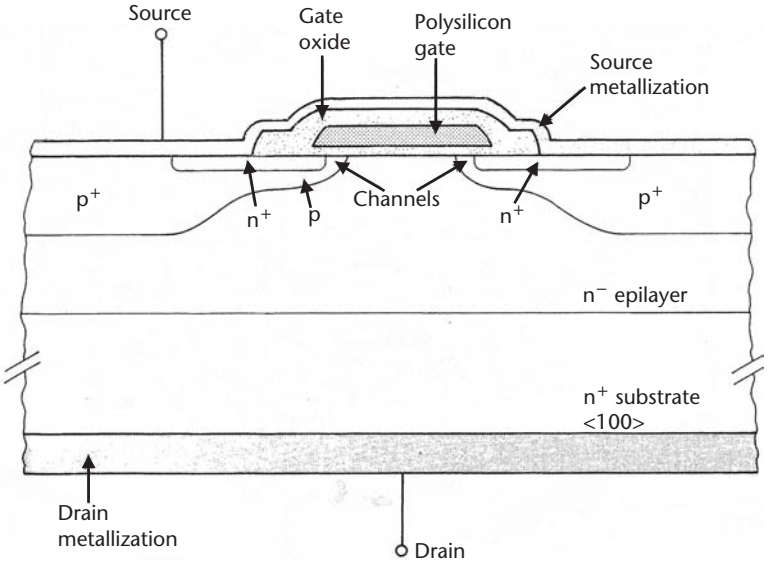


Figure 5.7 Schematic illustration of classical VDMOS transistor. (*After:* [26].)

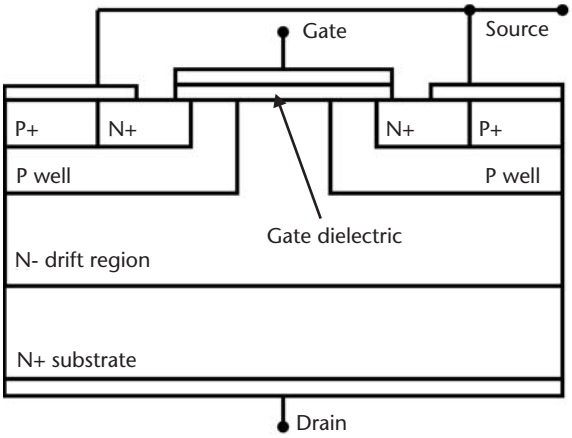


Figure 5.8 Schematic cross section of SiC vertical DIMOSFET.

capabilities along with low on-state voltage drop. In contrast to the SiC UMOSFETs, where the gate oxide is the weakest part of the device because of its location in the region of the highest electric field, DIMOS structure provides excellent protection of gate oxide from electric breakdown by screening it with p-n junctions. Partial sacrifice of on-state conductance by introducing the JFET region can be justified in the case of SiC MOSFETs, where channel resistance is still the dominant part of the total device resistance due to very low inversion channel mobility. Moreover, higher electric field is permitted in the drift region of SiC DIMOSFET, and this allows for a significant reduction of drift resistance compared with UMOS drift region (5.6). Another benefit of using DMOS configuration is that MOS channels can be made on a planar silicon-face surface, where SiC/SiO_2 interface quality is found to be optimal as opposed to the vertical trench surfaces in the UMOS [27].

The first planar double-implanted MOSFETs in 6H-SiC have been reported in 1997 [28]. These devices demonstrated specific on-resistance of 66 $m\Omega cm^2$ and blocking voltages up to 760V, which is nearly three times higher than previously reported operating voltages for SiC MOSFETs. 4H-SiC DiMOSFETs with a specific on-resistance of 55 $m\Omega cm^2$ at the gate bias of 25V capable of blocking 1,950V has been reported in [29]. Nitric oxide postoxidation anneal used in this work resulted in relatively high channel mobility of 14 $cm^2/(V \cdot s)$. Further improvement of the channel mobility to 22 $cm^2/(V \cdot s)$ and reduction of pitch size down from 25 μm to 16 μm, resulting in the channel packing density of 1,250 cm/cm^2 allowed to reduce specific on-resistance down to 42 $m\Omega cm^2$, while maintaining very high blocking capability [30]. The set of I-V curves measured on 10-A 4H-SiC DiMOSFET with a blocking voltage around 2.4 kV reported in this work is shown in Figure 5.9.

Significant improvement in the inversion channel mobility reported in [30] became possible due to a dramatic reduction in the interface state density by postoxidation annealing standard thermal oxides in an NO atmosphere. An extensive experimental and theoretical study exists showing that NO postoxidation anneal improves the $4H\text{-}SiC/SiO_2$ interface quality and inversion channel mobility (e.g., [31–33]). It has also been shown for NO-annealed oxides that the electron injection barrier height increases to values close to the theoretical value at RT that will

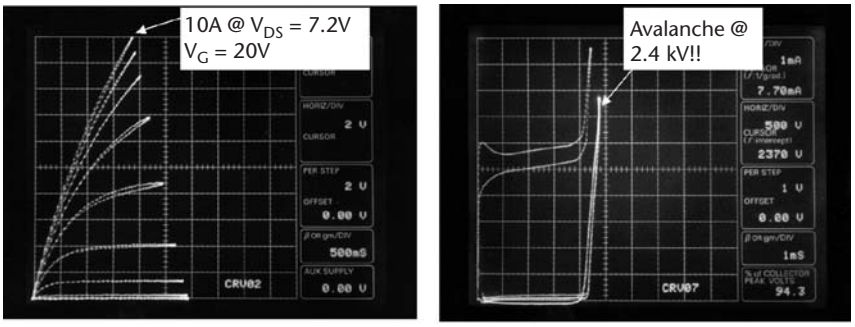


Figure 5.9 I-V characteristics of the 2.4-kV, 10-A 4H-SiC DMOSFET (*From:* [30]. © 2002 IEEE. Reprinted with permission.)

provide improved long-term stability of 4H–SiC power MOSFETs with nitrided gate oxides [34].

As discussed earlier in Section 5.2, introducing thin n-type buried layers under the gate oxide is expected to improve channel mobility. The accumulation mode DMOS structure, referred to as ACCUFET, has been patented by Baliga in 1996 [35]. Experimental results on this structure implemented in 6H-SiC have been published in work [36]. Similar devices implemented in 4H-SiC and referred to as Accu-DMOSFET have been reported later by Singh et al. [37].

A schematic cross section of ACCUFET is shown in Figure 5.10. This device offers a significant improvement over the conventional DMOS structure under both on- and off-state conditions. On one hand, it can withstand higher blocking voltage because the gate oxide is located farther away from the region of the highest electric field, compared with traditional DMOSFET; on the other hand, the accumulation channel is expected to show much higher effective electron mobility than inversion channels, which is very important in the case of 4H-SiC. Depending on the thickness of n-type channel and spacing between buried p^+ regions, this structure can exhibit either normally-off or normally-on behavior. The major drawback of the proposed

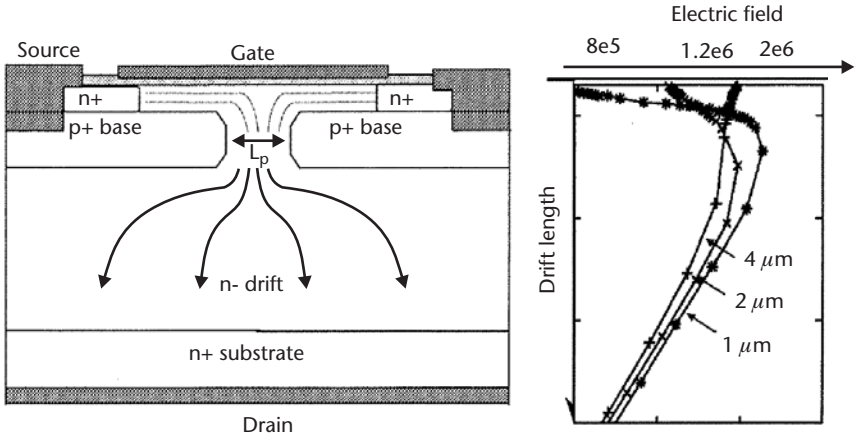


Figure 5.10 Basic structure of the ACCUFET and the reverse bias simulations showing electric field at the SiO2/SiC interface. The reverse bias simulations were for three p+ base region spacings of 1, 2, and 4 μm. (Courtesy of R. Singh of CREE Inc.)

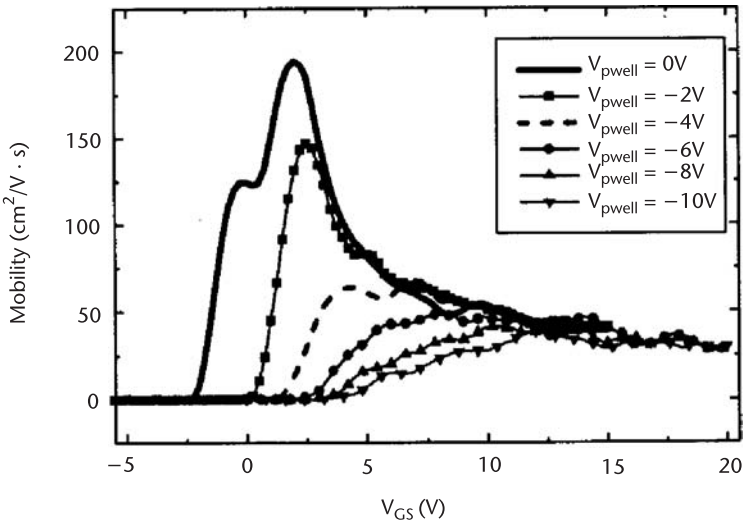


Figure 5.11 Effective channel mobility extracted from a 100 μm/100 μm lateral 4H-SiC FET with a buried channel structure. (*After:* [29].)

design is mobility degradation in the accumulation channel due to severe structural damage induced by deep heavy-dose p-type ion implantation through the low-doped n-type layer. To eliminate this problem, two approaches might be considered. First, accumulation channels can be epitaxially regrown on top of the implanted p^+ wells [38]. Another way is to use a moderate-dose p-well aluminum implantation followed by shallow compensation nitrogen implants to define an accumulation channel. Implementing this approach, reported by Agarwal et al. [29], has led to a dramatic breakthrough in improving effective channel mobility in power 4H-SiC DIMOS transistors. In this work, a thin n-type buried channel was formed by ion implantation of nitrogen with a total charge of 1.7×10^{12} cm^{-2} resulting in the channel mobility up to 195 $cm^2/V \cdot s$ (Figure 5.11). It should be noted, however, that the choice of the implantation dose for the buried channel in SiC could be very challenging because it depends on parameters that are difficult to control, such as anneal activation percentage of implanted species. In the discussed work, for example, a small "overshoot" of nitrogen dose resulted in a normally on device with V_{TH}=–2V.

Another important issue related to channel mobility in a SiC DIMOS transistor is the structural damage introduced by ion implantation. To activate impurity and repair lattice structure, a high-temperature postimplantation annealing step is required (above 1,600°C). Annealing at such high temperatures, however, can lead to outdiffusion of Si from the SiC surface, resulting in severe surface roughness. This problem can be overcome by using either different capping layers or silicon-rich ambient [39].

Dramatic improvement in channel mobility in work [29] by using a buried channel for the first time resulted in the total resistance of SiC DIMOSFET dominated by the resistance of JFET region. Design of this region, which means the choice of spacing between two adjacent p-wells, becomes a task of finding a trade-

off between the device on-resistance and its blocking capability. It can be found that the wider the spacing, the lower the JFET resistance, but also the higher field in the gate dielectric and vice versa. On the other hand, the electric field in the gate oxide can be adjusted by changing the resistance of the drift region to satisfy reliability requirements. In such a way, for a target blocking voltage, the optimal choice of the spacing between p-wells becomes an issue of finding the minimal total device resistance. Due to the two-dimensional nature of the problem, searching for such a minimum using analytical techniques becomes challenging, and numerical simulation must be employed.

Another innovation related to power SiC DMOSFET was a transistor structure, where the p-type base region was not electrically shorted to the source but could be biased independently as a p-type gate. Such a configuration, equivalent to plugging a VJFET fed from an accumulation channel in parallel with a BJT, resulted in a dramatic reduction of specific on-resistance. A schematic cross section of this device, denoted as static induction injected accumulated FET (SIAFET) and reported by Sugawara et al. in 2000 [40], is shown in Figure 5.12.

Despite poor MOS channel mobility and high pinch-off resistance, this device demonstrated breakdown voltage of 4,580V and specific on-resistance of 387 $m\Omega cm^2$, which is only 4% of the theoretical limit of Si for such voltage range. It has also demonstrated excellent dynamic characteristics, showing almost no dependence of turnoff and turn-on times on injected current [41].

Since specific on-resistance of SiC DIMOSFETs is not dominated by the drift region but rather by MOS and JFET channel resistances, it would be very beneficial to increase channel packing density. To achieve that, three different approaches can be used:

- Self-aligned fabrication process;
- High-precision lithography;
- Advanced layout solutions.

Because diffusion of impurities in SiC is impractical, SiC DIMOSFET cannot be fabricated using self-aligned processes adopted from the Si industry. On the other

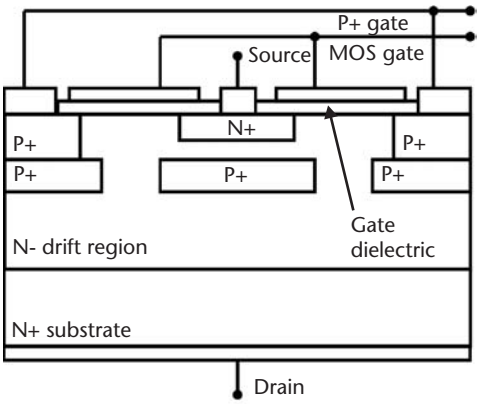


Figure 5.12 Schematic cross section of SiC SIAFET. Buried P^+ region under the source is connected to P^+ gate in third dimension.

hand, use of expensive high-precision lithography can be impractical from economical considerations. In this situation, one of the numerous cellular layout solutions from the Si industry can be used [26]. Figure 5.13 shows an example of a typical hexagonal cellular structure used in VDMOSFETs. Similar layout solutions have been reported recently in SiC power ACCUFETs to maximize channel packing density [37, 42, 43].

5.4 SiC LDMOS

The availability of a SiC Smart Power technology will have a big impact on system design in industrial, automotive, space, and aerospace applications able to operate under harsh environment conditions, such as high temperatures and high radiation levels. SiC MOSFETs have been demonstrated at operating temperatures above 600°C in 1988 [44]. Despite the fact that the first SiC integrated logic and analog circuits, based on n-channel metal oxide semiconductor (NMOS) technology, were demonstrated almost a decade ago [45, 46], the key building block of SiC Smart Power technology, 4H-SiC power lateral DMOSFET (LDMOS) was first introduced only in 1997 by Spitz et al. [47]. A schematic cross section of this device is shown in Figure 5.14. A semi-insulating substrate was used in this work to emulate semiconductor-on-insulator (SOI) technology, which is not available in SiC. The device exhibited blocking voltage of 2.6 kV, three times higher than that of the best vertical SiC devices available at that time. The 35-μm drift region between the p^+ guard ring and the drain region, which was used to reinsure high blocking voltage, has also resulted in extremely high-specific on-resistance.

As in the case of vertical devices, the drift region component of the total LDMOS' specific on-resistance depends on its dimensions and doping concentration. To reduce this component while maintaining the same blocking capability, a junction-isolation RESURF (REduced SURface Field) technology can be used. The RESURF effect is the result of the depletion region in the lateral n-type drift layer being generated by both the vertical and lateral p-n junctions. This yields a reduction of the electric field peaks that occur at the surface, leading to a considerable increase in the blocking voltage [48]. The 1.2 kV 4H-SiC lateral MOSFETs implementing RESURF technology have been published in 1999 [49]. A very high-specific on-resistance of 4 Ωcm^2 measured on these devices was caused by very low inversion

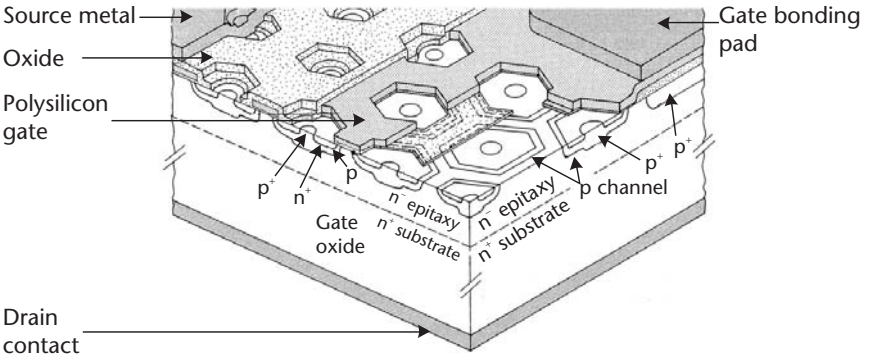


Figure 5.13 A hexagonal structure used in Si VDMOSFETs. (*After:* [26].)

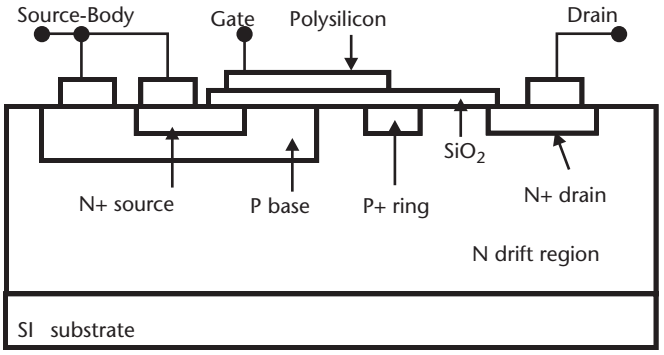


Figure 5.14 Schematic cross section of the first 4H-SiC lateral DMOSFET. (*From:* [47]. © 1998 IEEE. Reprinted with permission.)

channel mobility (~0.1-2 $cm^2/(V \cdot s)$). A gate oxide thickness of 0.9 μm led to the high blocking capability of the devices, but at the same time resulted in a very high threshold voltage. Lower voltage 600-V 6H-SiC lateral RESURF MOSFETs reported in the same year by Agarwal et al. [50] demonstrated specific on-resistance as low as 57 $m\Omega cm^2$. Because of the relatively high inversion channel mobility of 50–60 $cm^2/(V \cdot s)$, the total series on-resistance in these devices was dominated by its drift region component, which amounted to 69%. To further reduce resistance of the RESURF region by reducing its length and increasing its doping, some additional measures must be carried out to prevent electric field pinning at the sharp corners of the gate and drain electrodes. A lateral SiC DMOSFET structure implementing RESURF technology enhanced by extending the gate and drain electrodes over the field oxide was patented by Bhatnagar et al. in 1998 [51]. An example of the full utilization of this approach is given in work [39]. A schematic cross section of a reported 700-V 6H-SiC LDMOS, and a typical family of curves of a single finger device, is shown in Figure 5.15. In this design, the doping of a lateral n-type drift region was chosen to optimally spread the potential drop between the gate and the drain. When choosing the optimal nitrogen implantation (RESURF) dose for the drift region, such parameters as epi thickness and doping, as well as target blocking voltage, have been taken into consideration. Figure 5.16 shows the contour map of the simulated maximum electric field in the device as a function of epi concentration and RESURF dose for a given target blocking voltage (the implant dose is converted to the concentration in the drift region defined by a multienergy implanted box

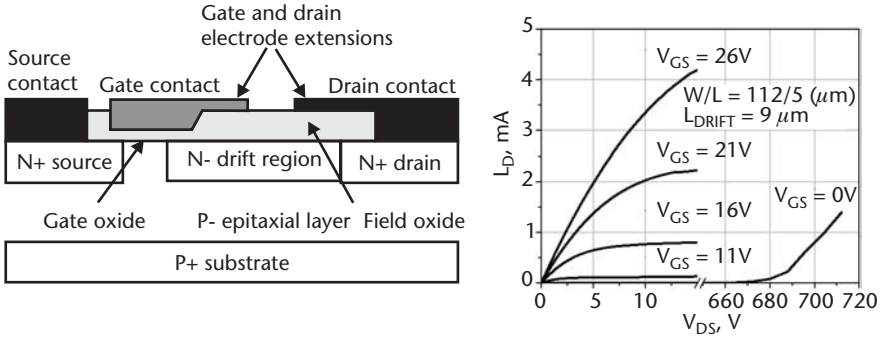


Figure 5.15 Device cross section (left) and top-view (right) of 6H-SiC LDMOS.

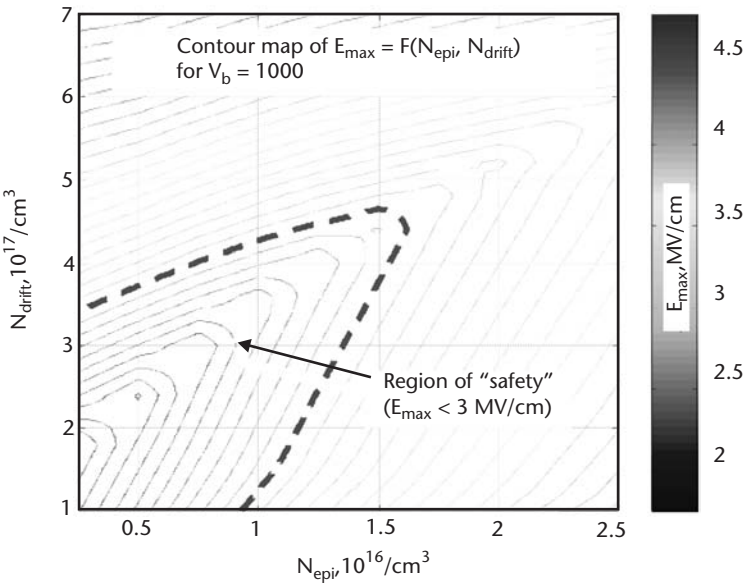


Figure 5.16 The contour map of the simulated maximum electric field in the bulk of 6H-SiC LDMOS as a function of epi concentration and the donor concentration in the implanted RESURF region for a blocking voltage of 1 kV.

profile). On this map, a region of "safety" is marked, where the electric field does not exceed its critical value in SiC, reported to be around 3 MV/cm. Since the epi doping concentration may vary in a wide range due to process immaturity for the p-type epi growth, the implantation dose should be chosen not on the border, but rather inside this region. The gate and drain electrode extensions over the field oxide (so-called field plates) have been used to suppress electric field pinning at the edges of the drift region. Simulation results of two-dimensional potential distribution in the device bulk as well as the electric field distribution along the surface of the drift region between the gate and drain electrodes are presented in Figure 5.17.

5.5 Summary and Future Development

In this chapter, we discussed different approaches used for the design and fabrication of power SiC MOSFETs, including a review of the various structures (UMOS, DMOS, and LDMOS) and process challenges associated with each structure.

By cumulative analysis of the drift region resistance and electric field distribution at the oxide/semiconductor interface in a power SiC UMOSFET, it has been shown that silicon dioxide is hardly compatible with silicon carbide in UMOS configuration. Different design solutions used to protect SiO_2 gate dielectric from a high electric field in SiC UMOSFETs resulted in dramatically complicated transistor structure, while not solving the major problem of incompatibility of the products of the dielectric constants and operating electric fields $\varepsilon_0 E_{op}$ for SiC and SiO_2. Use of emerging high-k dielectric materials such as HfO_2 for the gate dielectric is expected to realize the inherent advantages of SiC as a building material for power UMOSFETs over other semiconductors. However, this may require serious long-

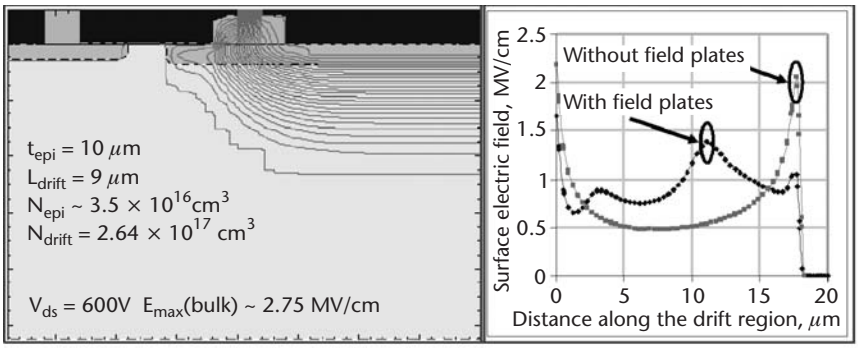


Figure 5.17 Medici simulation of 2-D potential distribution in the bulk of 6H-SiC RESURF LDMOS (left) and the surface electric field distribution with and without use of field plates (right).

term investigations to overcome possible issues related to the small conduction band offsets between SiC and high-k dielectrics and high interface state density. Meanwhile, the closest to the market power SiC MOSFET structures are vertical 4H-SiC DMOS-like transistors, which are now under intense investigation by leading SiC device developers. Increasing channel packing density by implementing self-aligned fabrication processes and advanced layout solutions in conjunction with sophisticated gate oxide growth/annealing techniques will help to overcome such traditional issues for SiC MOSFETs as inversion channel mobility and gate oxide reliability.

Significant progress has been achieved recently in the development of a power LDMOS for smart power electronics. Due to its high inversion channel mobility (several times higher than that in 4H-SiC) and relatively high electron mobility in the direction perpendicular to the *c*-axis (just 50% of that in 4H-SiC), 6H-SiC has appeared to be an excellent building material for lateral MOS devices such as LDMOS. The higher inversion channel mobility in 6H-SiC compared with that in 4H-SiC results from almost an order of magnitude lower interface state density than in 4H-SiC due to its higher conduction band offset to SiO_2. In general, the high value of the conduction band offset with related issues such as inversion channel mobility and gate oxide reliability renewed interest in alternative polytypes to 4H- and 6H-SiC such as 3C- and 15R-SiC. These polytypes also exhibit high operating electric field and high bulk electron mobility, which makes them very attractive for future SiC MOSFET development. So far, high-quality 3C- and 15R-SiC substrates are not commercially available; however, potential advantages of these polytypes as building materials for SiC MOS devices may induce future efforts toward their commercial bulk growth.

References

[1] Deboy, G., et al., "A New Generation of High Voltage MOSFETs Breaks the Limit Line of Silicon," *IEDM '98 Technical Digest,* December 6–9, 1998, pp. 683–685.

[2] Roschke, M., and F. Schwierz, "Electron Mobility Models for 4H-, 6H-, and 3C-SiC," *IEEE Trans. on Electron Devices*, Vol. 48, No. 7, July 2001, pp. 1442–1447.

[3] Chow, T. P., "SiC and GaM High-Voltage Power Switching Devices," *Mat. Science Forum*, Vol. 338–342, 2000, pp. 1155–1160.

[4] Bhatnagar, M., and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and Si for Power Devices," *IEEE Trans. on Electron Devices*, Vol. 40, Issue 3, March 1993, pp. 645–655.

[5] Palmour, J. W., H. S. Kong, and R. F. Davis, "Vertical Power Devices in Silicon Carbide," *Proc. Silicon Carbide and Related Materials*, 1994, p. 499.

[6] Agarwal, A. K., et al., "A Critical Look at the Performance Advantages and Limitations of 4H-SiC Power UMOSFET Structures," *Proc. of 8th Intl. Symposium on Power Semiconductor Devices and ICs,* May 23, 1996, pp.119–122.

[7] Agarwal, A. K., et al., "SiC Electronics," *Intl. Electron Device Meeting*, December 8–11, 1996, pp. 225–230.

[8] Agarwal, A. K., S. Seshadri, and L. B. Rolland, "Temperature Dependence of Fowler-Nordheim Current in 6H- and 4H-SiC MOS Capacitors," *IEEE Electron Device Letters*, Vol. 18, Issue 12, December 1997, pp. 592–594.

[9] Morisette, D. T., and J. A. Cooper, Jr., "Theoretical Comparison of SiC PiN and Schottky Diodes Based on Power Dissipation Considerations," *IEEE Trans. on Electron Devices*, Vol. 49, No. 9, September 2002, pp. 1657–1664.

[10] Sridevan, S., P. K. McLarty, and B.J. Baliga, "Analysis of Gate Dielectrics for SiC Power UMOSFETS," *IEEE Intl. Symposium on Power Semiconductor Devices and ICs 1997, ISPSD '97*, May 26–29, 1997, pp. 153–156.

[11] Lipkin, L. A., and J. W. Palmour, "Insulator Investigation on SiC for Improved Reliability," *IEEE Trans. on Electron Devices*, Vol. 46, Issue 3, March 1999, pp. 525–532.

[12] *Medici Two-Dimensional Device Simulation Program Version 2002, User's Manual*, Avanti Corporation, TCAD Businenti Corporation, TCAD Business Unit, Fremont, CA, July 2000.

[13] Iwai, H., and S. Ohmi, "CMOS Downsizing and High-k Insulator Technology," *Fourth IEEE Intl. Caracas Conference on Devices, Circuit and Systems,* Aruba, April 17–19, 2002, pp. D049-1–D049-8.

[14] Wang, X. W., et al., "High Temperature (450°C) Reliable NMISFET's on p-Type 6H-SiC," *Intl. Electron Device Meeting*, December 5–8, 1999, pp. 209–212.

[15] Zetterling, C. -M., et al., "SiC MISFETs with MBE-Grown AlN Gate Dielectric," *Mat. Sci. Forum*, Vol. 338–342, 2000, pp. 1315–1318.

[16] Robertson, J., "Electronic Structure and Band Offsets in High-K Oxides," *IWGI 2001, Tokio*, pp. 76–77.

[17] Tan, J., et al., "Metal-Oxide-Semiconductor Capacitors Formed by Oxidation of Polycrystalline Silicon on SiC," *Appl. Phys. Lett.*, Vol. 70, 1997, p. 2280.

[18] Li, Y., J. A. Cooper, Jr., and M. A. Capano, "High-Voltage (3 kV) UMOSFETs in 4H-SiC," *IEEE Trans. on Electron Devices*, Vol. 49, Issue 6, June 2002, pp. 972–975.

[19] Peters, D., et al., "4H-SiC Power MOSFET Blocking 1200V with a Gate Technology Compatible with Industrial Applications," *European Conference on Silicon Carbide and Related Materials,* September 1–5, 2002.

[20] Sugawara, Y., and K. Asano, "1.4 kV 4H-SiC UMOSFET with Low Specific On-Resistance," *Proc. of the 10th Intl. Symposium on Power Semiconductor Devices and ICs, ISPSD '98*, June 3–6, 1998, pp. 119–122.

[21] Ramungul, N., et al., *Digest of 54th Annual Device Research Conference*, June 24–26, 1996, pp. 56–57.

[22] Ogino, S., T. Oikawa, and K. Ueno, "Channel Doped SiC-MOSFETs," *Mat. Sci. Forum*, Vol. 338–342, 2000, pp. 1101–1104.

[23] Zhao, J., et al., "3.6 $m\Omega cm^2$, 1726V 4H-SiC Normally-Off Trenched-and-Implanted Vertical JFETs," *Proc. of 15th Intl. Symposium on Power Semiconductor Devices and ICs*, April 14–17, 2003, pp. 50–53.

[24] Hara, K., "Vital Issues for SiC Power Devices," *Materials Science Forum,* Vol. 264–268, Part 2, 1998, pp. 901–906.

[25] Li, Y., J. A. Cooper, Jr., and M. R. Melloch, "High-Voltage Accumulation-Layer UMOSFETs in 4H-SiC," *IEEE Electron Device Letters*, Vol. 49, Issue 6, June 2002, pp. 487–489.

[26] Grant, D. A., and J. Gowar, *Power MOSFETs: Theory and Applications*, New York: Wiley-Interscience, 1989.

[27] Casady, J. B., et al., "Silicon Carbide Power MOSFET Technology," *IEEE Intl. Symposium on Compound Semiconductors*, September 8–11, 1997, pp. 359–362.

[28] Shenoy, J. N., J. A. Cooper, Jr., and M. R. Melloch, "High-Voltage Double-Implanted Power MOSFETs in 6H-SiC," *IEEE Electron Device Letters*, Vol. 18, Issue 3, March 1997, pp. 93–95.

[29] Agarwal, A., et al., "Large Area 4H-SiC Power MOSFETs," *Proc. of the 13th Intl. Symposium on Power Semiconductor Devices and ICs*, June 4–7, 2001, pp. 183–186.

[30] Sei-Hyung, R., et al., "10A, 2.4 kV Power DiMOSFETs in 4H-SiC," *IEEE Electron Device Letters*, Vol. 23, Issue 6, June 2002, pp. 321–323.

[31] Chung, G. Y., et al., "Improved Inversion Channel Mobility for 4H-SiC MOSFETs Following High-Temperature Anneals in Nitric Oxide," *IEEE Electron Device Letters*, Vol. 22, Issue 4, April 2001, pp. 176–178.

[32] Schörner, R., et al., "Enhanced Channel Mobility of 4H–SiC Metal–Oxide–Semiconductor Transistors Fabricated with Standard Polycrystalline Silicon Technology and Gate-Oxide Nitridation," *Applied Physics Letters,* Vol. 80, No. 22, June 3, 2002, p. 176.

[33] Chung, G. Y., et al., "Effect of Nitric Oxide Annealing on the Interface Trap Densities Near the Band Edges in the 4H Polytype of Silicon Carbide," *Applied Physics Letters*, Vol. 76, No. 13, March 27, 2000, p. 1713.

[34] Hui-Feng, L., et al., "Analysis of Fowler-Nordheim Injection in NO Nitrided Gate Oxide Grown on n-Type 4H-SiC," *Microelectronics Reliability*, Vol. 40, No. 2, February 2000, pp. 283–286.

[35] Baliga, B. J., "Silicon Carbide Semiconductor Devices Having Buried Silicon Carbide Conduction Barrier Layers Therein," United States Patent 5543637, August 6, 1996.

[36] Shenoy, P. M., and B. J. Baliga, "The Planar 6H-SiC ACCUFET: A New High-Voltage Power MOSFET Structure," *IEEE Electron Device Letters*, Vol. 18, Issue: 12, December 1997, pp. 589–591.

[37] Singh, R., S. -H. Ryu, and J. W. Palmour, "High Temperature, High Current, 4H-SiC Accu-DMOSFET," *Mat. Sci. Forum*, Vol. 338–342, 2000, pp. 1271–1274.

[38] Singh, R., et al., "Development of High-Current 4H-SiC ACCUFET," *IEEE Trans. on Electron Devices*, Vol. 50, Issue 2, February 2003, pp. 471–478.

[39] Sankin, I., et al., "On Development of 6H-SiC LDMOS Transistors Using Silane-Ambient Implant Anneal," *Solid-State Electronics*, Vol. 45, No. 9, September 2001, pp. 1653–1165.

[40] Sugawara, Y., et al., "4.5 kV Novel High Voltage High Performance SiC-FET SIAFET," *Proc. on the 12th Intl. Symposium on Power Semiconductor Devices and ICs*, May 22–25, 2000, pp. 105–108.

[41] Takayama, D., et al., "Static and Dynamic Characteristics of 4–6 kV 4H-SiC SIAFETs," *Proc. of the 13th Intl. Symposium on Power Semiconductor Devices and ICs, ISPSD '01*, June 4–7, 2001, pp. 41–44.

[42] Onda, S., R. Kumar, and K. Hara, "SiC Integrated MOSFETs," *Physica Status Solidi (A) Applied Research,* Vol. 162, No. 1, July 1997, pp. 369–388.

[43] Nallet, F., et al., "Very Low R_{ON} Measured on 4H-SiC Accu-MOSFET High Power Device," *Proc. of the 14th Intl. Symposium on Power Semiconductor Devices and ICs*, June 4–7, 2002, pp. 209–212.

[44] Palmour, J. W., H. S. Kong, and R. F. Davis, "Characterization of Device Parameters in High-Temperature Metal-Oxide-Semiconductor Field-Effect Transistors in β-SiC Thin Films," *J. of Applied Physics*, Vol. 64, No. 4, August 15, 1988, pp. 2168–2177.

[45] Xie, W., M. R. Cooper, Jr., and M.R. Melloch, "Monolithic NMOS Digital Integrated Circuits in 6H-SiC," *IEEE Electron Device Letters,* Vol. 15, No. 11, November 1994, pp. 455–457.

[46] Brown, D. M., et al., "High Temperature Silicon Carbide Planar IC Technology and First Monolithic SiC Operational Amplifier IC," *Trans. of 2nd Intl. High-Temp. Elec. Conf. (HiTEC)*, 1994, pp. XI-17–XI-22.

[47] Spitz, J., et al., "2.6 kV 4H-SiC Lateral DMOSFET's," *IEEE Electron Device Letters*, Vol. 19, No. 4, April 1998, pp. 100–102.

[48] Popescu, A., et al., "Analytical Modeling for the RESURF Effect in JI and SOI Power Devices," *IEE Proc.-Circuits Devices Systems*, Vol. 149, No 516, October/December 2002, pp. 273–284.

[49] Chatty, K., et al., "Nitrogen vs. Phosphorus as Implant Species for High-Voltage Lateral RESURF MOSFETs on 4H-SiC," *Mat. Sci. Forum*, Vol. 338–342, 2000, pp. 1279–1282.

[50] Agarwal, A. K., et al., "Investigation of Lateral RESURF, 6H-SiC MOSFETs," *Mat. Sci. Forum*, Vol. 338–342, 2000, pp. 1307–1310.

[51] Bhatnagar, M., C. E. Weitzel, and M. Zunino, "Lateral MOSFET with Modified Field Plates and Damage Areas," U.S. Patent 5710455, January 20, 1998.

CHAPTER 6

Power and RF BJTs in 4H-SiC: Device Design and Technology

Anant Agarwal, Sei-Hyung Ryu, and John Palmour

6.1 Introduction

The Si IGBT is the most widely used power switch today. It is available from 600V to about 6,500V with current ratings of up to a few hundred amperes in a single chip. It is easy to drive since it has a MOS input gate, which does not draw any dc current. However, Si technology has matured to a point where the fundamental physical limits have been reached. Thus, other semiconductor materials such as SiC are of interest. SiC has some useful properties such as high critical electric field, high thermal conductivity, and high-temperature device operation. These properties are ideal for power devices. There are several device structures that can be used for power switching in SiC. The possible power device switch structures in SiC include power MOSFET, BJT, IGBT, GTO thyristor, and JFET. For very high voltage SiC devices (3,000V), MOSFET and JFET are inappropriate due to the unipolar nature of forward conduction and therefore the high-specific on-resistance. GTO is a latching-type device and the circuit designers do not have continuous control on its on-characteristics. This makes it unsuitable for kV applications. IGBT is not yet practical in SiC due to issues with p-type substrate and poor inversion layer electron mobility of n-channel MOSFET in SiC. This leaves SiC BJT as a most useful device for 3–10-kV applications. A potential disadvantage with the BJT is that it requires a high input base current for control. Therefore, improving the current gain of the SiC BJT is extremely important. This issue is discussed in detail in subsequent sections.

6.2 Device Structures and Operation of Power BJTs

The first BJT in SiC was reported by Muench et al. in 1977 [1]. The pn junctions were formed by growing p-type and n-type epilayers, and the emitter and base regions were then isolated using dry etching techniques. The device had a common emitter gain of 4, which remained the highest reported until Palmour et al. demonstrated the first power BJTs in 6H-SiC in 1993 [2]. These devices demonstrated a blocking voltage of 200V, and a common emitter current gain of 10.4 at RT. The current gain of this device decreased at elevated temperatures up to 250°C (7.8 at 250°C), then increased for temperatures greater than 250°C (10.2 at 400°C). Being

a current-controlled device, however, the SiC BJT did not receive much attention despite its excellent electrical characteristics, until the first high-voltage BJTs in 4H-SiC were reported by Ryu et al. in June 2000 [3]. The devices used an n^+ epilayer as the emitter layer and a p-type epilayer for the base layer. The emitter and base regions are formed by RIE etching of the two epilayers, resulting in an epitaxial emitter structure shown in Figure 6.1(a). Due to its simplicity in fabrication processing, the epitaxial emitter structure became very popular in SiC BJTs and was used in several subsequently reported 4H-SiC BJTs [4, 5]. The BJTs in [3] showed a common emitter current gain of 20, a specific on-resistance of 10.8 mΩ-cm^2, and a collector current of 3.8A (271 A/cm^2) at room temperature. A BV_{CBO} of 2.2 kV, which is 71% of the ideal breakdown voltage of the collector epilayer, and a BV_{CEO} of 1.8 kV were measured from the device.

Due to the lack of a shallow acceptor level in 4H-SiC and a relatively low hole mobility, the intrinsic base resistance of a 4H-SiC BJT is very high; for example, a base epilayer sheet resistance of 46 kΩ per square was reported for a 4H-SiC BJT in [6]. The high intrinsic base resistance in 4H-SiC BJTs results in a very severe emitter current crowding effect [7], which limits most of the current flow to within 1 μm from the edge of the emitter regions [8]. This indicates that tight cell pitches are necessary to achieve a low specific on-resistance, as shown in Figure 6.2(a) [6].

As discussed, 4H-SiC BJTs suffer from severe emitter current crowding. For epitaxial emitter structures, this means most of the current flows very close to the etched mesa sidewalls, therefore, the surface trap density at the etched sidewalls has a significant effect on the electrical characteristics of 4H-SiC BJTs. Figure 6.2(b) shows the common emitter current gains of 4H-SiC BJTs with three different cell pitches (14, 23, 35 μm) [6]. It is shown that the current gain is the lowest for the devices with the smallest cell pitch, which has the highest mesa sidewall density. This indicates a high-quality surface passivation is required for high-performance 4H-SiC BJTs. Recently, it was reported that the nitridation of SiO_2 on 4H-SiC surfaces using NO [9] or N_2O [10] results in a significant reduction of MOS surface state density in

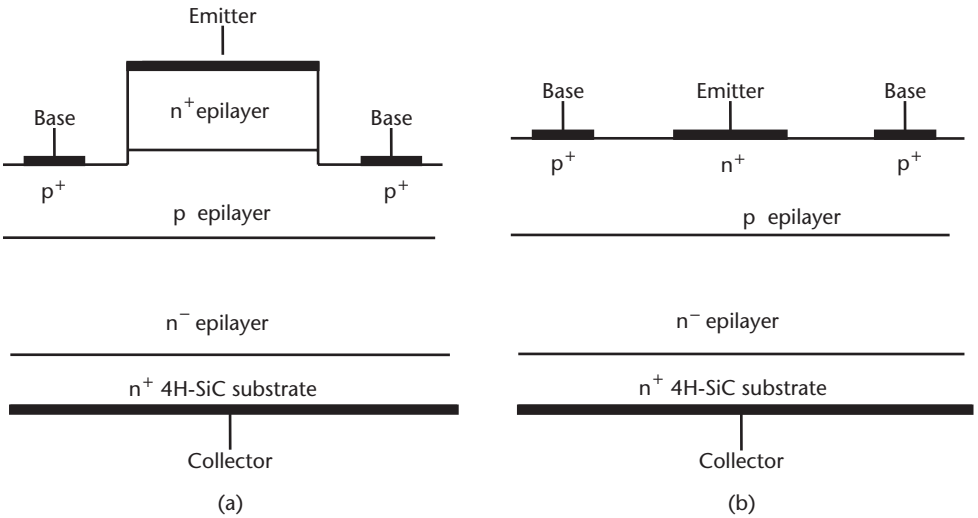


Figure 6.1 (a) Cross sections of an epitaxial emitter BJT. (b) Implanted emitter BJT in 4H-SiC.

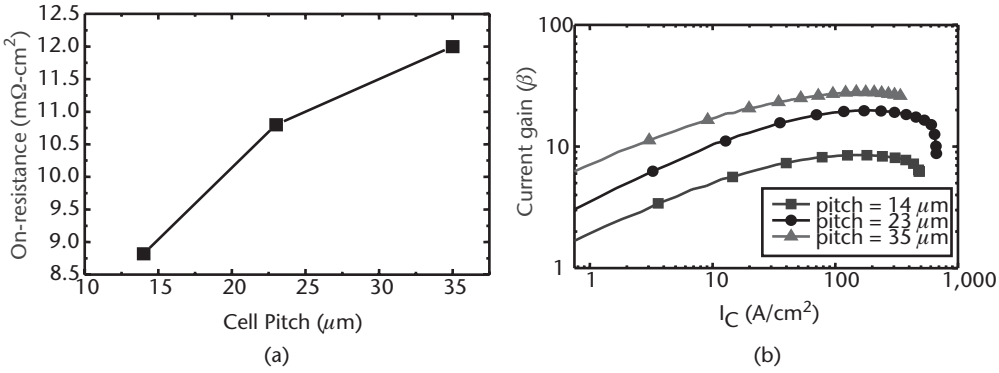


Figure 6.2 (a) Specific on-resistance of epitaxial emitter 4H-SiC BJTs as a function of cell pitch. (b) Effect of cell pitch on common emitter current gain. (*From:* [6]. © 2001 IEEE. Reprinted with permission.)

4H-SiC. These nitridation techniques were applied to 4H-SiC BJTs with epitaxial emitters for sidewall surface passivation [11, 12], resulting in common emitter current gain (β) of greater than 50 [11]. However, the base doping was extremely low in these devices and could also explain the higher values of β due to higher emitter injection efficiency. A series of devices were measured for β with different emitter-to-base contact spacings, as shown in Figure 6.3(a) [11]. The results are shown in Figure 6.3(b). It is observed that β increases with increasing emitter-to-base contact spacings and saturates around 3–4 μm, which is about one diffusion length for electrons in the base. This clearly indicates that the p^+ implant creates a damaged region with a high density of recombination centers, which then reduce the current gain by establishing a strong parasitic base-to-emitter diffusion current component in addition to the main current components.

The 4H-SiC BJTs with implanted emitter regions [Figure 6.1(b)] have also been investigated. The first 4H-SiC BJT, with implanted emitter, was reported by Tang et al. in June 2000 [13]. The emitter regions of the device were formed by implanting phosphorus ions into 1-μm-thick p-type epilayer (2×10^{17} cm^{-3}) grown on 12-μm-thick n-type collector epilayer with a doping concentration of 4×10^{15} cm^{-3}. A p^+ epilayer was grown in p base epilayer, which is then selectively etched to form p^+ contact regions to the base. The device showed an impressive common emitter current gain of 36. However, the blocking voltage of the device was very low (BV_{CEO} = 40V, BV_{CBO} = 160V) because of the punch-through effect [7]. Subsequently, the same group successfully developed a high-voltage (500V) 4H-SiC BJT with an implanted emitter structure [14]. The higher blocking voltage was achieved by increasing the base width, therefore preventing the punch-through effect. However, the peak common emitter current gain of the device was 8, which is substantially lower than the value reported in [12] or other values reported for 4H-SiC BJTs with epitaxial emitter structures. This is caused by a large number of implant-induced defects at the emitter-base pn junction, which trap carriers at and near the space-charge region of the emitter-base pn junction and reduce the emitter injection efficiency, as illustrated in Figure 6.4. A comparison of epitaxial emitter structure and implanted emitter structure was made in [15] (Figure 6.5). It is shown that the

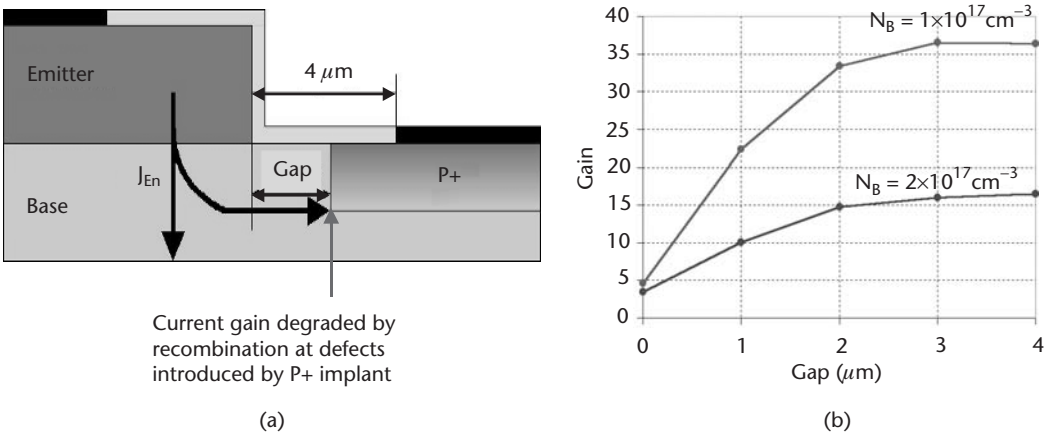


Figure 6.3 (a) Defects generated by P^+ implant cause degradation in current gain through recombination. (b) Effect of emitter-to-base spacing on common emitter current gain. (*From:* [11]. © 2004 IEEE. Reprinted with permission.)

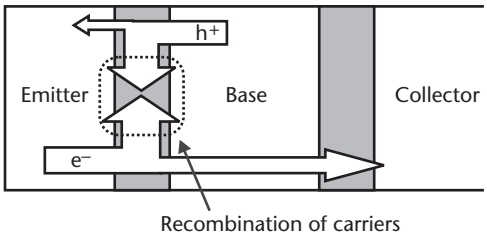


Figure 6.4 Carrier flow in implanted emitter 4H-SiC BJTs. Most of the electrons injected from the emitter are recombined at or near the SCR of the emitter-base pn junction.

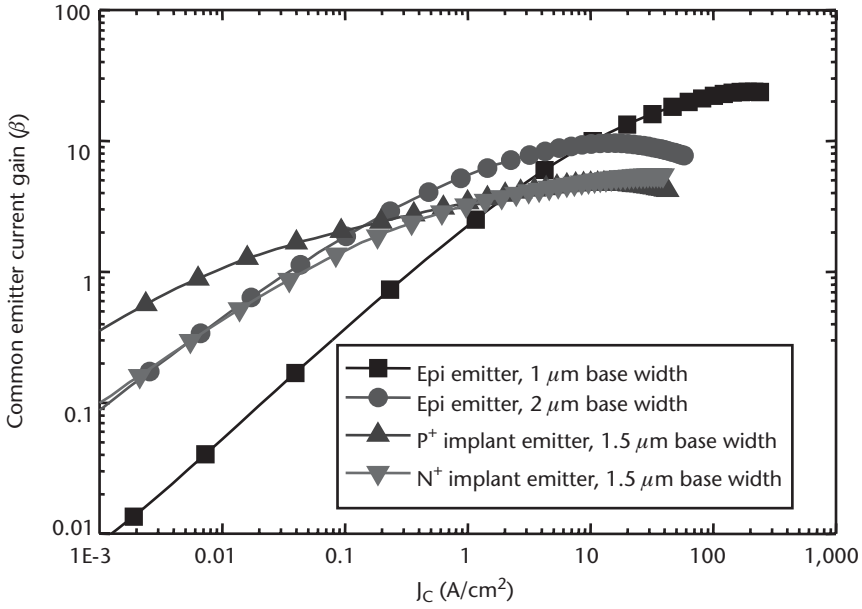


Figure 6.5 Common emitter current gains of epitaxial emitter and implanted base emitter 4H-SiC BJTs.

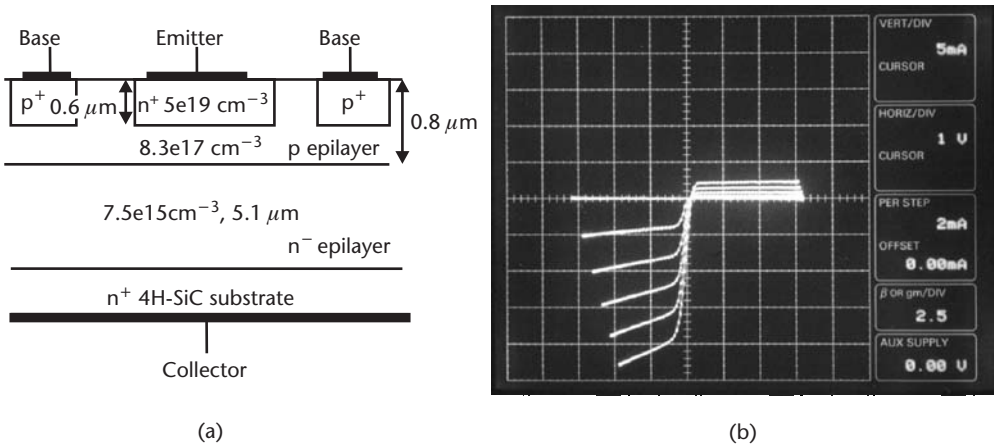
current gain of the implanted emitter BJTs with 1.5-μm base thickness, regardless of the implanted species (phosphorus or nitrogen), is approximately 5, whereas the current gain of epi emitter BJT with 2-μm base thickness is approximately 10. Even with a thicker base, the epitaxial emitter BJTs showed superior performance over the implanted emitter BJTs.

A more direct comparison of epitaxial emitter versus implanted emitter structures can be made by observing the reverse-active and forward-active regions of the I-V characteristics of an implanted emitter BJT. Figure 6.6 shows the structure of an implanted emitter 4H-SiC BJT and its I-V characteristics. The 0.6-μm deep emitter regions were formed by nitrogen implantations into 0.8-μm-thick, 8.3×10^{17} cm^{-3} doped p-type base layer, which was grown on 7.5×10^{15} cm^{-3} doped, 5.1-μm-thick n-type collector layer. In the forward-active region, the device shows a peak current gain of 0.6, whereas a peak current gain of 2.5 is measured in the reverse-active region. This is because the collector-base pn junction has greater injection than the implanted emitter-base pn junction, even though the doping concentration of the collector layer is two orders of magnitude lower than that of the base layer. The base transport factor is assumed to be equal because the same base layer is used for both forward- and reverse-active regions. This result proves that in 4H-SiC, the epitaxially formed pn junctions offer far superior charge injection to the implanted pn junctions and are more suitable to form emitter-base pn junctions in 4H-SiC BJTs. In this chapter, the focus will be exclusively on the epitaxial emitter 4H-SiC BJT because of its superior performances and simplicity in structure and fabrication processes.

6.3 Design of the Epitaxial Power BJT

6.3.1 Design of the Collector Layer

The blocking voltage of a power BJT is supported by the collector layer. In Si power BJTs, it is known that a very low specific on-resistance can be achieved due to the conductivity modulation in the lightly doped collector epilayer. However, none of



(a) (b)

Figure 6.6 (a) Structure of an implanted emitter BJT. (b) I-V characteristics of an implanted emitter 4H-SiC. The device shows greater common emitter current gain in the reverse-active region.

the previously reported 4H-SiC power BJTs has demonstrated conductivity modulation in the collector layer. Therefore, the on-resistance of a 4H-SiC BJT is very close to the drift resistance of its collector layer, which can be significant depending on the blocking voltage. The goal of the design process is to minimize the drift resistance of the collector epilayer for a given blocking voltage. This is generally achieved by the punch-through design, in which the depletion region reaches through the n-type drift layer before the breakdown occurs.

In this case, the open-emitter breakdown voltage, BV_{CBO}, is calculated as an area under the E versus x plot (Figure 6.7) and is given by:

$$BV_{CBO} = E_c \cdot d - \frac{qN_D d^2}{2\varepsilon_s} \tag{6.1}$$

where E_C is the critical electric field in 4H-SiC, d is the drift layer thickness, N_D is the doping density in the collector layer, and ε_s is the permittivity of SiC.

The specific on-resistance of the collector layer is simply given by,

$$R_{drift} = \frac{d}{q\mu_n N_D} \tag{6.2}$$

where μ_n is the bulk electron mobility in the drift layer. Eliminating N_D from (6.1) and (6.2), we get

$$R_{drift} = \frac{d^3}{2\mu_n \varepsilon_s (E_C d - BV_{CBO})} \tag{6.3}$$

It can be shown from (6.3) that R_{drift} is minimum when,

$$d_{optimum} = \left(\frac{3}{2}\right)\frac{BV_{CBO}}{E_C} \tag{6.4}$$

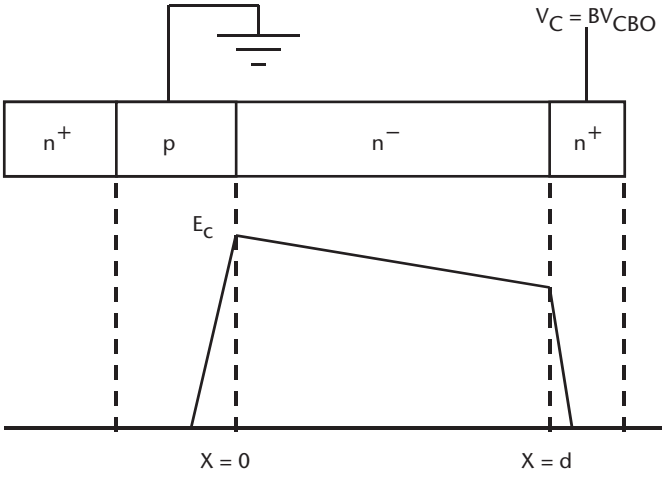


Figure 6.7 Electric field versus distance profile for the punch-through collector design.

Thus, the minimum value of R_{drift} is given by,

$$R_{drift,optimum} = \left(27/8\right)\frac{BV_{CBO}^2}{\mu_n \varepsilon_s E_C^3} \tag{6.5}$$

The blocking capability of a power BJT is generally determined by the open-base breakdown voltage (BV_{CEO}) of the device. The BV_{CEO} is usually much smaller than the BV_{CBO} of the device, and the relationship between the BV_{CBO} and BV_{CEO} is given in (6.6) [7].

$$BV_{CEO} = BV_{CBO} \cdot \left(1-\alpha_0\right)^{1/n} \tag{6.6}$$

where α_0 is common base current gain and n is a constant. This behavior is well understood in Si BJTs. However, it is difficult to predict BV_{CEO} of a 4H-SiC BJT. Generally, the BV_{CEO} of a 4H-SiC power BJT is assumed to be 50% of the theoretical BV_{CBO} of the device. In the previously reported epitaxial emitter 4H-SiC BJTs, the BV_{CEO} of the devices ranged from 40% [5] to 60% [16] of the ideal parallel plate breakdown voltage of the collector layer, assuming an E_c of 2 MV/cm.

6.3.2 Design of the Base Layer

The design of the base layer plays an important role in determining the performance of the power BJT. First, the base layer should contain enough charge, so that it can support a very high field in the blocking state and prevent emitter-collector punch-through. In 4H-SiC power BJTs, a sheet charge density (doping concentration × layer thickness) of at least 1×10^{13} cm^{-2}, which is enough to support an electric field of 2 MV/cm, is provided in the base layer to accomplish this goal. Second, to achieve a high common emitter current gain, the thickness of the base layer should be less than the minority carrier diffusion length (L_n). L_n is proportional to minority carrier lifetime (τ_n) in the base, which can be reduced for higher impurity concentration. Third, the resistance of the base layer should be reasonably low because a lower base resistance results in higher switching speeds and reduced emitter current crowding effect [7]. The first condition suggests that a thicker base layer with higher doping concentration should be used, whereas the second condition dictates that a thinner base layer with lower doping concentration should be used. A careful compromise must be made to meet both conditions. Since the third condition is not as critical as the first two conditions, it will not be considered.

A typical base layer of a 4H-SiC power BJT has a base layer thickness of approximately 1 μm and a doping concentration ranging from 1×10^{17} to 2×10^{17} cm^{-3}. This corresponds to a sheet charge ranging from 1×10^{13} to 2×10^{13} cm^{-2}, which satisfies the first condition. Next, the diffusion length can be calculated from τ_n and mobility. A typical value of τ_n measured using photoluminescence technique for a similarly doped epilayer is approximately 40 ns, and the electron mobility of 200 cm^2/V · s can be assumed for given doping concentration [17]. A diffusion length of 4.5 μm, which is 4.5 times that of the base layer thickness, can be obtained, and the second condition is also satisfied.

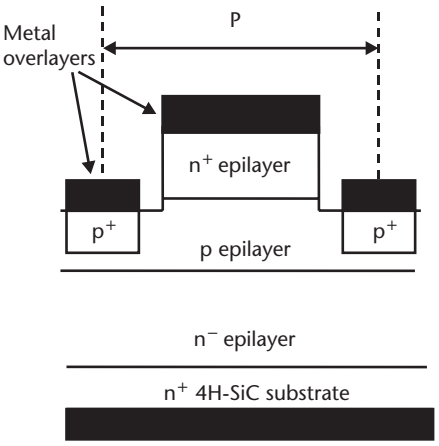


Figure 6.8 Simplified cross section of a unit cell of a 4H-SiC power BJT.

6.3.3 Design of the Unit Cell

Figure 6.8 shows a simplified cross section of a unit cell of a 4H-SiC power BJT. The cell pitch, P, is given by the sum of width of the emitter mesa, width of the p^+ base implant, and the total base-to-emitter spacings. An example of the device layout is shown in Figure 6.9. The goal of unit cell design is to minimize the cell pitch, since most of the current flows along the sidewalls of emitter mesas. It is important to maximize the density of emitter mesa sidewall density without compromising the performance of the transistor.

Recently, the correlation between the common emitter current gain and the spacing between the emitter mesa and the base implants for epitaxial emitter 4H-SiC BJTs was reported [11]. It was shown that the common emitter current gain decreases if the emitter mesa-base implant spacing is less or equal to the diffusion length, in this case, approximately 4.5 μm, because of the implant-induced damage. Further increase in emitter mesa-to-base implant spacing did not result in higher current gains, suggesting the optimal spacing from the emitter mesa to base implant is about 5 μm. However, this will result in an increased base resistance and an enhanced emitter current crowding.

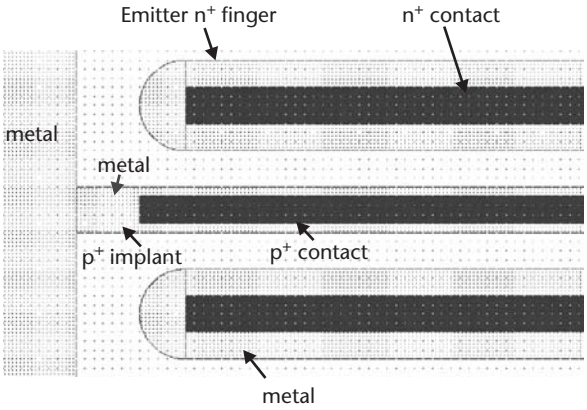


Figure 6.9 A sample layout of a 4H-SiC power BJT. (*From:* [16]. © 2004 IEEE. Reprinted with permission.)

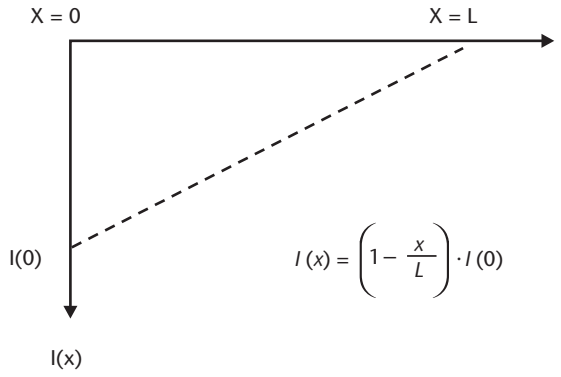


Figure 6.10 Distribution of lateral current flow in the emitter metal over layer along the length of an emitter finger.

For devices with an interdigitated finger design, as shown in Figure 6.9, care must be taken so that the resistive voltage drop along the emitter and base fingers is less than kT/q, otherwise, parts of the device will not turn on because of debiasing of the emitter-base pn junction. The thickness of metal that can be patterned is limited by the process technology. The lengths and the widths of emitter and base fingers should be selected so that the total voltage drops from one end to the other are less than kT/q.

Figure 6.10 shows the distribution of lateral current flow in the emitter metal overlayer along the length of an emitter finger, assuming a uniform vertical current flow within the device. The total voltage drop can be obtained by integrating voltage drop in the metal layer as follows:

$$V = \frac{\rho}{W \cdot t} \cdot \int_0^L I(x)dx = \frac{\rho \cdot I(0)}{W \cdot t} \cdot \int_0^L \left(1 - \frac{x}{L}\right)dx = \frac{\rho \cdot I(0) \cdot L}{2 \cdot W \cdot t} = \frac{\rho \cdot J_C \cdot P \cdot L^2}{2 \cdot W \cdot t} \tag{6.7}$$

where P is the cell pitch, J_C is the collector current density, $I(0)$ is the total current flowing through the emitter finger, ρ is the resistivity of the metal layer, W is the width of the metal layer (or emitter finger), t is the thickness of the metal layer, and L is the length of the emitter finger.

For example, the interdigitated design shown in Figure 6.9 has the following parameters: P is 23 μm, W is 10 μm, t is 3 μm, L is 1.2 mm, and Au ($\rho = 2.2 \times 10^{-6}$ Ω-cm) is used for the metal overlayer. For a collector current density of 200 A/cm^2, the total voltage drop along the length of an emitter finger is 24.2 mV, which is less than kT/q (26 mV) at RT.

Debiasing of emitter-base pn junction can be minimized by using a double metal process. A simplified cross section of a 4H-SiC power BJT with double metal process is shown in Figure 6.11. In this structure, the emitter electrode covers most of the active area and is connected to emitter fingers through vias, whereas the base electrode is placed outside of the active area. Use of this structure eliminates most of the resistive voltage drop in the emitter fingers at an increased cost of the fabrication process.

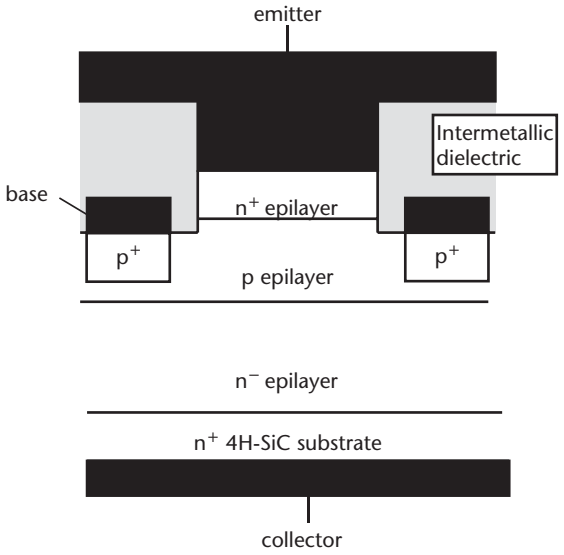


Figure 6.11 Simplified cross section of a unit cell of a 4H-SiC power BJT with a double metal process.

6.4 Process Integration

6.4.1 Process Sequence

Figure 6.12 shows a simplified fabrication process sequence of 4H-SiC power BJT with epitaxial emitters. All required epilayers are grown before the fabrication process begins [Figure 6.12(a)]. The lightly doped n-type collector layer is grown on the Si-face of an n^+ 4H-SiC silicon carbide substrate. Since the collector layer supports the blocking voltage of the BJT, the doping and thickness of this layer is selected so that the peak field in SiC is approximately 2 MV/cm in the blocking mode. About 1-μm-thick p-type base layer with doping concentrations ranging from 1×10^{17} cm^{-3} to 2×10^{17} cm^{-3} is then grown on the collector layer. Finally, a heavily doped (1×10^{19} cm^{-3} – 5×10^{19} cm^{-3}) n-type epilayer, with a thickness ranging from 0.75 μm to 1 μm, is grown on the p-type base layer as the emitter layer.

First, the n^+ emitter epilayer is selectively etched using dry etching techniques to isolate n^+ emitter regions. The alignment marks are formed at this level. The base regions are then isolated by selectively etching the p-base epilayer using dry etching techniques [Figure 6.12(b)]. Then, p-type species, preferably aluminum, are implanted to form p^+ contact regions in the base. The floating guard ring termination structure can be implemented at this step if desired [Figure 6.12(c)]. The implants are then activated at a temperature greater than 1,550°C. During the high-temperature implant activation, a silicon overpressure [18, 19] must be provided in the ambient to suppress surface roughening.

A thick (> 1 μm) field oxide layer is formed after the implant activation. The field oxide is generally deposited using low-pressure CVD (LPCVD) or plasma-enhanced CVD (PECVD) process because the Si-face of SiC has very low oxidation rate and because consumption of the implanted layer must be minimized. The field oxide layer is then patterned by selectively etching to remove all oxide from the

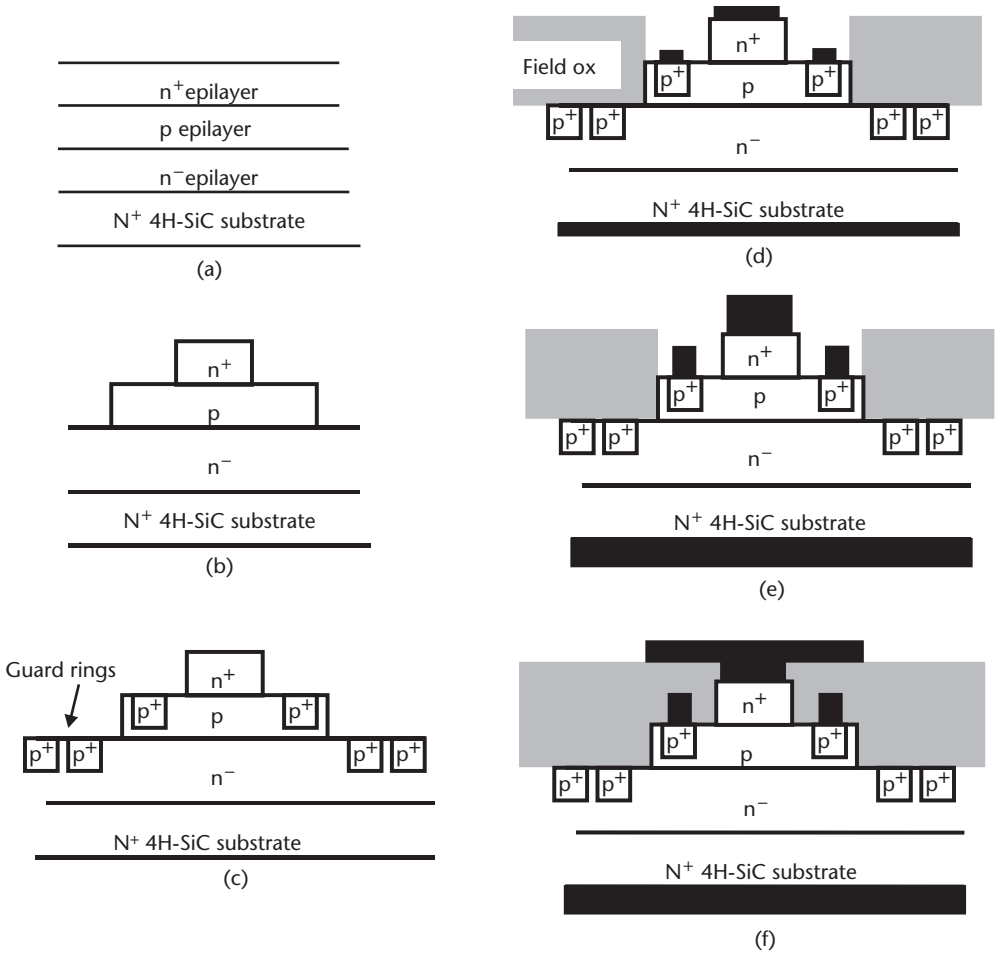


Figure 6.12 Cross-sectional view of the 4H-SiC power BJT fabrication. (a) Starting epilayer structure. (b) Dry etching of emitter and base epilayers. (c) p^+ implantation for guard rings and contacts to p-base. (d) Formation of ohmic contacts. (e) Over layer metal deposition. (f) Double metal process.

active areas, then a MOS gate quality surface passivation layer is formed using either thermally grown oxide layer or densified LPCVD oxide. This passivation layer can be nitrided using NO [9] or N_2O [10] to further reduce the surface trap density, so that higher common emitter current gains can be achieved [11, 12]. The contacts are formed by removing oxide layers from the contact regions (both n^+ and p^+) and the backside of the wafer and depositing metal [Figure 6.12(d)]. Ni is the most commonly used metal for ohmic contacts to n-type 4H-SiC. For p-type ohmic contacts, Ni [6], Ti [16], or Al/Ti [5, 11, 12] can be used. The contacts are generally annealed at temperatures greater than 650°C to achieve ohmic properties. Finally, thick (1–6 μm) metal layers, such as Al or Ti/Pt/Au stack, are deposited and patterned as the final metal over layers [Figure 6.12(e)].

A double metal process can be used to reduce the cell pitch and minimize parasitic resistance and capacitance, which can be critical for 4H-SiC BJTs intended for high-frequency operations. The finished structure in Figure 6.12(e) can be covered with an intermetallic dielectric layer. Via holes are then opened, and a thick metal

layer, such as Al or Ti/Pt/Au stack, is deposited and patterned to form emitter and base electrodes [Figure 6.12(f)].

6.5 1.2-kV Power BJTs

A simplified device structure of the NPN BJT is shown in Figure 6.13 with a pitch of 23 μm [20]. Emitter fingers were 10 μm long, base contacts were 3 μm long, and emitter-to-base contact spacing was designed to be 5 μm to minimize recombination and improve the current gain. The overall dimensions of the device, including the guard ring edge termination, were 3.38 mm × 3.39 mm with an active area of 0.09 cm^2. The n-type collector layer was 15 μm thick, doped at 4.4×10^{15} cm^{-3} and the p-base layer was 1 μm thick, doped at 2×10^{17} cm^{-3}. The n^+ emitter layer was 0.75 μm thick. A double metal process was used as discussed in Section 6.4. The emitter fingers were isolated by RIE etching. The base layer was then RIE etched to isolate the devices. Next, aluminum ($^{27}Al^+$) was implanted to form the base contact regions as well as the floating guard rings. The implants were electrically activated with a 1,600°C, 5-minute anneal in Ar. A combination of thermal and deposited oxides (total thickness ~ 2 μm) was used as passivation. The alloyed Ni was used for both n-type and p-type ohmic contacts. A 2-μm-thick second level metal (Ti/Au) was then deposited and patterned.

Figures 6.9 and 6.14 show details of the chip design. Base fingers are connected, by the first level of metal, to the pad in the center of the chip by the cross-shaped bus and are further connected to another bus, which runs all around the chip. The emitter fingers are connected by the second-level metal all over the active area, excluding the center pad for the base.

Figure 6.15 shows the room temperature blocking characteristics of the device in common emitter mode. A BV_{CEO} of 1,400V was observed. The forward on-characteristics are shown in Figures 6.16 and 6.17. The device showed a maximum current gain (β_{max}) of 14 at room temperature, which reduced to about 8 at 225°C. The low current gain is attributed to a low minority carrier lifetime in the base/emitter space charge region [21]. Collector current of 17A was observed at $I_B = 2$A and $V_{CE} = 1$V. The maximum collector current reduces to 6A at $V_{CE} = 1$V at 225°C due to

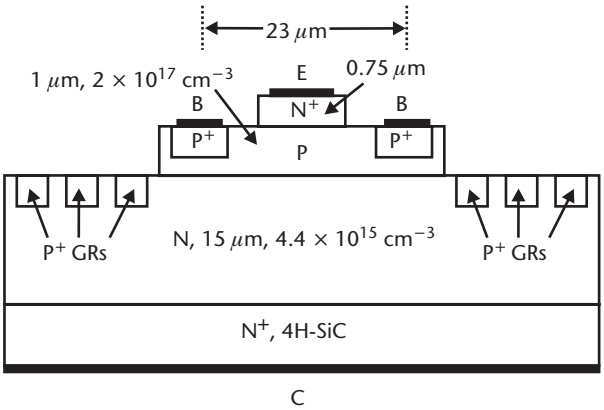


Figure 6.13 A simplified cross section of the SiC BJT.

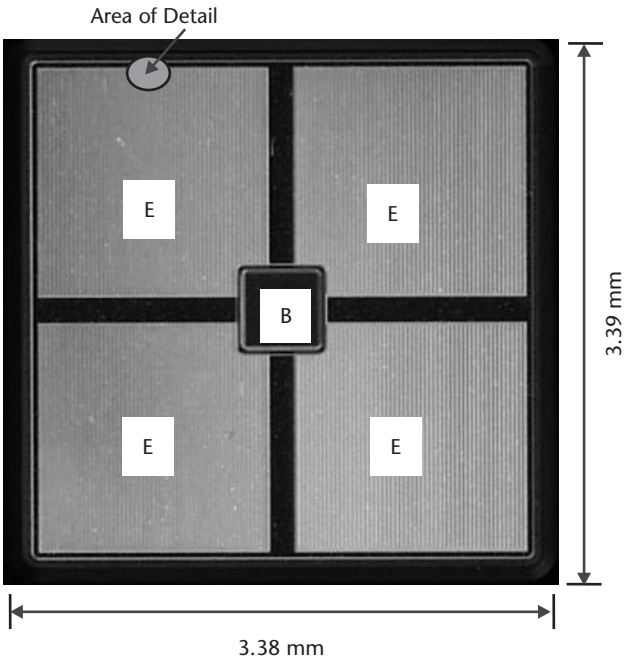


Figure 6.14 Picture of the 3.38 mm × 3.39 mm chip. Area of detail is shown in Figure 6.9.

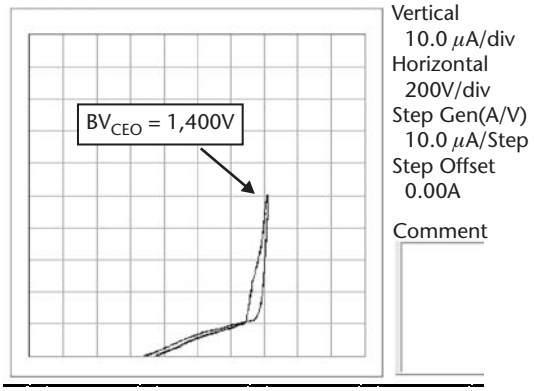


Figure 6.15 Room temperature reverse blocking characteristics (common emitter) of the 4H-SiC BJT with a footprint of 3.38 mm × 3.39 mm and an active area of 0.09 cm^2.

an increase in resistance of the collector region. In the saturation region, various curves can be seen to be overlapping, indicating lack of conductivity modulation of the collector layers. The specific on-resistance at RT is about 5.1 mΩ-cm^2, which essentially reflects the resistance of the unmodulated drift layer.

The input characteristics in Figure 6.18 show that a relatively small V_{BE} of 3.2V is required to drive a base current of about 5A. This is attributed to a relatively better specific contact resistance of the p$^+$ contact (~1×10^{-4} ohm-cm^2).

The common emitter current gain was characterized at elevated temperatures. Figure 6.19 shows the current gain (β) as a function of temperature ranging from RT to 500K. At elevated temperatures, the ionization of deep level acceptor atoms

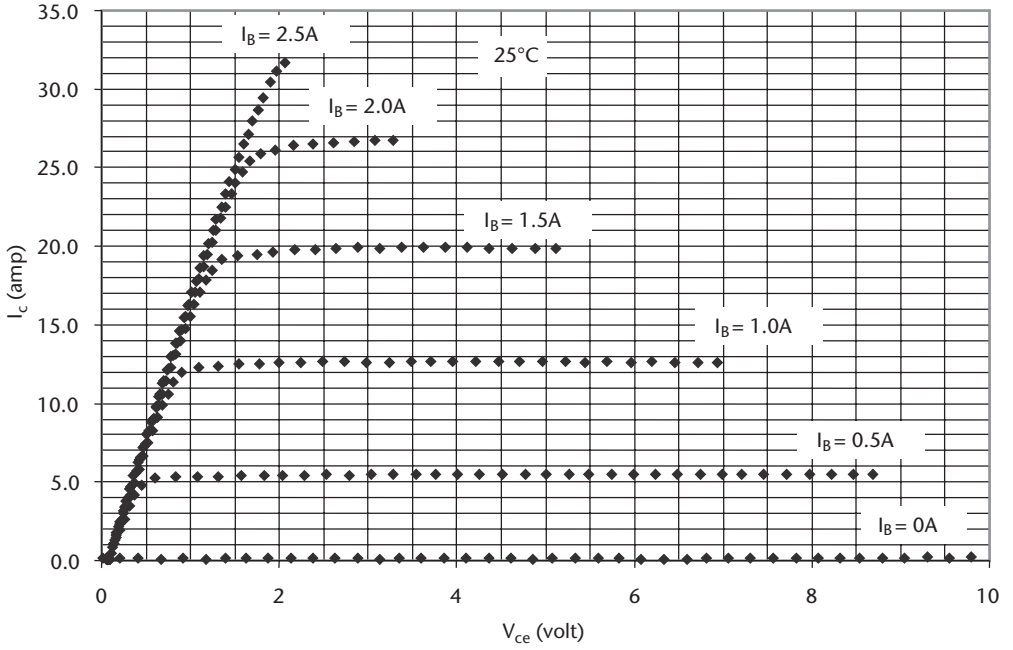


Figure 6.16 Room temperature forward dc characteristics in common emitter configuration of the 3.38 mm × 3.39 mm 4H-SiC BJT.

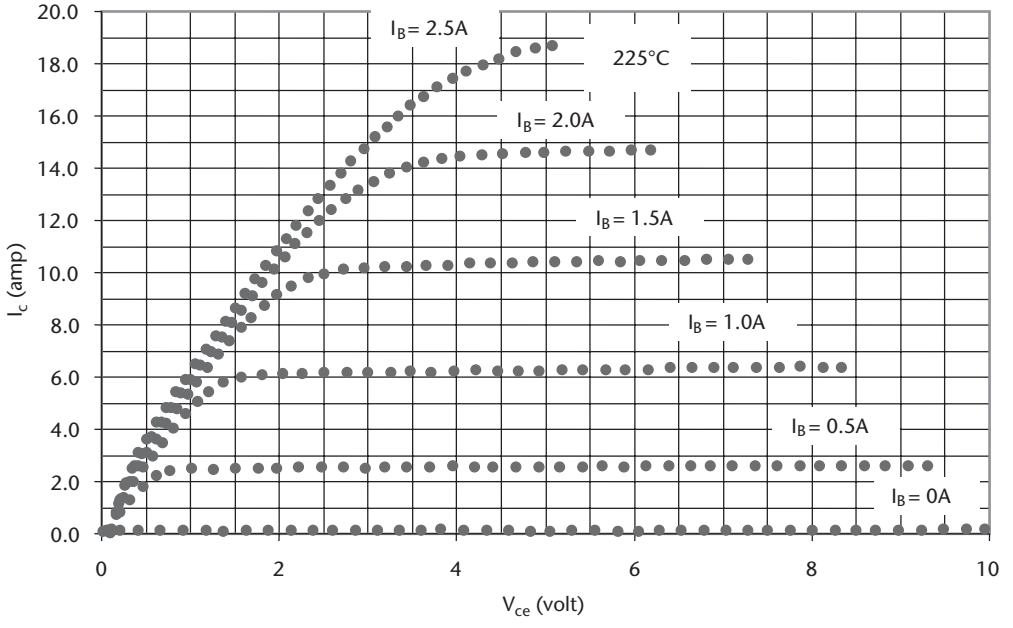


Figure 6.17 The dc characteristics in common emitter mode at 225°C. The on-resistance increased by three times and current gain reduced by two times.

increases, which results in a reduction in the emitter injection efficiency. For example, the acceptor (Aluminum in 4H-SiC) doping of 2×10^{17} cm^{-3} is only 10% ionized

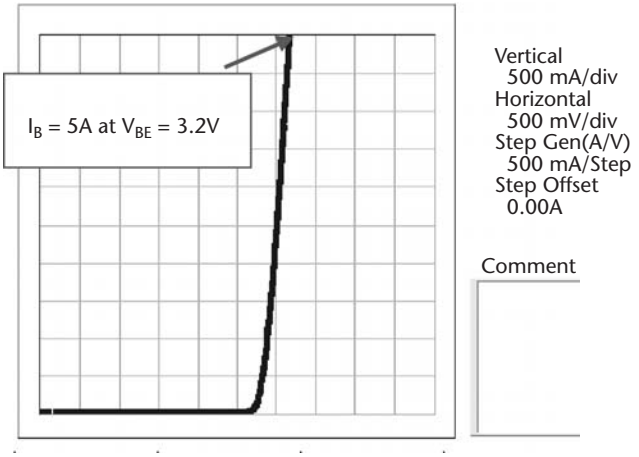


Figure 6.18 The room temperature input characteristics (V_{BE} versus I_B) of the 3.38 mm × 3.39 mm 4H-SiC BJT.

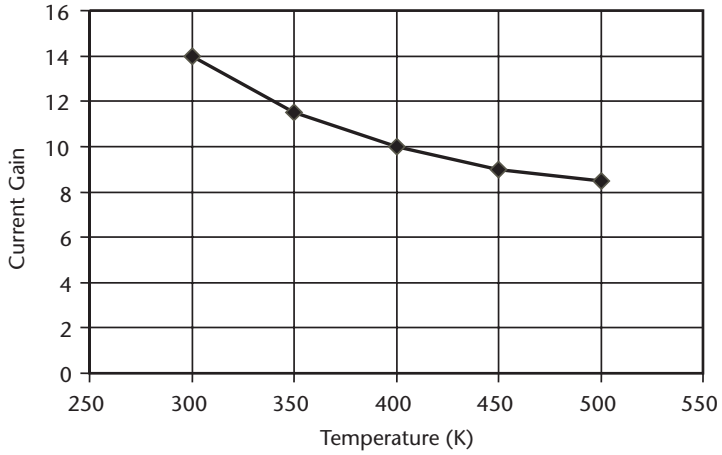


Figure 6.19 Current gain as a function of temperature.

at room temperature. The percent ionization increases to 55% at 500K. This effect cancels the effect of increased minority carrier lifetime and reduces the current gain with temperature. This feature, along with the positive temperature coefficient in the on-resistance (Figure 6.20), reduces the possibility of a thermal runaway and makes paralleling easy for these devices.

The turn-on and turnoff measurements were performed at room temperature using a power supply voltage of 300V and a load resistance of approximately 20Ω in common emitter mode. Typical turnoff and turn-on transients recorded at 25°C are shown in Figures 6.21 and 6.22. The device was turned off by simply removing the base current. A turn-on rise time of 160 ns and a turnoff fall time of 120 ns were observed at 25°C. In addition, a storage time of approximately 40 ns was observed.

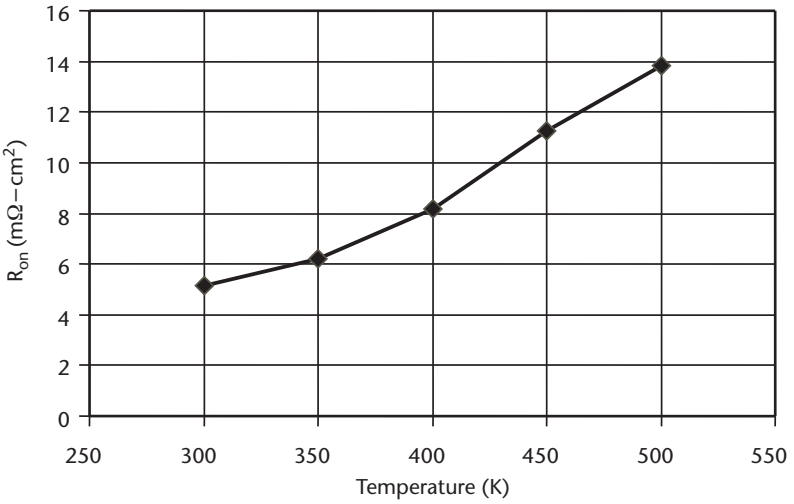


Figure 6.20 Specific on-resistance of the 3.38 mm × 3.39 mm 4H-SiC BJT normalized to the active area of 0.09 cm^2. The R_{on} increases from 5.15 mΩ-cm^2 at 25°C to 13.85 mΩ-cm^2 at 500K.

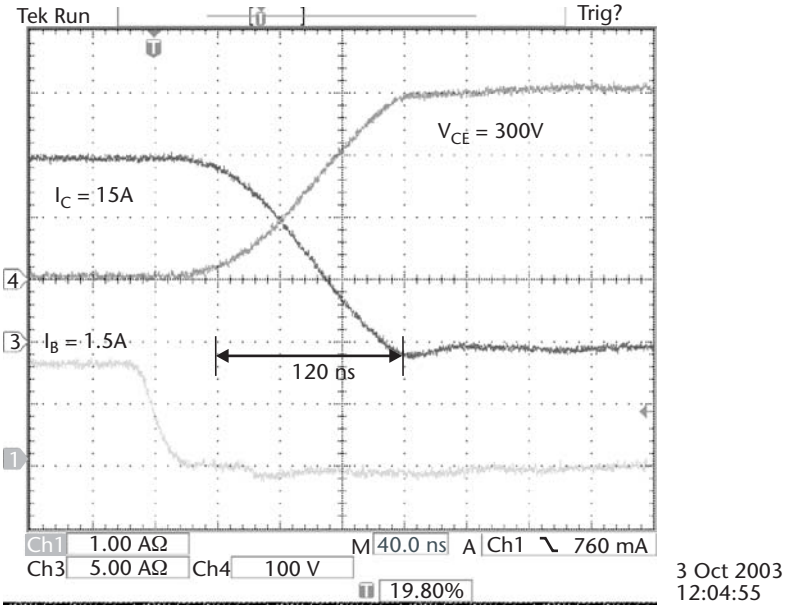


Figure 6.21 Turnoff measurements in common emitter mode with a load resistance of 20 ohms at 25°C.

6.6 Design and Fabrication of UHF Transistors

Power gain is one of the most important design considerations in the design of a microwave power transistor. The power gain is determined by the f_{max}, the maximum frequency of oscillation. Under small signal conditions, the highest power gain a transistor can achieve at frequency f_0 is given by

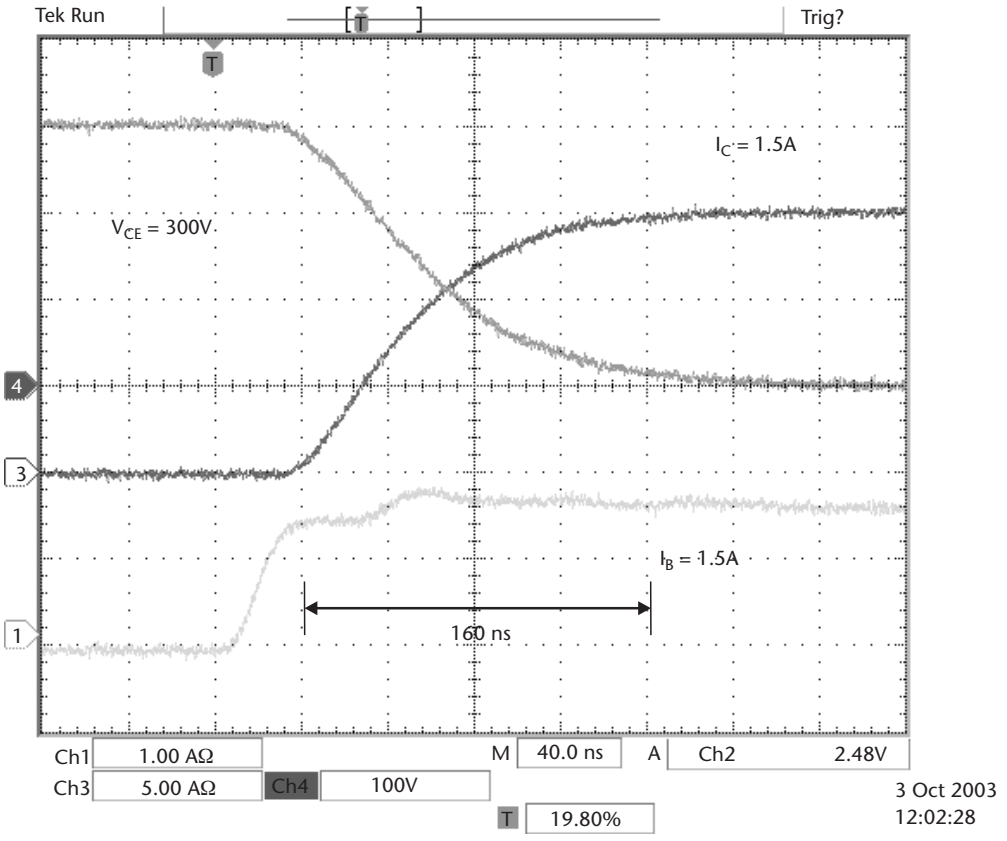


Figure 6.22 Turn-on measurements in common emitter mode with a load resistance of 20 ohms at 25°C.

$$powergain \approx \left(\frac{f_{\max}}{f_0}\right)^2$$

Normally, however, the power gain predicted by this equation cannot be obtained due to parasitics. For large-signal Class C operation, the power gain is further reduced by the current and voltage saturation of the transistor. Therefore it is not unusual for a power transistor to have gain, which is 3 to 4 dB lower than this relation predicts. Assuming that we need a small-signal gain of 12 dB at 400 MHz, this relation dictates an f_{max} of at least 1.6 GHz.

To design a transistor with a 1.6-GHz intrinsic f_{max}, we should examine the factors that affect the f_{max} of the transistor. A simplified cross section of the epitaxial emitter structure is shown in Figure 6.23. The stripe geometry has been assumed. All microwave transistors are fabricated more or less with this geometry. The intrinsic part, directly under the emitter, is the active part of the transistor. The extrinsic part, which connects the intrinsic base (under the emitter) to the base contacts, is the parasitic part of the transistor. The effects of these two parts on the transistor f_{max} can be evaluated by the following formula [22]:

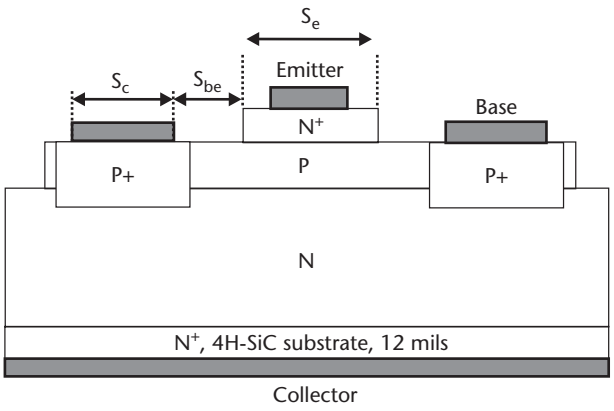


Figure 6.23 A simplified cross section of the RF BJT structure.

$$f_{\max} = \sqrt{\frac{f_T}{8\pi\left(r_{con}C_t + \frac{r_{be}C_{be}}{2} + r_b C_i\right)}}$$

where the various terms are defined:

f_T Current gain bandwidth of the transistor.
r_{con} Base contact resistance.
r_{be} Extrinsic base resistance.
r_b Intrinsic base resistance.
C_t Total base-collector capacitance.
C_{be} Collector base capacitance due to the extrinsic part of the base.
C_i Collector base capacitance due to the intrinsic part of the base.

For interdigitated transistor structures, the device parameters in the previous formula can be further expressed in terms of the transistor structure parameters [22]. Thus we have,

$$r_{con}C_t = \frac{1}{2}R_c C_{cb}\left(S_c + 2S_{be} + S_e\right)$$

$$r_{be}C_{be} = \frac{1}{2}R_{be}C_{cb}S_{be}^2$$

$$r_b C_i = \left(\frac{R_{be}S_{be}}{2} + \frac{R_b S_e}{12}\right)C_{cb}S_c$$

where

R_c Base contact resistance per unit length in ohm-cm.
R_b Intrinsic base sheet resistance in ohm/sq.
R_{be} Extrinsic base sheet resistance in ohm/sq.
C_{cb} Collector base capacitance in F/cm^2.

S_e Emitter width (shown in Figure 6.23).

S_c Base contact width (shown in Figure 6.23).

S_{be} Spacing between emitter mesa and the base contact (shown in Figure 6.23).

Assuming R_c ~ 1 ohm-cm, $R_b = R_{be}$ = 100,000 ohm per sq. (for $N_A = 2 \times 10^{18}$ cm^{-3}), f_T = 2 GHz, S_c = 2 μm, and W_c, depleted collector thickness of 2 μm ($C_{cb} = (\varepsilon_{SiC}/W_c)$, the f_{max} was calculated for various values of S_e and S_{be}. The results are summarized in Figure 6.24. Based on these calculations, it may be concluded that the f_{max} is limited by the extrinsic base resistance and not by the emitter width to the first order. Therefore, we have chosen the emitter width, S_e = 2.5 μm for ease of fabrication. The nominal design uses S_{be} = 0.5 μm to assure that we get f_{max} > 1.6 GHz.

The f_T may be estimated as follows:

$$\tau_{ec} = \frac{1}{2\pi f_T} = \frac{W_b^2}{2D_n} + \frac{W_C}{2v_s} + \frac{kT/q}{I_C}\left(C_{BE} + C_t\right)$$

where

τ_{ec} Total delay between emitter to collector.

W_b Base thickness (500–2,000Å).

D_n Diffusion coefficient of electrons in the base (1.95 cm^2/sec at 25°C assuming electron mobility of 75 $cm^2/V \cdot s$ in the base doped at 2×10^{18} cm^{-3}).

W_C Collector thickness (6 μm).

V_s Velocity of electrons in the collector (1.5×10^7 cm/sec at 25°C).

I_C Collector current (50% of the maximum value at a current density of 6,000 A/cm^2).

C_{BE} Total base-emitter junction capacitance.

C_t Total base-collector capacitance.

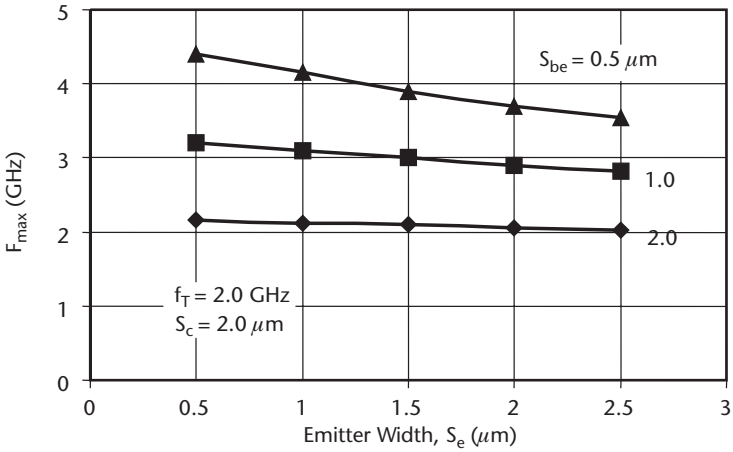


Figure 6.24 Calculation of f_{max} versus emitter stripe width, S_e, with a variable spacing between emitter mesa and the base contact, S_{be}.

The calculated values of f_T as a function of W_b at room temperature and 250°C junction temperature are shown in Figure 6.25. We have chosen a nominal value of W_b ~ 1,000Å to provide an f_T ~ 2 GHz at a junction temperature of 250°C. The collector thickness is chosen to be 6 μm to provide a reasonably high V_{CBO} of around 600V. It turns out that if a power supply voltage of 300V is chosen for Class B operation, the output power density in BJT cells is very high. With approximately 50% power-added efficiency, about the same amount of power is thermally dissipated. As a result, the junction temperature rises to above 400°C, which then reduces f_T and consequently f_{max} and power gain. Therefore, we have chosen a collector supply voltage of 80–100V to minimize the thermal issues. This then dictates a V_{CEO} of approximately 200V (assuming common emitter operation) and a V_{CBO} of approximately 250–300V. Thus, in future designs, the collector thickness may be reduced to 2.5 μm, resulting in further improvement in f_T. Although reduction in collector thickness will increase the base-collector capacitance, C_t, its overall effect will be to improve both f_T and f_{max}.

The epitaxial emitter structure was fabricated, as shown in Figure 6.26 [23]. In this case, only 1,000-Å-thick, p-type base layer doped at 2×10^{18} cm^{-3} is grown. This is followed by an epitaxial growth of 3,000-Å-thick n^+ emitter layer. The emitter layer is etched using RIE to stop at the base layer. The rest of the process details are similar to those described in Section 6.4. The most difficult step in this process is the etching of the emitter layer and stopping at the base layer. The uniformity of the RIE is critical at this step.

Figure 6.27 shows the layout of a typical cell with a pitch of 6 μm. The cell has an approximate height of 1 mm (166 emitter fingers) and an active area width of 75 μm. Counting both edges of the emitter finger, the total emitter periphery per cell is approximately 1 inch. In each cell, six base pads have been used to uniformly feed the base. The emitter pad lies on the active area. Five floating guard rings are used for edge termination. The base contact implants and the ohmic contacts have been connected to two busses on either side of the cell. After the ohmic metal, a thick passivation is applied and contact windows are opened on the base busses and the emitter fingers. Metal-2 is used to contact the base busses and the emitter fingers.

Figure 6.28 shows the I-V characteristics of a single epitaxial emitter cell. A maximum current gain of about 15 is obtained. This current gain is extremely sensitive to the base contact implant spacing from the edge of the emitter mesa (in the

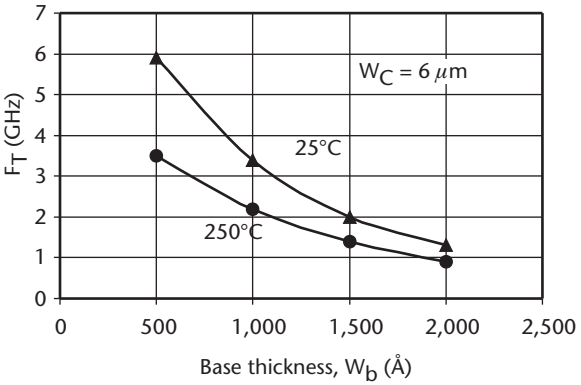


Figure 6.25 The calculated values of f_T versus base thickness.

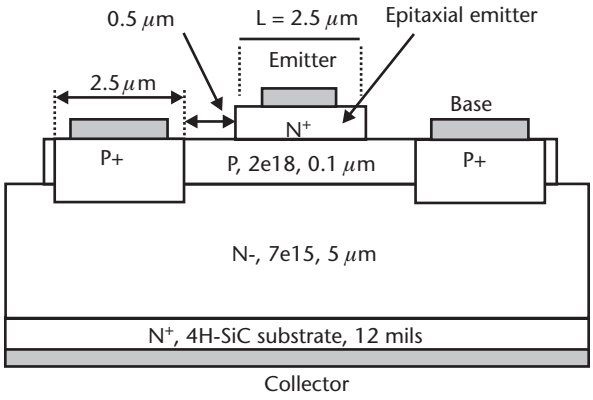


Figure 6.26 An idealized cross-section of the epitaxial emitter structure with a pitch of 6 μm.

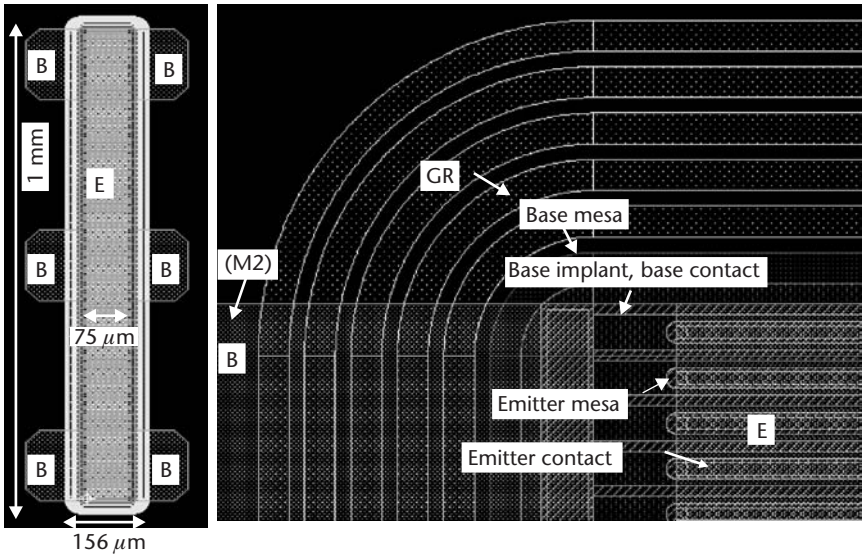


Figure 6.27 The internal details of the cell design.

present design, it is 0.5 μm, as shown in Figure 6.26). This indicates that the surface recombination is the limiting factor for current gain in the epitaxial emitter structure. Better passivation is needed to suppress the surface recombination and further improve the current gain. The common emitter breakdown voltage was in excess of 500V, consistent with the 5-μm collector thickness.

The f_T of the cell was measured as a function of the collector current with different collector supply voltages (Figure 6.29). For V_{CC} = 20V, f_T peaks at about 1.5 GHz, whereas for V_{CC} = 30V, f_T peaks at about 1.3 GHz. This reduction in f_T with collector voltage is expected as the electron transit delay in the collector depletion width increases with increasing collector bias. The sudden drop in f_T at high current for V_{CC} = 30V is attributed to a hot spot on the device.

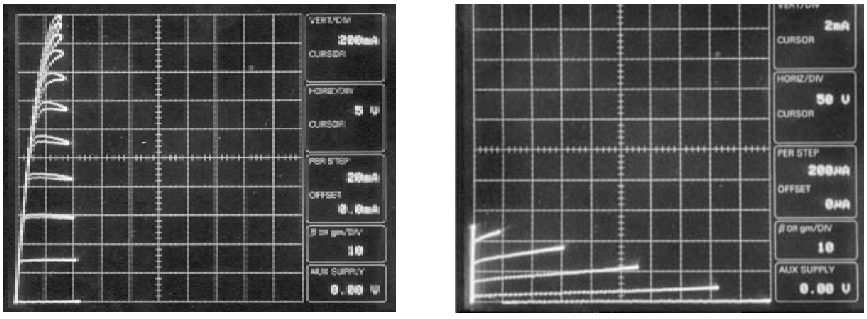


Figure 6.28 Common emitter (CE) I-V characteristics of a single epitaxial emitter cell showing (a) a maximum current of 2A, β_{max} ~ 15 and (b) a BV_{CEO} = 500V.

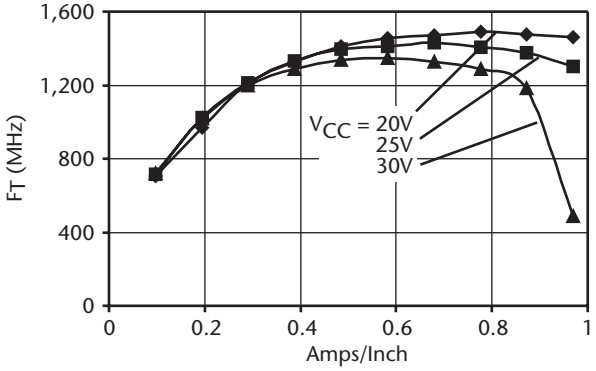


Figure 6.29 Measurement of f_T as a function of collector current and the collector voltage.

A single cell was measured in common base (CB), class C mode at 425 MHz using a collector supply voltage of 80V. The pulse width of 100 μs with a duty cycle of 10% was used. The single measurement yielded a maximum power of 39.8W with a power gain of 5.1 dB and a collector efficiency of 57.85% (Figure 6.30). The power gain in class C or class B is expected to be low due to a large input power required to turn on the input base-emitter junction, which has a turn-on voltage of about 3V due to the wide bandgap of SiC. The output power level is consistent with the power triangle measured under dc conditions [40W = (160V × 2A)/8].

A single cell was also measured in CE mode with a collector supply voltage of 80V at 425 MHz. The device was biased in class AB mode with a collector bias current of about 50 mA, just enough to overcome the 3-V turn-on voltage. A 100-μs pulse width with 10% duty cycle was used. The results are shown in Figure 6.31. A maximum output power of 50W for a single cell was achieved. This represents an output power density of 47 kW/cm^2 when normalized by the active base area. The power density is more than five times higher than that typically obtained with Si BJTs at this frequency. The peak large-signal power gain was 9.6 dB. The collector efficiency at the output power of 50W was 51% with a power gain of 9.3 dB. Next, three cells were connected in parallel to yield an output power of 150W with a collector efficiency of 60% and power gain of 6.5 dB (Figure 6.32). This clearly shows

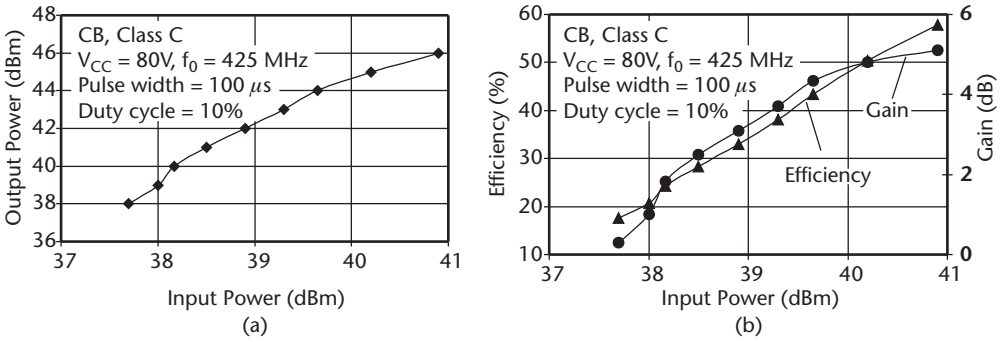


Figure 6.30 (a) Output power versus input power for a single cell in CB mode operated in class C mode at 425 MHz, pulse width 100 μs, duty cycle 10%, and V_{CC} = 80 V. (b) Collector efficiency and power gain versus output power for conditions stated in part (a).

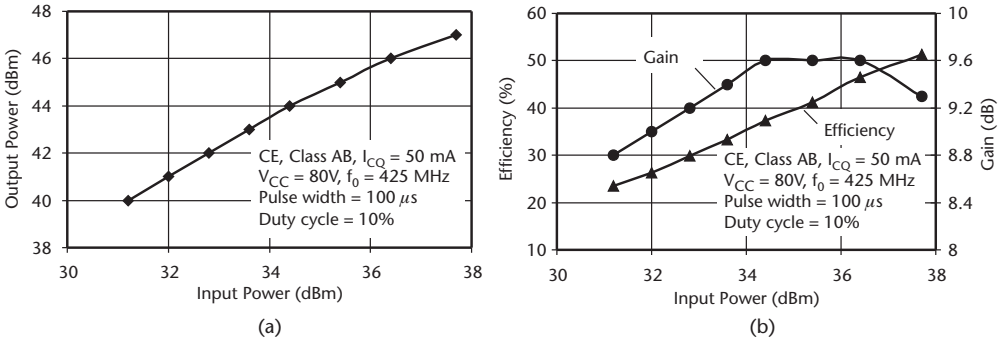


Figure 6.31 (a) Output power versus input power for a single cell in CE mode operated in class AB mode at 425 MHz, pulse width 100 μs, duty cycle 10%, V_{CC} = 80V and I_{CQ} = 50 mA. (b) Collector efficiency and power gain versus output power for conditions stated in part (a).

that the output power is scalable with additional cells. The details of the input and output matching determine the power gain and collector efficiency, which could be different in single-cell and three-cell configurations.

These results are highly encouraging as they demonstrate the high power capability of the SiC RF-BJT devices along with acceptable power gain and efficiency. From thermal simulations, it is estimated that the junction temperature may reach a peak value of 171°C for pulse widths of 250 μs and 6% duty cycle without any external cooling. Since SiC junctions can easily sustain a temperature of 250°C, there is room to increase the pulse width even further.

6.7 Future Work

From the previous discussion, it is gathered that there are two potential issues that need to be addressed in any future research on SiC BJTs: (1) The current gain of the devices is low (10–15) at present; and (2) the base resistance is rather high due to the high sheet resistance of the base layer and the necessity of keeping the base contact implant at least 5 micron away from the edge of the emitter mesa. The current gain

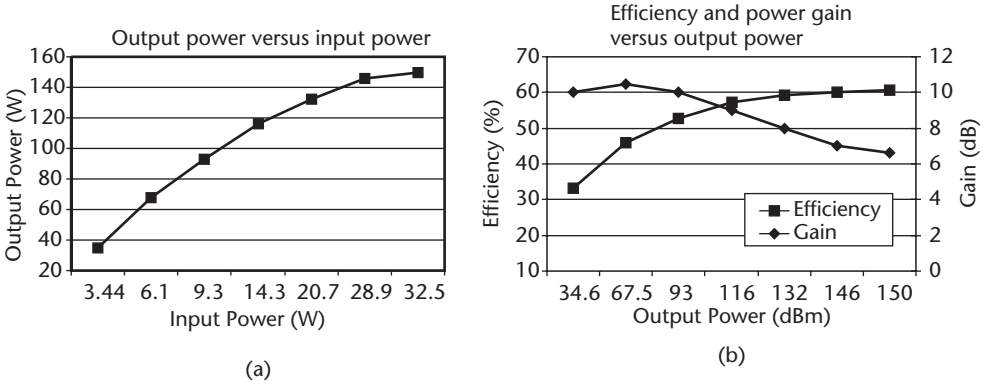


Figure 6.32 Three cells in CE, class AB mode at 425 MHz, pulse width 100 μs, duty cycle 10%, V_{CC} = 80V, and I_{CQ} = 100 mA.

is presently dominated by the recombination in the base/emitter space charge region. This can be addressed by further optimizing the growth of these layers. The base contact can be further improved by optimizing the p^+ implant schedule and annealing conditions. There is considerable ongoing research in these areas and it is expected that useful SiC BJTs will be commercially available in a few years.

References

[1] Von Muench, W., P. Hoeck, and E. Pettenpaul, "Silicon Carbide Field-Effect and Bipolar Transistors," *Technical Digest of 1977 Intl. Electron Devices Meeting*, pp. 337–339.

[2] Palmour, J. W., et al., "6H-Slicon Carbide Power Devices for Aerospace Applications," *Proc. of the 28th Intersociety Energy Conversion Engineering Conference, American Chem. Soc.*, Vol. 1, 1993, pp. 249–254.

[3] Ryu, S., et al., "1800V, 3.8A Bipolar Junction Transistors in 4H-SiC," *Technical Digest of 58th Device Research Conference*, Denver, CO, June 19–21, 2000, pp. 133–134.

[4] Luo, Y., L. Fursin, and J.H. Zhao, "Demonstration of 4H-SiC Power Bipolar Junction Transistors," *Electronics Letters,* Vol. 36, No. 17, August 17, 2000, pp. 1496–1497.

[5] Huang C-F, and J.A. Cooper, Jr., "4H-SiC npn Bipolar Junction Transistors with BV_{CEO} > 3,200V," *Proc. of the 14th Intl. Symposium on Power Semiconductor Devices and ICs*, Santa Fe, NM, June 4–7, 2002, pp. 57–60.

[6] Ryu, S. -H., et al., "1800V NPN Bipolar Junction Transistors in 4H-SiC," *IEEE Electron Device Letters*, Vol. 22, No. 3, March 2001, pp. 124–126.

[7] Sze, S. M., *Physics of Semiconductor Devices*, New York: Wiley, 1981, pp. 133–189.

[8] Ivanov, P.A., et al., "Factors Limiting the Current Gain in High-Voltage 4H-SiC npn-BJTs," *Solid-State Electronics*, Vol. 46, No. 4, April 2002, pp. 567–572.

[9] Li, H-F, et al., "Effect of NO Annealing Conditions on Electrical Characteristics of n-Type 4H-SiC MOS Capacitors," *J. of Electronic Materials*, Vol. 29, No. 8, August 2000, pp. 1027–1032.

[10] Lipkin, L. A., M. K. Das, and J. W. Palmour, "N_2O Processing Improves the 4H-SiC:SiO2 Interface," *Mat. Sci. Forum*, Vols. 389–393, 2002, pp. 985–988.

[11] Huang, C. -F, and J. A. Cooper, Jr., "4H-SiC Power Bipolar Transistors with Common Emitter Current Gain > 50," *Technical Digest of the Device Research Conference 2002*, Santa Barbara, CA, June 2002, pp. 183–184.

[12] Zhang, J., et al., "A High Current Gain 4H-SiC NPN Power Bipolar Junction Transistor," *IEEE Electron Device Letters*, Vol. 24, No. 5, May 2003, pp. 327–329.

[13] Tang, Y., J. B. Fedison, and T. P. Chow, "An Implanted-Emitter 4H-SiC Bipolar Transistor with High Current Gain," *Technical Digest of 58th Device Research Conference*, Denver, CO, June 19–21, 2000, pp. 131–132.

[14] Tang, Y., J. B. Fedison, and T. P. Chow, "High-Voltage Implanted-Emitter 4H-SiC BJTs," *IEEE Electron Device Letters*, Vol. 23, No. 1, January 2002, pp. 16–18.

[15] Ryu, S. -H., et al., "1.8 kV, 3.8A Bipolar Junction Transistors in 4H-SiC," *Proc. of the 13th Intl. Symposium on Power Semiconductor Devices and ICs. ISPSD '01*, Osaka, Japan, June 4–7, 2001, pp. 37–40.

[16] Agarwal, A. K., et al., "Large Area, 1.3 kV, 17A, Bipolar Junction Transistors in 4H-SiC," *Proc. of the 15th Intl. Symposium on Power Semiconductor Devices and ICs. ISPSD '03*, Cambridge, England, April 14–17, 2003, pp. 105–108.

[17] Schaffer, W. J., et al., "Conductivity Anistropy in Epitaxial 6H and 4H-SiC," *Mat. Res. Soc. Symp. Proc.*, Materials Research Society, Vol. 339, 1994, pp. 595–600.

[18] Capano, M. A., et al., "Surface Roughening in Ion Implanted 4H-Silicon Carbide," *J. of Electronic Materials*, Vol. 28, No. 3, March 1999, pp. 214–218.

[19] Sankin, I., et al., "On Development of 6H-SiC LDMOS Transistors Using Silane-Ambient Implant Anneal," *Solid-State Electronics*, Vol. 45, No. 9, September 2001, pp. 1653–165.

[20] Agarwal, A. K., et al., "SiC BJT Technology for Power Switching and RF Applications," *ICSCRM 2003*, Lyon, France, October 6–10, 2003.

[21] Ivanov, P. A., et al., "Base Current Gain of Power (1800V, 10A) 4H-SiC npn-BJTs," *ICSCRM 2003*, Lyon, France, October 6–10, 2003.

[22] Yuan, H. -T., et al., "A 2-Watt X-Band Silicon Power Transistor," *IEEE Trans. on Electron Devices*, ED-25, 1978, pp. 731–736.

[23] Agarwal, A. K., et al., "Power Amplification in UHF Band Using SiC RF Power BJTs," *Proc. of the 4th European Conference on Silicon Carbide and Related Materials*, Linköping, Sweden, September 2–5, 2002, *Mat. Sci. Forum*, Vols. 433–436, 2003, pp. 785–788.

About the Editors

Stephen E. Saddow received his Ph.D. in electrical engineering from the University of Maryland in College Park, Maryland, in 1993. In 2001, he joined the faculty at the University of South Florida, Tampa, Florida, as an associate professor of electrical engineering. There he formed the USF SiC Group, which is focused on SiC materials and device research. From 1988 until 1996, Dr. Saddow was a senior electronics engineer with the Army Research Laboratory in Adelphi, Maryland. From 1997 until 2001, he was an assistant professor of electrical and computer engineering and the director of the Emerging Materials Research Laboratory at Mississippi State University. Dr. Saddow's research has focused primarily on SiC epitaxial growth via chemical vapor deposition, and he has pioneered the use of porous SiC materials for novel applications. These applications include improved epitaxial materials, gas sensors, and fuel cells. He has more than 75 publications on SiC and holds six U.S. patents based on his research. Dr. Saddow has held visiting positions at several laboratories around the world, most notably the Institute of Applied Physics at the University of Erlangen-Nürnberg, The Royal Institute of Technology (KTH) in Kista, Sweden, the Institut d'Electronique Fondamentale at the University of Paris Sud in Orsay, France, and, more recently, the Max Planck Institute of Solid State Physics in Stuttgart, Germany. He is a senior member of the IEEE and a member of Sigma Xi, the scientific research society, and Eta Kappa Nu, the electrical engineering honor society.

Anant Agarwal received his Ph.D. in electrical engineering from Lehigh University in Bethlehem, Pennsylvania, in 1984. In 1984, he joined AT&T Bell Laboratories in Murray Hill, New Jersey, where he worked on the GaAs digital circuits for optical communications. From 1985 to 1990, he was an assistant professor of Electrical Engineering at the M.N.R. Engineering College in Allahabad, India. In 1990, Dr. Agarwal joined the Northrop Grumman Science & Technology Center (STC, formerly Westinghouse STC) in Pittsburgh, Pennsylvania, where he performed extensive research on SiGe HBTs and SiC high-power devices. Along with his colleagues, he pioneered the development of SiC static induction transistor for power amplification at UHF and S-band. In 1998, Dr. Agarwal was promoted to the position of fellow engineer. He joined Cree, Inc., in 1999 as a senior scientist, where he led a team of engineers and technologists who successfully developed and commercialized 600-V and 1,200-V SiC Schottky diodes. Dr. Agarwal has also been engaged in the development of SiC UMOSFETs, GTOs, PiN rectifiers, power BJTs, and DMOSFETs. Currently, his research activities include basic SiC device technology and

systems applications. Dr. Agarwal is a member of IEEE. He has coauthored more than 75 technical papers and conference presentations and holds eight U.S. patents.

Index

Related Titles from Artech House

Electrical and Thermal Characterization of MESFETs, HEMTs, and HBTs, Robert Anholt

High-Level Test Synthesis of Digital VLSI Circuits, Mike Tien-Chien Lee

Principles and Analysis of AIGaAs/GaAs Heterojunction Bipolar Transistors, Juin J. Liou

Reliability and Degradation of III–V Optical Devices, Osamu Ueda

System-on-a-Chip: Design and Test, Rochit Rajsuman

For further information on these and other Artech House titles, including previously considered out-of-print books now available through our In-Print-Forever® (IPF®) program, contact:

Artech House
685 Canton Street
Norwood, MA 02062
Phone: 781-769-9750
Fax: 781-769-6334
e-mail: artech@artechhouse.com

Artech House
46 Gillingham Street
London SW1V 1AH UK
Phone: +44 (0)20 7596-8750
Fax: +44 (0)20 7630-0166
e-mail: artech-uk@artechhouse.com

Find us on the World Wide Web at:
www.artechhouse.com