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Foreword by Lawrence E. Larson

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FOREWORD

Well over a billion people are currently using cellular telephones, and this number is expected to grow to over two billion in the next few years. It is remarkable that a device that was considered a high-technology "toy" just a few years ago is now an indispensable feature of modern life. One of the key reasons for this remarkable transformation is the integration of all the radio functions of a cellular telephone onto a single inexpensive piece of silicon. This achievement is a result of innovations in design and process technology that allowed formerly discrete and separate devices to be integrated onto a common substrate.

Now that this integration has been accomplished, the next challenge is to make these radio functions adaptive to their environment. For example, a cellular telephone of the future will be able to "sense" its environment, and configure its radio functions to optimize the performance - and minimize the battery drain - for that environment; when the cellular telephone is close to a base station and is in a low interference environment it will reduce its power consumption for the relaxed performance requirements. Conversely, when it is far from the base station and in a high interference environment, the radio will be adjusted accordingly.

This "adaptive" feature of wireless communications devices is just today becoming a reality, and this book represents one of the first comprehensive treatments of the subject. Adaptive radio transceivers require a comprehensive theoretical framework in order to optimize their performance. The authors provide this framework with their discussion of joint optimization of Noise Figure and Input Intercept Point in receiver systems. They then provide original techniques to optimize voltage controlled oscillators and low-noise amplifiers to minimize their power consumption while maintaining adequate system performance. The experimental results that they present at the end of the book confirm that utility of their techniques.

I expect that this book will be an invaluable reference in the future, as adaptive multistandard radio frequency transceivers become a reality.

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May, 2006.

OUTLINE

Some background on wireless and RF circuits and systems is given in Chapter 1. Application of adaptivity to low-power and multistandard wireless RF circuits is then discussed.

After the introductory chapter, basic definitions of receiver performance parameters are reviewed in Chapter 2, viz., gain, linearity and noise parameters.

Chapter 3 discusses spectrum and signal transformation in various downconverter topologies. Mixer-oscillator models are then classified. Using the spectrum-signal presentation and the mixer-oscillator models, an all-encompassing analysis of a number of receiver architectures and related phenomena is performed.

A procedure to select noise and linearity specifications for receiver circuits is described in Chapter 4. An outline is given for the assigning of the noise and linearity performance parameters to receiver circuits. In addition, we derive conditions for the optimal dynamic range of a receiver, and for the equal noise and linearity improvements with respect to the performance requirements. Finally, some design trade-offs between performance parameters in a single receiver circuit are described by means of a K-rail diagram.

Chapter 5 introduces amplifier adaptivity models (i.e., adaptivity figures of merit). They give insight into how low-noise amplifiers can trade performance, such as noise figure, gain, and linearity, for power consumption. The performance trade-offs in adaptive low-noise amplifiers are discussed using amplifier K-rail diagrams.

The application of adaptivity concepts to voltage-controlled oscillators is discussed in Chapter 6. The concepts of phase-noise tuning and frequency-transconductance tuning are first introduced. An adaptive phase-noise oscillator model is then derived. The adaptivity figures of merit are defined, viz., the phase-noise tuning range and frequency-transconductance sensitivity. Comprehensive performance characterization of oscillators by means of K-rail diagrams concludes this section. Numerous relationships and trade-offs between oscillator

performance parameters, such as voltage swing, tank conductance, power consumption, phase noise, and loop gain, are qualitatively and quantitatively described. Furthermore, the oscillator adaptivity figures of merit are captured using K-rail diagrams.

Adaptivity design proofs-of-concept are reviewed in Chapter 7. An 800MHz voltage-controlled oscillator design is presented with a phase-noise tuning range of 7dB and a factor of around three saving in power consumption. In addition, we discuss an adaptive multistandard/multi-mode voltage-controlled oscillator and a multi-mode quadrature downconverter in the context of the second- and third-generation standards, i.e., DCS1800, WCDMA, WLAN, Bluetooth and DECT. By trading RF performance for current consumption, the adaptive oscillator and the adaptive image-reject downconverter offer factors of 12 and 2 saving in power consumption, respectively, between the demanding mode (e.g., DCS1800) and the relaxed mode (e.g., DECT) of operation.

LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
AFOM	Adaptivity Figure of Merit
BB	Baseband
CAD	Computer-Aided Design
CGM	Frequency-Transconductance Tuning
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processor Unit
D (subscript)	Desired
DC-MO	Double-Complex Mixer-Oscillator
DCS1800	Digital Cellular Communications
DECT	Digital Enhanced Cordless Telecommunications
DR	Dynamic Range
DR-MO	Double-Real Mixer-Oscillator
DSB	Double-Side Band
E (subscript)	Equilibrium
EQ (subscript)	Equivalent
F	Noise Factor
FDD	Frequency-Division Duplex
G (g)	Gain
GMSK	Gaussian Minimum-Shift Keying
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
IC	Integrated Circuit
ID	Inductive Degeneration
IDR	Inverse Dynamic Range
IF	Intermediate Frequency
IM2	Second-Order Intermodulation
IM3	Third-Order Intermodulation
IIP3TR	Input-Referred Third-Order Intercept Point Tuning Range
IITR	Imaginary-Impedance Tuning Range
IP2	Second-Order Intercept Point
IP3	Third-Order Intercept Point
IRR	Image-Rejection Ratio
LC	Inductance-Capacitance

LNA	Low-Noise Amplifier
LO	Local Oscillator
MB	Multi-Band
MMS	Multimedia Message Service
MO	Mixer-Oscillator
MP3	Moving Pictures Experts Group Audio Layer 3
MS	Multistandard
MSK	Minimum Shift Keying
MSM	Multistandard Module
NF	Noise Figure
NFTR	Noise-Figure Tuning Range
NT	Non-Tapped
OBT (subscript)	Obtained
OPT (subscript)	Optimum
OPT-MIN	Optimum-Minimum
PCB	Printed-Circuit Board
PN	Phase Noise
PND	Phase-Noise Difference
PN-D	Phase-Noise Demanding
PN-M	Phase-Noise Moderate
PNR	Phase-Noise Ratio
PN-R	Phase-Noise Relaxed
PNTR	Phase-Noise Tuning Range
QPSK	Quadrature-Phase Shift Keying
QT	Quasi-Tapped
RF	Radio Frequency
RD	Resistive Degeneration
RID	Resonant-Inductive Degeneration
RITR	Real-Impedance Tuning Range
RSTR	Source-Impedance Tuning Range
SFDR	Spurious-Free Dynamic Range
SIGE	Silicon-Germanium
SMS	Short Messaging System
SNR	Signal to Noise Ratio
SS	Spectrum Signal
SSB	Single-Side Band
S-UP (subscript)	Start-Up
S_S-UP (subscript)	Safety Start-Up
TCN	Tail-Current Noise
TCS	Tail-Current Source
TFD	Transformed-Feedback Degeneration

TDD	Time-Division Duplex
VCO	Voltage-Controlled Oscillator
VG	Voltage Gain
VGTR	Voltage-Gain Tuning Range
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
16QAM	16 Symbol Quadrature Amplitude Modulation
2G	Second-Generation
3G	Third-Generation

Chapter 1

INTRODUCTION

One emerging worldwide vision of communication is that *wireless communications* and *ambient intelligence* will be highly advantageous in satisfying our yearning for information at any time and anywhere. Electronics that is sensitive to people's needs, personalized to their requirements, anticipatory of their behavior and responsive to their presence is one visionary conception of ambient intelligence [1]. Ambient intelligence technologies are expected to combine concepts of ubiquitous computing and intelligent systems. Technological breakthroughs will allow people to integrate electronics into more friendly environments: roll-up displays [2], intelligent mobiles [3], internet-enabled furniture [4]. People will relate to electronics in a more natural and comfortable way than they do now.

1.1 Why Silicon?

The Greek messenger Phidippides set off for 42km with news of his nation's victory over the invading Persian army at the battle of Marathon in 490 BC, uttering the words "be joyful, we win" on arrival, before promptly dropping dead of exhaustion [5]. Since then, it took humanity some 2400 years to find a harmless way to send a spoken message over a distance.

The technique of using radio waves to send information, exercised by Heinrich Hertz in 1888, and later by Nikola Tesla [6], was demonstrated in 1895 by Guglielmo Marconi [7], who successfully established the first transatlantic radio contact. This event is often referred to as the beginning of wireless communications [8].

At the beginning of the 20th century, Lee De Forest developed a triode vacuum tube that allowed for the amplification of an applied signal [9]. Around his amplifier vacuum tube, he developed the first radio- and audio-frequency amplifiers [8]. In the 1930s, scientists at Bell Labs, seeking

improved RF demodulation, resorted to the antiquated crystal detector, paving the way to a reliable semiconductor material, *silicon*.

The unreliability, heat dissipation problems and relatively large power consumption of vacuum tubes initiated a search for new means of amplification. In 1947, Walter Brattain and John Bardeen observed that a germanium crystal in touch with wires 0.002 inches apart could amplify an applied signal [10,11]. The point-contact transistor was born. Somewhat later, the junction (sandwich) transistor and field-effect transistor were implemented by William Shockley [12,13]. This trio was awarded the Nobel Prize for the invention of the transistor in 1956. The first commercial use of the transistor was in telephone equipment in the early 1950s [8].

The first transistorized radio appeared in 1954, and was the fastest selling retail object of that time. Using discrete components in those days, transistor circuits occupied a number of printed circuit boards the size of postcards. The idea of integrating a complete circuit on a single slice of silicon was implemented independently by Jack Kilby [14] and Robert Noyce [15] in 1958.

Thanks to techniques such as photolithography and computer-aided design, millions of transistors and other electronic components can nowadays be compactly integrated onto a silicon die smaller in size than a cornflake. Integrated circuits (IC) have paved the way to low-cost mass production of electronic equipment. A continuous reduction of the minimum feature sizes, i.e., scaling of microelectronic devices, reduces the cost per function by 25% per year and promotes IC market growth with 17% per year. Doubling of the number of components per chip every 18 months (Moore's Law) [16] has led to improved productivity and improved quality of human life through the proliferation of consumer and industrial electronics.

1.2 Why Wireless and RF?

Progress in silicon IC technology and innovations in IC design have enabled mobility of wireless consumer products and services.

Having started out with limited performance capabilities beyond simple telephony, mobile communications technologies are now entering all aspects of our lives. Mobile equipment today is shaped by user and *application* demands on the one hand and enabling semiconductor process *technologies* as well as radio frequency microelectronics on the other. Main drivers for mobile wireless devices are related to:

- *cost*, which depends on volume of production, size of mobile units, power consumption, and performance.

- *power consumption*, which depends on available frequency spectrum, functionality, and performance.

- *performance*, which depends on applications, standards and protocols.

The factors that make an integrated piece of silicon a desirable item are: mobility, high performance (voice, text and video transfer), low cost (advances in IC processing technology) and long lifetime (low power consumption).

An example of the enormous expansion of the wireless market is shown in Fig. 1.1. The total number of global mobile users amounts to 2 billion (third quarter 2005), whereas the number of GSM (Global System for Mobile communications) users is estimated at 1.5 billion [17].

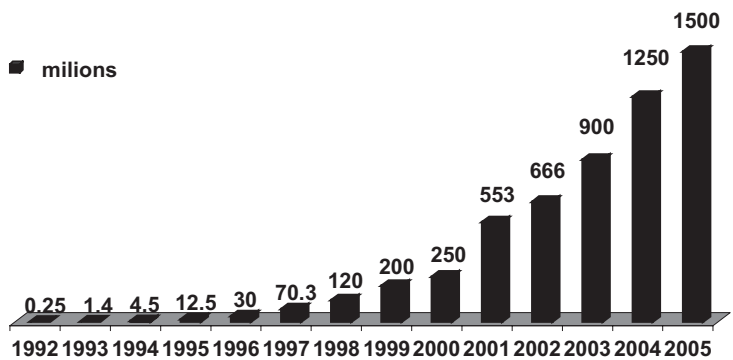

Figure 1.1: GSM growth for the period 1992-2005.

GSM sales are projected to grow at a Compound Annual Growth Rate of 11% through 2009, as color-, MMS- (Multimedia Messages Service), camera- and Java-enabled devices become widely available, and the cost of wireless services declines [18].

Despite the expansive sales growth of wireless devices, the use of wireless services generates even greater profit for telecom companies. Furthermore,

even larger growth requires many new services provided by mobile equipment (e.g., MMS, web access, and e-mail).

By introducing third-generation (3G) systems [19], more spectrum for voice services has become available, whilst enabling a wider variety of data and multimedia services. 98% of handsets sold worldwide in 2009 will be 3G devices, with the remainder being primarily GSM handsets sold into emerging markets and very cost sensitive segments of the mature markets [17].

Aside from the mobile phone market [16,19], there are many other wireless applications. Wireless connections to wired computer networks have become feasible. Wireless systems allow for cost-effective installation and deployment of electronics equipment by obviating the need for wires and cables. Wireless RF systems will undoubtedly spawn telemedicine, that is, remote, wireless medical monitoring. An intelligent transportation system that allows for communication and traffic control on the highway is yet another example of a mass market for wireless technology in the future.

However, to support all these applications, more sophisticated RF devices are required.

1.3 Why Low-Power and Adaptive RF?

The communication devices of the near future will not only have to support applications ranging from text, telephony, audio, and graphics to video, but they will also have to maintain connections with many other devices in a variety of environments (and not only with a single base station). Moreover, they should be position aware, and perhaps wearable rather than just portable.

Both the lifetime and size of mobile equipment critically depends on the battery. Low-power circuits (e.g., an order of mW for analog RF front-end circuits [20]) prolong battery lifetime while meeting the performance requirements [20,21]. However, for wearable devices that require the use of the highest-volume and highest-weight density batteries [22], even a low-power design strategy can offer only limited savings.

A combination of multiple functional requirements and the limited energy supply from a single battery is an argument for the design of both adaptive low-power (i.e., power-aware) hardware and software. Simply stated, as consumer demands outstrip the cost benefits achieved by Moore's Law and low-power circuit design, a new design direction is found in *adaptivity*. This eventually leads to smaller physical size, longer standby and active times, and enhanced functionality of mobile wearable devices.

The quality of service of mobile devices changes with the position and speed of mobile users. It also depends on the application, the number of users in a cell as well as their activity. A mobile device must handle the variable context efficiently due to scarce resources, especially limited battery power.

A power-aware (i.e., adaptive) RF design approach poses unique challenges: from hardware design to application software, throughout all layers of the underlying communication protocol (i.e., the processing technology, device level, circuit level, system level, as well as protocol, software, and application levels).

A block diagram of the receive part of an adaptive mobile device is shown in Fig. 1.2. This receiver consists of adaptive analogue RF front-end circuitry, adaptive analogue baseband circuitry (analogue processing of the received signal), and an adaptive digital back-end consisting of a dedicated central processing unit and a memory.

Whereas the transceiver circuits determine instantaneous power consumption, the average consumption depends on the power management of the complete system [23]. This implies that not only local, but also global (in all layers and at all time) power optimization and awareness are important for extending "lifetime" of mobile devices (i.e., time between battery recharges).

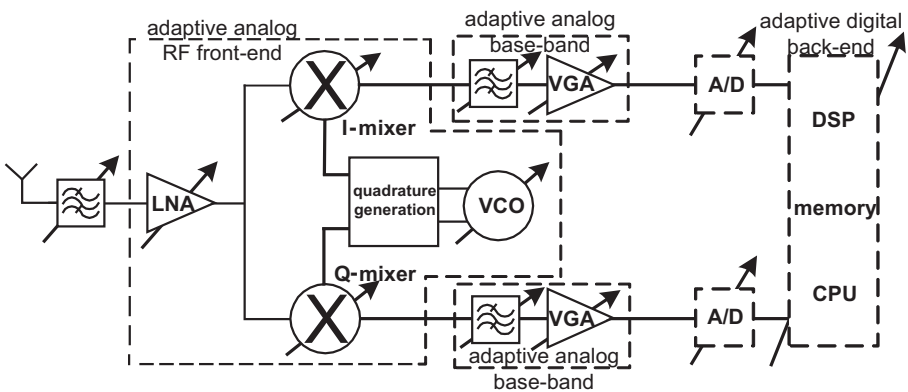

Figure 1.2: Block diagram of an adaptive receiver.

RF and power management have become the fastest growing segments in wireless IC revenue, due to the integration and increasingly complex power requirements, which are driven by advancing functionality (e.g., video, text) and transmission speeds in wireless devices. The RF portion is estimated at 19% of the wireless IC market [24].

Setting the performance parameters of an RF front-end by means of adaptive circuitry [25] is a way to manage power consumption in the RF path of a receiver. An adaptive low-noise amplifier, an adaptive mixer, and an adaptive oscillator (see Fig. 1.2) allow efficient use of scarce battery resources, thereby extending the lifetime of a mobile device. Furthermore, adaptive analogue baseband and digital back-end circuits enable complete hardware adaptivity. Analogue and digital baseband signal processing functions could be used to monitor quality of service (e.g., error rate of the detected bit sequences) and adjust the receiver parameters (e.g., tune a single bias current or multiple currents) in real time to meet the performance requirements. The theory and design of adaptive RF front-end circuits and adaptive RF front-ends for wireless communications are elaborated in detail in this book.

RF front-end robustness can be further improved by control of symbol rates, antenna beam patterns, transmitter power levels, and by control of circuit noise and linearity levels. For example, adaptive modulation and adaptive coding strategies [26], where the system can choose an optimal modulation and coding technique based on the temporal circumstances, can ameliorate the effects of multi-path fading, shadow fading, and path loss.

Graphical interaction with our direct environment combined with mobility is another intriguing concept in which low-power RF circuit design plays an important role [27]. If a lightweight video camera is attached to a mobile display for position tracking and recording of video, the hardware complexity must be reduced in order to keep the power consumption low. Since the RF front-end cannot operate with scarce resources, the power consumption can be reduced by limiting the processing and memory capabilities of the headset unit. In turn, this requires “clever” (power-aware) processing of received and transmitted data.

At an even higher hierarchical level, an example of a power-aware software implementation is the efficiency of a compiled code [28]. An example of application-level adaptivity is scaling the operating power and clock frequency in a general-purpose processing unit under the control of power-aware applications, such as video- and audio-decoding software. Here, dynamic adjustment of the supply voltage can be traded for processor speed, allowing considerable power savings in the digital circuitry [29].

A framework for the exchange of performance and power consumption information between receiver, hard disk, central-processing unit, operating system and the application has been developed within the Ubiquitous Communications project [23]. It is an example of a fully adaptive low-power mobile system.

1.4 Why Multistandard and Adaptive RF?

Continuous migration towards higher data rates and higher channel capacities and provision of various services (such as text, audio and video) for multimedia applications require not only adaptive and low power designs, but also the designs that work across multiple bands and standards.

Multistandard front-ends typically use duplicate circuit blocks, or even entire radio front-ends for each standard. Although this approach is simpler to implement, it is neither optimal in cost nor in power consumption [30]. When different standards do not operate simultaneously, circuit blocks of a multistandard handset can be shared. By using circuits that are able to trade off power consumption for performance on the fly, i.e., *adaptive multi-standard circuits*, considerable power can be saved. There is currently an apparent migration in RF IC design towards multi-mode multi-band integrated modules for low-noise amplifiers [31], oscillators [32], power amplifiers [12] and transceivers [25].

For multistandard low-noise amplifiers and mixers, adaptivity comes down to trading off dynamic range for power consumption, whereas for adaptive multistandard oscillators a trade-off between phase noise, oscillation frequency and power consumption matters. Design of multistandard oscillators and multistandard front-ends is discussed in detail in this book.

In addition to multimode capability at radio frequencies, adaptivity should be implemented at baseband frequencies as well. After a signal is downconverted to the baseband, it must be filtered, amplified and digitized. In order to accommodate multiple radio standards with different bandwidths and modulation schemes, multistandard receivers require different channel, and image-reject filter bandwidths, and different analogue-to-digital converter (ADC) resolutions. For example, a variable-bandwidth baseband filter and variable-resolution ADC can be used to alternate between different modes of operation [33-37].

Finally, because adaptive multistandard low-power RF front-ends are able to share building blocks across different standards, they have advantages over their predecessors: they use a smaller chip area, and most importantly, have a potential for lower overall cost.

1.5 Adaptivity Objectives

The overall goal of this work is to develop design methodologies and a proof-of-concept for analog RF front-end circuits that trade performance for power

consumption in an *adaptive* way. This results in a transceiver front-end that either consumes less average power for a given performance or offers better performance for a given average power compared to a conventional transceiver front-end.

When exploring the fundamental and practical limits of an adaptive radio frequency implementation for multiple communication standards, we have examined basic aspects of the physical mechanisms underlying the operation of adaptive RF front-end circuits, and have developed design methodologies for their *structured synthesis*.

The techniques and methodologies developed have been validated by specifying requirements and implementing adaptive wireless receiver circuits and an adaptive wireless receiver front-end for multiple communication standards.

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Chapter 2

PERFORMANCE PARAMETERS OF RF CIRCUITS

Interdisciplinarity is essential to RF circuit design. An RF designer is a system designer, an analogue circuit designer, a microwave circuit designer, and a passive and active component designer.

Gain, noise figure, phase noise, distortion, and dynamic range are only a few of the parameters of interest to an RF IC designer, which are reviewed in this chapter. The performance parameters of the front-end part of a receiver are then determined.

2.1 Gain Parameters

Current, voltage and power are fundamental circuit design quantities. The choice of the input and output quantities determines the transfer function of a two-port network [1]: power gain, voltage gain, current gain, transconductance gain and transimpedance gain. Usually, signal power is taken as a design variable when maximum power transfer (i.e., conjugate impedance match) is desired [2]. This is required at input of a receiver, because of the impedance match to the receive antenna (in order to avoid signal reflection), between front-end circuits in heterodyne receivers, and also when interconnect dimensions are on the order of the signal wavelength (e.g., microwave circuit design). On the other hand, voltage and/or current quantities can be the preferable design choice for circuits in homodyne receivers where stages reside on-chip and power matching is not required (e.g., the interface between very large and very small impedances).

For a two-port network connected to load impedance Z_L, source impedance Z_S, and characterized by a scattering matrix [*S*] [3-10] and/or chain matrix [*ABCD*] (see Fig. 2.1), a number of gain definitions are in use [11-15].

The *transducer* power gain (g_T) stands for the ratio of the power delivered to the load (P_L) and the power available from the source (P_{AVS}). If Γ_{IN} and Γ_{OUT} are the input and the output reflection coefficients (which characterize

quality of input and output two-port impedance matching), and Γ_S and Γ_L the reflection coefficients of the source and the load respectively, this gain definition becomes [12]

$$g_T = \frac{P_L}{P_{AVS}} = \frac{|S_{21}|^2 (1-|\Gamma_L|^2)(1-|\Gamma_S|^2)}{|1-\Gamma_{IN}\Gamma_S|^2 |1-S_{22}\Gamma_L|^2}, \tag{2.1}$$

where S_{11}-S_{22} are the parameters of the two-port scattering matrix [*S*]. The *S*-parameters can be directly measured with a vector network analyzer, and are especially useful at high frequencies (e.g., order of GHz) where it is difficult to measure currents and voltages.

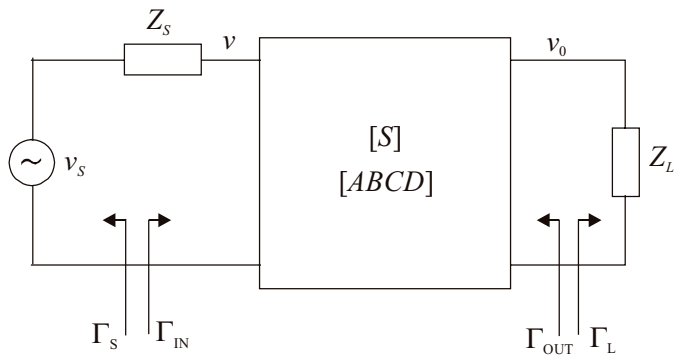

Figure 2.1: A two-port network.

From the relationship between the *S*-parameters and chain-matrix parameters (*A,B,C,D*) [13,14], the transducer power gain can also be expressed as

$$g_T = \frac{4R_L R_S}{|AZ_L + B + CZ_S Z_L + DZ_S|^2}, \tag{2.2}$$

where R_S and R_L are the real parts of the source and load impedances, respectively, and *A, B, C* and *D* are the parameters of the chain matrix. This matrix is especially useful for characterization of a cascade connection of two-port networks (e.g., a receiver) by multiplying the individual *ABCD* matrices of the individual two-ports. In a similar manner, the impedance *Z*-parameters and the admittance *Y*-parameters can be used to describe the

relationship between total voltages and currents at network ports. Whereas analogue circuit designers are more familiar with voltages and currents (i.e., *Z-, Y-, ABCD*-parameters), microwave circuit designers prefer *S*-parameters.

The transducer power gain depends on both the source and the load impedances (i.e., mismatches Γ_S and Γ_L). This gain parameter can be easily extracted from measurements (required impedance match with signal generator only). Moreover, a maximum operation frequency (f_{MAX}) of a device can be directly estimated from the measured unilateral (S_{12}=0) transducer power gain.

In the case of matched input and output impedances for a two-port network, the *available* power gain (g_A) can be defined. It stands for the ratio of the power available from the two-port network and the power available from the source (P_{AVS}). The transducer power gain equals the available power gain when the input and output are power matched simultaneously.

Throughout the book we refer to the transducer power gain if only the input power match condition is satisfied. For a simultaneous input and output power match, we refer to the available power gain (which in this case equals the transducers power gain).

If v_S is the signal voltage swing at the source and v_0 is the output voltage swing (at the load; see Fig. 2.1), the relationship between the transducer power gain and the voltage gain (*vg*, from the source) can be determined as

$$vg^2 = \frac{v_0^2}{v_S^2} = \frac{v_0^2 / R_L}{v_S^2 / 4R_S} \frac{R_L}{4R_S} = g_T \frac{R_L}{4R_S}, \tag{2.3}$$

where the input power match, and real source and load impedances (R_S and R_L) are assumed. When we consider the voltage gain from the input of the two-port network (i.e., not with respect to v_S), voltage and power gain definitions are equal when expressed in decibels for R_L=R_S.

2.1.1 Stability

We distinguish between unconditional and conditional stability of a two-port network [12,16-18]. If Γ_{IN} and Γ_{OUT} are less than one only for a range of source and load impedances, then the two-port network is conditionally stable, because impedances outside of this range may cause oscillations (i.e., the real part of either the input or output two-port impedance has a negative real part). If Γ_{IN} and Γ_{OUT} are always below one, the two-port is unconditionally stable.

The conditional stability criterion can be expressed as [4]

$$\left|\Gamma_{IN}\right| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right| < 1\,, \tag{2.4}$$

$$\left|\Gamma_{OUT}\right| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}\right| < 1\,. \tag{2.5}$$

A device is unconditionally stable if Rollet's condition [19] (Eq. (2.6)) is satisfied.

$$K = \frac{1 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2 + \left|\Delta\right|^2}{2\left|S_{21}S_{12}\right|} > 1 \qquad \Delta = S_{11}S_{22} - S_{12}S_{21} < 1 \tag{2.6}$$

As this condition involves constraints on two different parameters, it is difficult to compare the stability of different devices. However, the μ test [20,21] for the unconditional stability can be used for both testing and comparison, and is given by Eq. (2.7).

$$\mu = \frac{1 - \left|S_{11}\right|^2}{\left|S_{22} - S_{11}^{*}\Delta\right| + \left|S_{12}S_{21}\right|} > 1 \tag{2.7}$$

This condition reads as: the larger the μ, the better the stability. Generally, figures expressed with *S*-parameters can be conveniently mapped and followed using Smith charts [10].

If there is feedback in a circuit, the stability criteria can be related to loop gain and loop phase shift [15].

2.1.2 Matched Gain Parameters

Referring to Eq. (2.1), we can distinguish between the gain factors of the source matching network g_S, Eq. (2.8), of the designed two-port network (Fig. 2.1) g_0, Eq. (2.9), and of the load matching network g_L, Eq. (2.10) [11,12].

$$g_S = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{IN}\Gamma_S|^2} \tag{2.8}$$

$$g_0 = |S_{21}|^2 \tag{2.9}$$

$$g_L = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2}. \tag{2.10}$$

For the maximum power transfer, the input impedance of the two-port network must be conjugate matched to the impedance of the source-matching network, and the output impedance of the two-port network must be conjugate matched to the impedance of the load-matching network [12]. This condition is satisfied if

$$\Gamma_{IN} = \Gamma_S^* \qquad \Gamma_{OUT} = \Gamma_L^*. \tag{2.11}$$

Input and output power match design practice is common to circuits of a heterodyne receiver. If the matching conditions are violated at either the input or the output of an external (usually 50Ω terminated) image-reject or channel-select filter, the passband and stopband characteristics of the filter will exhibit loss and ripples [2].

However, for an ideal voltage or current amplification, different requirements result, as shown in Table 2.1. For example, infinite impedance at the input of the two-port is expected for the maximum voltage gain (Γ_{IN}=1), whereas zero input impedance enables the maximum current gain (Γ_{IN}=-1). This design practice is common to circuits where power matching is not required (e.g., homodyne receiver circuits).

Table 2.1: Reflection coefficients for ideal current (Z_{IN}=0) and voltage (Z_{IN}->∞) quantities; Z_{IN} is the input impedance of a two-port network.

input voltage	**input current**
Z_{IN}->∞, Γ_{IN}=1	Z_{IN}=0, Γ_{IN}=-1

2.2 Nonlinearity Parameters

As a minimal detectable signal at the input of wireless receivers can be an order of microvolt large, it must be heavily amplified (without distortion) for further processing.

If a system is linear and memoryless, then its output can be presented as

$$y(t) = ax(t)\,, \tag{2.12}$$

where $x(t)$ is an input signal and $y(t)$ is the output signal.

For memoryless nonlinear systems, the input-output relationship has the form

$$y(t) = a_0 + a_1 x(t) + a_2 x(t)^2 + ... \tag{2.13}$$

The parameters a_i are time dependent for time-varying systems.

Whereas a linear model can approximate an RF circuit for small input signals (e.g., -100dBm), for large input signals (e.g., -10dBm) or for heavily amplified signals, an RF circuit is characterized by a nonlinear model.

By inspecting the response to a sinusoidal excitation ($x(t)=A\cos\omega t$) using the nonlinear model (Eq. (2.13)), we can describe numerous nonlinearity phenomena (from Eq. (2.14)).

$$y(t) = \frac{a_2 A^2}{2} + (a_1 A + \frac{3}{4} a_3 A^3)\cos\omega t + \frac{a_2 A^2}{2}\cos 2\omega t + \frac{1}{4} a_3 A^3 \cos 3\omega t + ... \tag{2.14}$$

In the remainder of this section we will comment on gain compression, desensitization, cross modulation and intermodulation [22-39].

In a symmetric system (odd-order terms eliminated) dominated by the third-order term [22,23] (i.e., higher-order terms neglected as they are small compared to lower-order terms), from Eq. (2.14), the gain g of the nonlinearly modeled system is

$$g = a_1 + \frac{3}{4} a_3 A^2\,. \tag{2.15}$$

If $a_3<0$, the gain is a decreasing function of amplitude A. The 1-dB *compression point* quantifies this gain reduction effect [2]. It is defined as the

input signal level at which the gain g is reduced by 1dB compared to the linear gain term (a_1). From Eq. (2.15), this point is

$$A_{1\text{dB}} = \sqrt{0.145\left|\frac{a_1}{a_3}\right|}\,. \tag{2.16}$$

Note that the signal at the output of an analogue circuit is a result of the combination of the factors: nonlinear model (2.13) as well as bias conditions. Therefore, for very large input signals, the gain can even become zero, because either the output signal is limited by the bias supply quantity (see Fig. 2.2), or $a_3<0$ (see Eq. (2.15)).

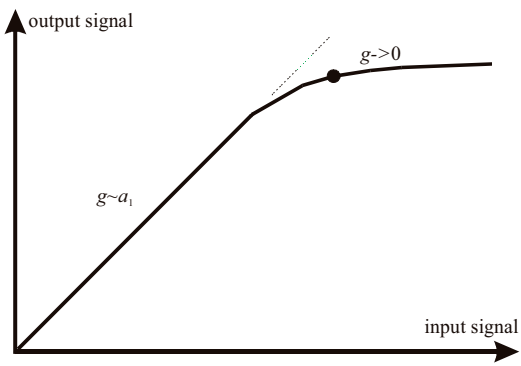

Figure 2.2: A relationship between the input and output signal amplitudes under the constraint of bias (supply) conditions in a nonlinear system.

In the presence of a strong interferer, the desired signal may experience a very small gain. If the signal (a desired signal at an angular frequency ω_1 and an interferer at ω_2) applied at the input of a nonlinear system has the form

$$x(t) = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t\,, \tag{2.17}$$

the gain of the desired signal can be calculated after combining Eqs. (2.13) and (2.17). The term representing the content of the output signal around the angular frequency ω_1 becomes

$$y(t) \cong (a_1 + \frac{3}{2} a_3 A_2^{\,2}) A_1 \cos \omega_1 t \,. \tag{2.18}$$

For sufficiently large A_2, the gain term may drop to zero. This effect is referred to as *blocking* [2]. The interferer leading to this effect is called the blocking signal.

If the amplitude of a strong interferer is modulated and applied to the input of a nonlinear system along with a desired signal, then at the output the desired signal experiences the effect of a modulated interferer. This phenomenon is called *cross modulation* [2,24,25].

2.2.1 Intermodulation

When signals of different frequencies are applied to the input of a nonlinear system, not only does the output exhibit components that are harmonics of the input signals, but also of their combinations. This phenomenon is referred to as *intermodulation* [2,26,27]. If the input signal is given by Eq. (2.17), the following terms are generated at the output of the system (2.13):

desired component: $$(a_1 + \frac{3}{4} a_3 A_1^{\,2} + \frac{3}{2} a_3 A_2^{\,2}) A_1 \cos \omega_1 t \tag{2.19}$$

second-order distortion component: $$a_2 A_1 A_2 \cos(\omega_1 - \omega_2) t \tag{2.20}$$

third-order distortion component: $$\frac{3}{4} a_3 A_1^{\,2} A_2 \cos(2\omega_1 - \omega_2) t \tag{2.21}$$

These are the fundamental component, Eq. (2.19), the second-order intermodulation component, Eq. (2.20), and the third-order intermodulation component, Eq. (2.21).

Due to mismatches in real designs, the distortion that originates from the second-order nonlinearities must be taken into account, even in differential circuits (even components fractional matching below 1% can be critical [28]). Especially, circuits that transform a high-frequency input spectrum to the baseband would suffer from this type of the distortion (e.g., homodyne receivers). This phenomenon is referred to as *second-order intermodulation distortion* [29].

As third-order intermodulation products are located near the desired signal, it is often difficult to filter them out without affecting the information content. It is therefore expected that such in-band products will distort the output signal. The associated phenomenon is referred to as *third-order intermodulation distortion* [2,26,27].

Second- and third-order intercept points characterize the introduced intermodulation distortion phenomena. They are derived in the remainder of this section.

2.2.1.1 Third-Order Intercept Point

Referring to Eqs. (2.19) and (2.21), and assuming $A_1=A_2=A$, it can be seen that the output power of the third-order products increases with the cube of the input power, whereas the fundamental output power is proportional to the input power [23]. This effect is shown in Fig. 2.3.

A hypothetical intersection point where the first-order power product (P_O) and the third-order power product (P_{OIM3}) are equal is called *third-order intercept point* (IP3). Table 2.2 describes the notation that is used throughout this book.

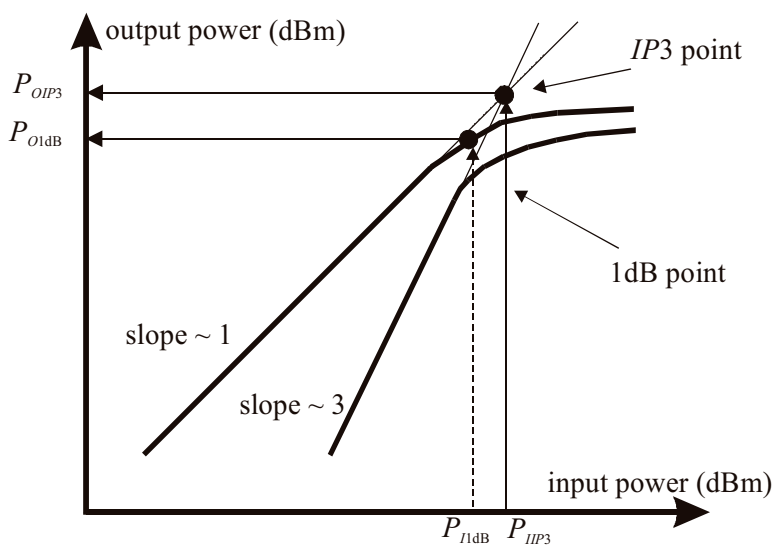

Figure 2.3: Input-output power relationship of a nonlinear device.

If the corresponding power definitions are given by Eq. (2.22),

$$P_O = \frac{1}{2}a_1^2 A^2 \qquad P_{OIM3} = \frac{1}{2}(\frac{3}{4}a_3 A^2 A)^2 = \frac{9}{32}{a_3}^2 A^6 , \tag{2.22}$$

the amplitude of the input-referred third-order intercept point (A_{IIP3}) becomes

$$A_{IIP3} = \sqrt{\frac{4a_1}{3a_3}} . \tag{2.23}$$

Once the parameters a_0, a_1, … of the corresponding circuit are determined, the intercept point can be calculated. What is more, the effects of distortion can be fully encompassed only by analysis at the circuit level, after all circuit nonlinearity contributors are taken into account [30-37]. For example, A_{IIP3} for a single bipolar transistor, as derived from Eq. (2.23) using the simplified exponential characteristic [38], is $A_{IIP3}=\sqrt{8}V_T$ (V_T is the thermal voltage).

Table 2.2: Amplitude-power-dB scale notation.

parameter\presentation	**amplitude**	**power**	**dB scale**
3rd-order input-intercept point	A_{IIP3}	P_{IIP3}	*IIP*3
3rd-order output-intercept point	A_{OIP3}	P_{OIP3}	*OIP*3
3rd-order input-referred intermodulation product	A_{IIM3}	P_{IIM3}	*IIM*3
3rd-order output-referred intermodulation product	A_{OIM3}	P_{OIM3}	*OIM*3
input desired signal	A	P	P [dB]
output desired signal	A_O	P_O	P_O [dB]

The equivalent IIP3 of, most generally, an n-stage cascaded network equals [2,39,40]

$$\frac{1}{{A_{IIP3}}^2} = \frac{1}{{A_{IIP3,1}}^2} + \frac{{a_1}^2}{{A_{IIP3,2}}^2} + \frac{{a_1}^2{b_1}^2}{{A_{IIP3,3}}^2} + \ldots , \tag{2.24}$$

where $A_{IIP3,1}$, $A_{IIP3,2}$, … are the third-order input-intercept amplitudes and a_1, b_1, … are the linear gain coefficients of the corresponding blocks in a receive chain (similar to Eq. (2.13)).

An important conclusion that can be derived from the above result is the inverse proportionality of the first-stage linear gain a_1 and the overall *IIP*3. Namely, a larger gain of the first stage results in a larger intermodulation product that is responsible for an even larger distortion at the output of the second stage.

Note that IIP3 cannot be obtained directly from measurements, but as an intersection between the extrapolated linear and third-order intermodulation responses (Fig. 2.3), which are, however, obtained for small input signals. The reason for this is that *IIP*3 is often far beyond the maximal signal range of the system.

2.2.1.2 Second-Order Intercept Point

A hypothetical intersection point of the first-order product (a_1A) and the second order product (a_2A^2) of a nonlinear system is *second-order intercept point* (IP2) [29]. The amplitude of the input-referred IP2 is defined as

$$A_{IIP2} = \frac{a_1}{a_2}. \tag{2.25}$$

Similar to the derivation of the cascaded *IIP*3, the cascaded second-order input-intercept point (*IIP*2) can be expressed as

$$\frac{1}{A_{IIP2}} = \frac{1}{A_{IIP2,1}} + \frac{a_1}{A_{IIP2,2}} + \frac{a_1 b_1}{A_{IIP2,3}} + \ldots, \tag{2.26}$$

where $A_{IIP2,i}$ are the input-referred second-order intercept amplitudes of the corresponding cascaded stages.

2.3 Noise Figure

The reduction in signal-to-noise ratio (SNR) throughout a two-port network is characterized by the *noise factor* [41].

$$F = \frac{SNR_I}{SNR_O} = \frac{S_I / N_I}{S_O / N_O} \tag{2.27}$$

Here, SNR_I and SNR_O are the input and output signal-to-noise ratios, respectively. S_I and N_I are the input signal power and the input noise power, and S_O and N_O are the output signal and noise power (see Fig. 2.4). When expressed in decibels (dB), this ratio is called the *noise figure*.

The general expression for noise factor is given below [42-47],

$$F = F_{MIN} + \frac{R_N}{G_S}\left[(G_S - G_{OPT})^2 + (B_S - B_{OPT})^2\right], \tag{2.28}$$

where F_{MIN} is the minimum noise factor, R_N the equivalent noise resistance, G_S and B_S the source conductance and susceptance, and G_{OPT} and B_{OPT} the optimum source admittance parameters corresponding to the minimum noise factor. The source admittances that minimize noise factor and maximize power transfer (impedance match) of a two-port network are usually not the same. Therefore, orthogonal optimization for noise figure and power transfer is required if one wants to enjoy simultaneous noise and power match (if possible). Whereas F_{MIN} stands for the noise factor achieved under noise-matched conditions, noise resistance R_N characterizes the sensitivity of the minimum noise figure to changes in the source impedance.

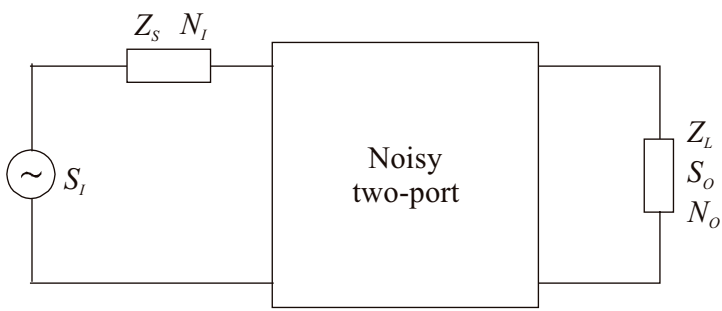

Figure 2.4: A noisy two-port network.

On the other hand, microwave designers are more familiar with the noise-factor definition that is related to reflection coefficients of a two-port network, Eq. (2.29) [4],

$$F = F_{MIN} + 4\frac{R_N}{Z_0}\frac{\left|\Gamma_S - \Gamma_{OPT}\right|^2}{(1-\left|\Gamma_S\right|^2)\left|1+\Gamma_{OPT}\right|^2}, \tag{2.29}$$

where Γ_{OPT} is the optimum reflection coefficient corresponding to the optimum source admittance that provides the minimum noise factor, and Γ_S is the source reflection coefficient.

The noise parameters, F_{MIN}, R_N, and Γ_{OPT}, are characteristics of the device, and they can be measured with a noise-figure test set, or determined from the device *S*-parameters.

Another noise figure of merit is the *noise temperature*, T_E [48]. By referring to Fig. 2.4, we can establish the relationship between the noise factor and noise temperature as follows.

Parameters of the two-port network are the power gain g, the bandwidth B, and the noise temperature T_E. The noise temperature of the source is T_0. If the input noise power corresponding to the matched condition and temperature T_0=290K equals N_I=KT_0B, the output noise power is

$$N_O = KB(T_0 + T_E)g\,. \tag{2.30}$$

Now, the relationship between the noise figure and the equivalent noise temperature can be obtained by combining Eqs. (2.27) and (2.30) as

$$F = 1 + \frac{T_E}{T_0} \qquad T_E = (F-1)T_0\,. \tag{2.31}$$

The use of the noise factor is in some situations error prone. Namely, the noise factor of a receiver is defined for the input noise level of KT_0B, i.e., the source temperature T_0. However, as the noise originating from the source (i.e., an antenna with a noise temperature T_A) is generally KT_AB, the calculation of the output noise power using the noise factor (Eq. (2.32)) is correct only if T_A=T_0.

$$N_O = N_I F\frac{S_O}{S_I} = N_I Fg = KT_A BFg \tag{2.32}$$

Finally, the equivalent noise factor F for the cascaded connection of the stages is given by Friis formula [49],

$$F = F_1 + \frac{F_2 - 1}{g_1} + \frac{F_3 - 1}{g_1 g_2} + \ldots, \tag{2.33}$$

where g_i and F_i are the power gain and noise factor values of the corresponding stages. Similarly, the equivalent noise temperature T_E of an n-stage cascaded system has a form [49]

$$T_E = T_{E1} + \frac{T_{E2}}{g_1} + \frac{T_{E3}}{g_1 g_2} + \ldots \tag{2.34}$$

2.4 Phase Noise

Power of an oscillation signal (e.g., $v(t)$) is ideally concentrated at one frequency (f_0), so that

$$v(t) = V_0 \cos \omega_0 t \,. \tag{2.35}$$

However, as the oscillation signal is generated by non-ideal (thus noisy) circuit components [46,49-51], the actual power spreads over a number of frequency components (i.e., a frequency range), as shown in Fig. 2.5.

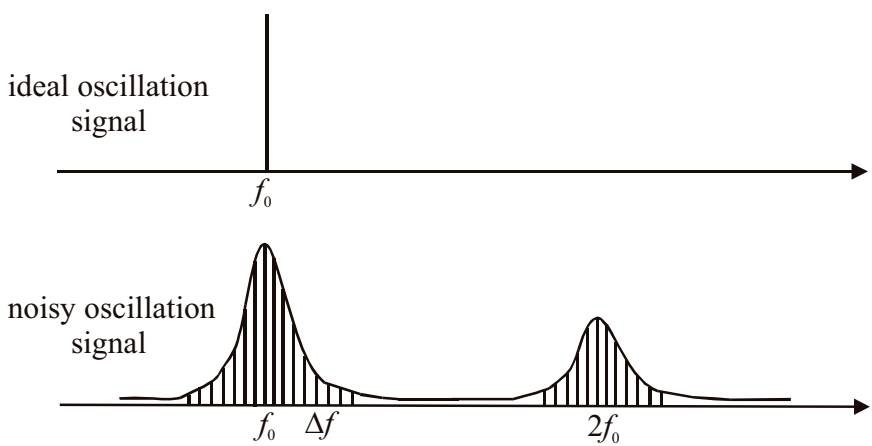

Figure 2.5: Spectra of an ideal and a real (noisy) oscillation signal.

The oscillation-signal skirt is responsible for the mixing of a number of components (desired and undesired) to the same frequency. For example, a desired signal (f_{RF}) converts with an oscillation signal (f_0) to a low frequency ($\Delta f=f_{RF}-f_0$). On the other hand, an undesired interferer at frequency $f_{RF}+\Delta f$ converts with the component of the oscillation signal at $f_0+\Delta f$ to the same frequency Δf. This phenomenon is referred to as *reciprocal mixing* [2], and it is responsible for the deterioration of the converted desired signal content.

The real (noisy) oscillation signal (Fig. 2.4) has a form,

$$v(t) = V_0(1 + A(t))\cos(\omega_0 t + \Phi(t)) \tag{2.36}$$

where $A(t)$ is an amplitude-modulating (AM) component and Φ(t) is a phase-modulating (PM) component [52]. The spectral component of the oscillation signal and the corresponding AM and PM noise components at certain offset frequency Δf from the carrier are depicted by Fig. 2.6.

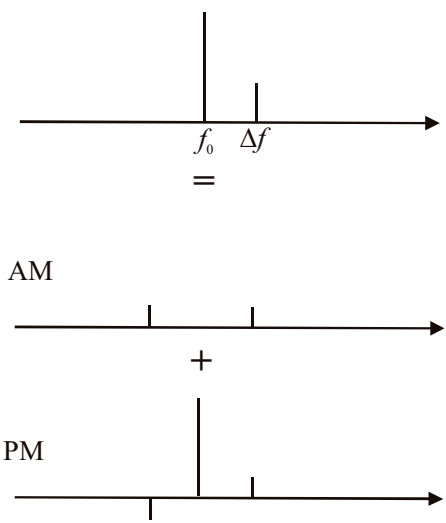

Figure 2.6: AM and PM modulated components of an oscillation signal.

As the AM component can be removed by, for example, an amplitude control mechanism of an oscillator [53,54], the PM component determines a deviation from the ideal case (Eq. (2.36)).

Therefore, the noisy nature of oscillators (random variation of oscillation phase) is described by the *phase noise*. This figure of merit is defined as the ratio of the noise power in a 1Hz bandwidth at an offset frequency (Δf) from the carrier and the signal power (at f_0) (see Fig. 2.6) [55,56]. The Intuitive Leeson's formula [56], Eq. (2.37),

$$\mathcal{L} = F\frac{KT}{2P}\frac{1}{Q^2}\left(\frac{f_0}{\Delta f}\right)^2, \tag{2.37}$$

shows the relationship between the phase noise $\mathcal{L}$ of a harmonic oscillator and its design parameters, i.e., oscillator noise factor F, oscillation signal power P, quality of resonator Q, and frequency parameters (K is Boltzman's constant and T is absolute temperature).

2.5 Dynamic Range

The capability to process both the weakest and the strongest signals is referred to as *dynamic range*. Among a number of definitions two are most used, viz., the *linear* and *spurious free dynamic range* (SFDR).

The linear dynamic range is defined as a difference between the input signal level that causes 1dB gain compression and the minimum input signal level that can be distinguished from the noise. This is a useful figure for power amplifier designers.

For low-noise amplifiers and mixers, however, operation may be limited by noise at the low end, and the maximum power level for which distortion becomes unacceptable at the high end.

The range where the spurious response is minimal is referred to as spurious free dynamic range. The higher end of the SFDR is determined by the signal power level (P_{MAX}) at which the (output) third-order intermodulation product is equal to the noise level (N_O). The lower end is related to the minimum detectable signal, i.e., a signal power level (P_{MIN}) that allows for detection with a desired signal-to-noise ratio and accordingly desired error probability (or bit error rate). The SFDR is defined by Eq. (2.38), whereas Fig. 2.7 gives a graphical interpretation.

$$SFDR[\text{dB}] = P_{MAX}[\text{dB}] - P_{MIN}[\text{dB}] \tag{2.38}$$

In order to calculate the SFDR, we will first determine the relationship between the linear product (P_O) and the IM3 product (P_{OIM3}) of a nonlinear system (e.g., Eq. (2.13)).

With the aid of Eqs. (2.22) and (2.23), the power of the output third-order intermodulation product (see Table 2.1) can be expressed as

$$P_{OIM3} = \frac{9}{32} a_3^{\,2} A^6 = \frac{a_1^{\,6} A^6 / 8}{4a_1^{\,6} / 9a_3^{\,2}} = \frac{P_O^3}{P_{OIP3}^2}. \tag{2.39}$$

Transforming Eq. (2.39) into a dB-scale, the linear input-referred power product becomes

$$P\,[\mathrm{dB}] = \frac{2IIP3 + IIM3}{3}. \tag{2.40}$$

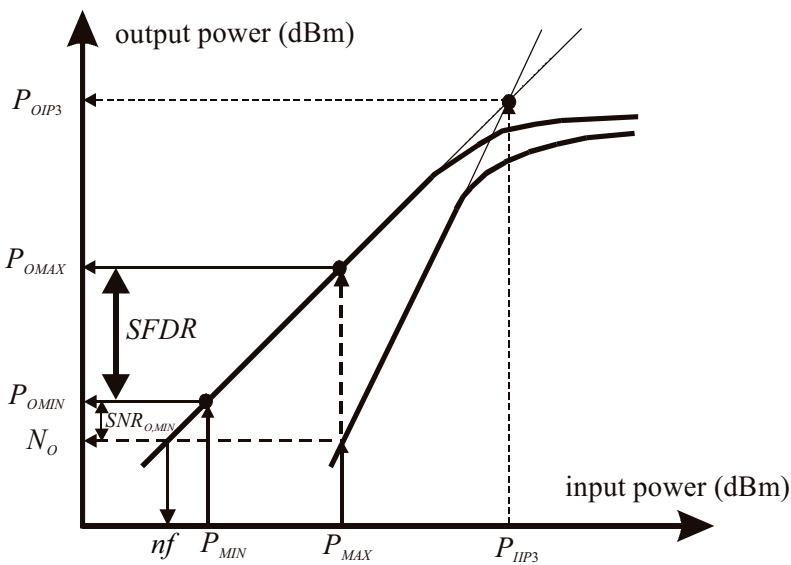

Figure 2.7: Dynamic range analysis.

Now, the maximum input power level (P_{MAX}) is obtained by equating the *IIM*3 with the input-referred system noise floor (*nf*) in accordance with the definition of the *SFDR*,

$$P_{MAX}\left[dB\right] = \frac{2IIP3 + nf}{3}, \tag{2.41}$$

where

$$nf = 10\log KTB + NF\ . \tag{2.42}$$

K is *Boltzmann's* constant, *T* is the absolute temperature, and *NF* is the noise figure.

On the other hand, the minimum input power (P_{MIN}) refers to the signal power that provides a system with a desired minimal (output) signal-to-noise ratio $SNR_{O,MIN}$. This is given by Eq. (2.43).

$$P_{MIN} = nf + SNR_{O,MIN}[\text{dB}] \tag{2.43}$$

Finally, the *SFDR* is obtained (Eq. (2.44), [2]) as a difference between P_{MAX} and P_{MIN}.

$$SFDR[\text{dB}] = \frac{2}{3}(IIP3 - nf) - SNR_{O,MIN}[\text{dB}] \tag{2.44}$$

As the output noise power is $N_O = g \cdot nf = gkBT_0F$ (assuming a gain *g* and an antenna temperature T_0), Eq (2.44) transforms into

$$SFDR[\text{dB}] = \frac{2}{3}(OIP3 - N_O[\text{dB}]) - SNR_{O,MIN}[\text{dB}]\ . \tag{2.45}$$

This equation allows for the estimation of the distortion-free dynamic range (in third-order intermodulation distortion dominated systems) once the output third-order intercept point, the output noise power and the minimum signal-to-noise ratio are known.

2.6 RF Front-End Performance Parameters

A block diagram of a front-end part of a receiver, consisting of a low-noise amplifier (LNA), a filter, and a mixer, is shown in Fig 2.8. Given the circuit block specifications, a number of receiver performance parameters will be determined, viz., the gain, the noise figure, the linearity, the dynamic range.

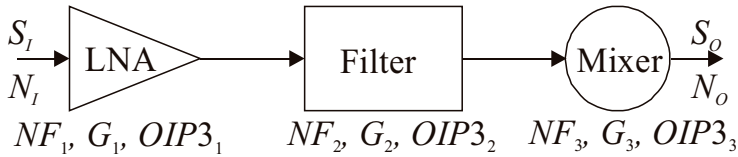

Figure 2.8: A simplified RF front-end receiver model.

In order to put the previously defined parameters into the context of RF front-end circuit design, we will use an example. Let us therefore assume the following operation conditions and circuits parameters:

- The operation frequency is f=1850MHz, the channel bandwidth B=200kHz, the bit rate R_B=14.4kb/s, the desired error probability $P_E=10^{-5}$, and the modulation *GMSK* type [2].

- The transmit power is P_T=30dBm, the transmit antenna gain G_T=1dB, the minimum distance between receiver and transmitter R_{MIN}=10m, the receive antenna gain G_R=1dB, and the antenna noise temperature T_A=900K.

- The power gains G_i, noise figures NF_i and output intercept points $OIP3_i$ of the corresponding blocks (see Fig. 2.8) are given in Table 2.3.

Table 2.3: Performance parameters of the receiver circuits.

Performance\Blocks	**LNA**	**RF Filter**	**Mixer**
G	15dB	-2dB	4dB
NF	2dB	2dB	14dB
*OIP*3	15dBm	-	10dBm

Referring to the definitions and calculations of the previous sections, we can determine the receiver performance parameters as follows.

- The system power gain is

$$G = G_1 + G_2 + G_3 . \tag{2.46}$$

Substituting values given in Table 2.4, this results into G=17dB.

- The system noise factor is

$$F = F_1 + \frac{F_2 - 1}{g_1} + \frac{F_3 - 1}{g_1 g_2}, \tag{2.47}$$

where g_1 and g_2 are the linear gain terms (total gain g=$g_1 g_2$). For the given noise-figure values, NF=10log$F$=4.6dB.

- The system $IIP3$ is

$$IIP3 = -10\log(10^{-\frac{OIP3_1 - G_1}{10}} + 10^{-\frac{OIP3_2 - G_2 - G_1}{10}} + 10^{-\frac{OIP3_3 - G_3 - G_2 - G_1}{10}}). \tag{2.48}$$

For the given $OIP3$ values, $IIP3$=–2.1dBm.

- The output noise power is

$$N_O = K[T_A + (F-1)T_0]Bg. \tag{2.49}$$

- The minimum output SNR [52] is

$$SNR_{O,MIN} = \frac{R_B}{B}\frac{E_B}{n_O}, \tag{2.50}$$

where the energy-per-bit-to-noise ratio, E_B/n_O, can be determined from

$$P_E = \frac{1}{2} erfc(\sqrt{\frac{E_B}{n_O}}). \tag{2.51}$$

- The spurious free dynamic range [2] is

$$SFDR[dB] = \frac{2}{3}(OIP3 - N_0[dB]) - SNR_{O,MIN}[dB]. \tag{2.52}$$

- The minimum detectable input signal (the receiver sensitivity) [2] is

$$S_I = P_{MIN} = SNR_{O,MIN}\frac{N_0}{g} = SNR_{O,MIN}KB[T_A + (F-1)T_0]. \qquad (2.53)$$

- The required receiver dynamic range (*DR*) [12] is

$$P_{MIN} = S_I \qquad P_R\Big|_{R=R_{MIN}} = \frac{g_R g_T P_T \lambda^2}{(4\pi R_{MIN})^2} \qquad (2.54)$$

$$DR = P_R\Big|_{R=R_{MIN}}[\text{dB}] - P_{MIN}[\text{dB}]. \qquad (2.55)$$

P_R is the receive signal power (a more accurate model can be found in [57]), λ the signal wavelength, and g_T and g_R the corresponding linear gain terms.

As the sensitivity depends on the minimum SNR, which depends on the ratio of the bit energy and the noise-power spectral density, where the latter is related to the desired probability of error, the dynamic range is dependent on both the modulation type and the SNR.

- The maximum range of operation, R_{MAX} [12], is

$$R_{MAX} = \sqrt{\frac{P_T g_T g_R \lambda^2}{(4\pi)^2 P_R}}, \qquad (2.56)$$

if the required receive signal power equals

$$P_R = E_B R_B = \frac{E_B}{n_0} n_0 R_B = \frac{E_B}{n_0} K[T_A + (F-1)T_0]R_B. \qquad (2.57)$$

2.7 Conclusions

A number of definitions essential to RF design are outlined in this chapter. The gain, nonlinearity and noise parameters are revisited, followed by a discussion on the dynamic range and the receiver performance.

The reviewed parameter definitions form a base for the characterization of the RF circuits and systems.

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Chapter 3

SPECTRUM-SIGNAL TRANSFORMATION

For the last few decades, there haven't been significant breakthroughs at receiver system-level design, as frequently only a few architectures have been exploited: high-IF [1,2] and zero-IF topologies [3,4], and lately low-IF topologies [5]. Even though a small number of different topologies are in use, the high-level receiver front-end characterization lacks a unique presentation, which in turn prevents research of new design strategies and architectures at the system level.

Moreover, most of the existing system studies on RF front-ends [6,7,8] fail to present how signals and spectra are transformed from an antenna input to the backend of the receiver in a consistent way. Without the understanding of the signal and spectrum transformations throughout a front-end, it is difficult to grasp all design concepts at the RF system level and the RF circuit level.

Therefore, a unique presentation of spectral and signal transformation in receiver RF front-ends is introduced in this chapter. The approach presented here gives insight into high-level modelling of RF front-ends [9], and accordingly can lead to new design strategies. Various mixer-oscillator models are introduced that allow for an all-encompassing interpretation of both signal and spectral transformations in different receiver architectures.

This chapter is organized as follows. First, the existing RF front-end architectures are briefly outlined followed by a description of the signal and (signal's) spectral (SS) transformations in a quadrature downconverter topology. Different mixer-oscillator (MO) models are then introduced. Using the presentation of transformation of signals and their spectra, and MO models, a comprehensive analysis of a number of RF front-end topologies is performed. Finally, the mixer-oscillator models and the spectrum-signal presentation are applied to the calculation of the image-rejection ratio of quadrature receiver topologies, illustrating their utility.

3.1 Transceiver Architectures

The vast use of communication equipment imposes strict regulations on communication standards, and accordingly RF circuit and system designs. To provide users with good quality of service (QoS), a number of issues in various disciplines must be considered. Designers search for more efficient coding techniques and modulation schemes, better transmission and reception schemes, higher-performance circuits and systems, lower-power and higher-speed baseband signal processing, more efficient protocols, and higher energy-density batteries. We will focus on the RF system-level issues in this chapter.

The role of an analogue RF front-end is to downconvert a signal received by a receive antenna to a digital back-end. The receiver architecture is called a high-IF architecture [1,2,10-22] if an intermediate frequency (IF) prior to the back-end processing unit doesn't fall into the range of the baseband signal-processing capabilities of the current era (tens of MHz at the time of writing). The architecture is known as a homodyne or zero-IF [3,4,23-49] for a zero intermediate frequency, and as a low-IF architecture [5,7,50-56] for a low IF (a frequency that falls into the baseband processing capabilities, i.e., on the order of kHz and/or MHz at the current era). The system-level design considerations for these architectures will be outlined in the following sections.

3.1.1 Heterodyne Architectures

A simplified model of a heterodyne receiver architecture [1,2] is shown in Fig. 3.1. It consists of a band-select filter, a low-noise amplifier, an image-reject filter, a mixer, a local-oscillator, and a channel select filter.

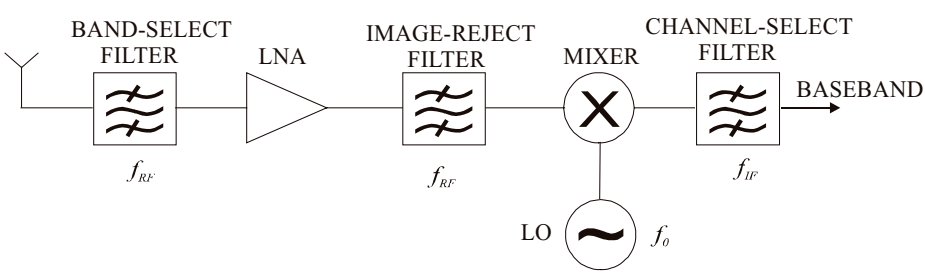


Figure 3.1: A heterodyne receiver.

The RF front-end first selects the spectrum that is allocated to users of a particular standard (band selection), and subsequently it selects the spectrum allocated to a particular user (channel selection) while suppressing interfering signals.

The transformation of the spectra traversing a part of the heterodyne receiver (Fig. 3.1) is shown in Fig. 3.2 (only positive frequencies are shown).

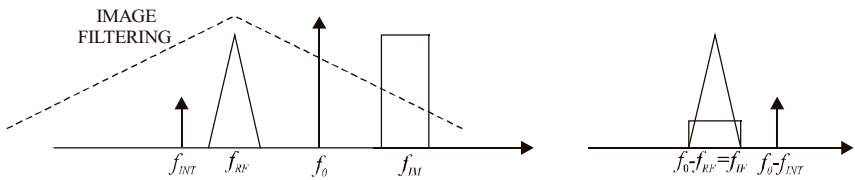


Figure 3.2: High-IF spectral conversion.

Here, f_0 stands for the local-oscillator (LO) frequency, f_{RF} the frequency of the desired signal, f_{IM} the image-signal frequency, and f_{INT} the frequency of the nearby (adjacent-channel) interferer. If $f_0<f_{RF}$, we refer to "low-side injection". Otherwise ($f_0>f_{RF}$), it is high-side injection.

A trade-off between suppression of the near and the far interferers (images) dictates the choice of the IF for the illustrated downconversion scheme (see Fig 3.2). Namely, the higher the IF is chosen, the more frequency "space" (bandwidth) there is to filter the image. In contrast, when a lower IF is chosen, only a small portion of an image signal will be suppressed, whereas nearby interferers will be easily removed because higher-order filters can be integrated more easily at low intermediate frequencies.

High-quality image-reject and channel-select filters are required for the efficient suppression of undesired signals. However, as these filters are often implemented with discrete, external components, the increased complexity (e.g., parts count) and large power consumption (50Ω matching between filters and front-end circuits) of high-IF receivers are due.

The selection/sensitivity problem, i.e., channel selection and image rejection, is somewhat alleviated in superheterodyne receivers [10] by performing the downconversion in a few steps rather than in one step (see Fig. 3.3).

A higher intermediate frequency after the first downconversion allows for better image suppression, even with moderate-Q filters. On the other hand, a lower final IF allows for better suppression of nearby interferers, having available high-Q filters at this frequency. However, more (discrete) IF filters

are necessary when more IF stages are used, which increases circuit-board and chip-packaging complexity and increases overall cost.

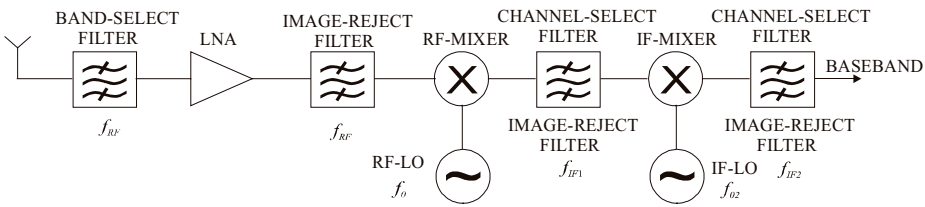


Figure 3.3: A superheterodyne receiver.

3.1.2 Homodyne Architectures

In homodyne or zero-IF receivers [3,4], an intermediate frequency of 0Hz is chosen. At the cost of degraded performance, the external bulky filters can be eliminated, obviating the need for the "power-expensive" 50Ω inter-stage matching.

An input high-frequency RF signal (f_{RF}) is downconverted to the baseband after the mixing with an oscillation signal f_0=f_{RF} in a zero-IF receiver (Fig. 3.1 with f_0=f_{RF}). The signal spectra before and after the downconversion with a single oscillation signal (e.g., *cosine*) are given in Fig. 3.4 (only positive frequencies are shown).

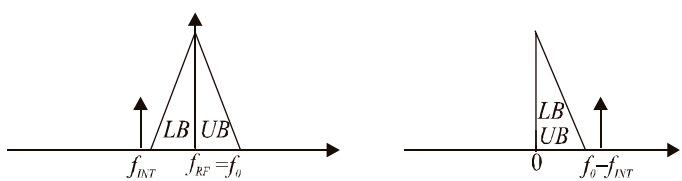


Figure 3.4: Zero-IF *s*pectral conversion.

The lower band (LB) of the spectrum of the desired signal overlaps with the upper band (UB) of the spectrum after the downconversion. In order to avoid loss of information, a zero-IF downconversion with a single LO signal requires identical LB and UB of the signal spectrum (e.g., double side-band amplitude modulated signal) [6,8].

However, frequency- and phase-modulated signals (most often employed modulation techniques in mobile communication systems [57]) don't carry the same information in the lower and the upper parts of the spectra [6,8,58]. Therefore, a certain degree of image rejection is necessary for the correct signal detection in homodyne receivers [6,8], where we can consider that the LB of the information spectrum (Fig. 3.4) is an image of the UB of the spectrum.

3.1.2.1 Image-Reject Zero-IF Architectures

In order to avoid the successive and extensive filtering found in heterodyne receivers, without compromising the selectivity and sensitivity of the receiver, other techniques of coping with the image problem have been devised. Two well-known image-reject architectures are those of Hartley [59] and Weaver [60], shown in Figs. 3.5 and 3.6, respectively.

By processing the desired signal and the image signal in a different way, both architectures reject the image signal and transfer the desired signal. Namely, by mixing the incoming signal with two quadrature-phase oscillation signals (*sine* and *cosine*) and subsequently adding the downconverted signals in quadrature (90^0 shift in Fig. 3.5a), the desired signal adds constructively whereas the image signal is cancelled.

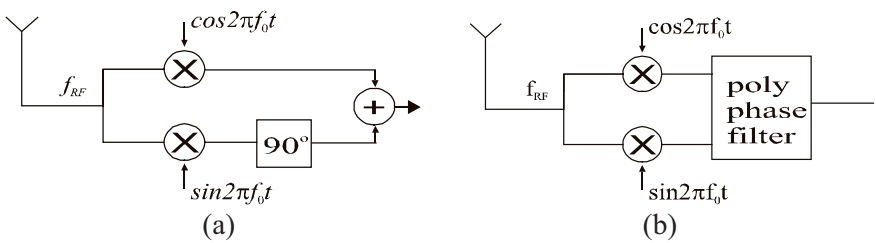


Figure 3.5: The Hartley architecture:
a) a functional description, b) a practical implementation.

An implementation of Hartley architecture is shown in Fig. 3.5b. Image suppression is achieved by means of complex polyphase filters [61,62] that can distinguish between positive and negative phase sequences, i.e., positive and negative frequencies, and accordingly transfer/suppress parts of spectra.

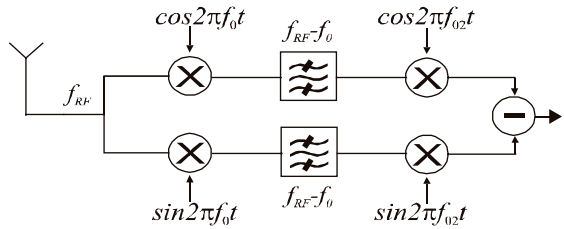


Figure 3.6: The Weaver architecture.

The image signal can also be suppressed by two consecutive downconversions with quadrature LO signals. This is shown in Fig. 3.6.

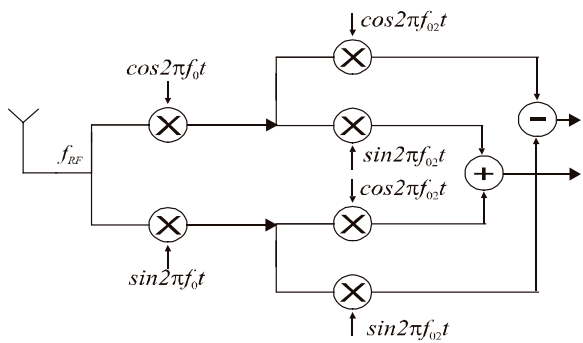


Figure 3.7: A double-quadrature downconverter.

Image suppression using a double-quadrature downconverter [6-8] is shown in Fig. 3.7. After the first quadrature downconversion, signals are again converted in quadrature to lower frequencies, allowing for the image cancellation and transfer of the desired signal.

Section 3.2 describes in detail the transformation of signals and their spectra in image-reject architectures (Figs. 3.5-3.7).

3.1.2.2 Drawbacks of Zero-IF Architectures

Although zero-IF receivers offer a higher degree of the integration as well as reduced complexity and reduced power consumption, there are also drawbacks to this architecture [44,45]. As the RF signals are directly converted to the baseband, any DC and low-frequency signals other than the desired signal cause information distortion.

Firstly, due to a finite isolation between the LO and RF ports of a mixer, a portion of the local-oscillator signal is mixed with itself, producing a large undesired DC component. The leakage of the LO signal is the result of the capacitive and substrate coupling, or for externally provided LO signals, bond-wire coupling. Even more problematic is self-mixing of LO signal radiated by the antenna and reflected back to the receiver. In such situations, a time-varying DC component is generated due to time variations between the oscillator signals. Not only does this DC component fall into the band of the desired signal, but it can also saturate the receiver through a subsequent amplification. A way to circumvent the problem of DC offset is to apply DC-free coding schemes [49] or, at circuit level, by filtering [6] and cancellation techniques [46-48].

Secondly, second- and third-order distortion products degrade the performance of zero-IF receivers, both falling into the band of the downconverted desired signal (i.e., baseband). The second-order distortion [39,63] can be due to a finite isolation between the IF and RF ports of a mixer, allowing for a feedthrough of the second-order intermodulation products. Second-order intermodulation can be alleviated with differential circuits, albeit at the expense of increased power consumption.

Flicker noise (1/f noise) is another source of hazard. Namely, the 1/f noise of devices (situated at low frequencies) can corrupt the desired signal at baseband. Effects of the 1/f noise are more influential for CMOS technologies than for bipolar technologies, due to the inherently higher 1/f-noise cut-off frequency of CMOS devices.

3.1.3 Low-If Architecture

To circumvent the detrimental effects of DC-offset and to still benefit from a high degree of integration of zero-IF topologies, the final IF can be modified to other than a zero frequency, i.e., a low IF falling into the range of the baseband signal processing capabilities [5]. However, as an image signal, e.g., a nearby interferer, can now be a lot stronger than the desired signal, receivers

with a low intermediate frequency (low-IF receivers) employ the quadrature image-reject architectures shown in Figs. 3.5-3.7.

Though low-IF receivers require more rigorous image filtering, they are relieved from problems that arise from the LO self-mixing and the second-order intermodulation distortion.

Signals and spectra undergo the same transformations in low-IF topologies as in zero-IF topologies. A detailed treatment of signals and their spectral transformations is given in Section 3.2.

3.1.4 Wireless Standards and Employed Architectures

The performance of wireless services is determined by the standardization committees [64,65]. The functionality requirements influence the choice of the receiver architecture.

An overview of wireless standards [66-74] is given in Table 3.1.

Table 3.1: Properties of various wireless standards.

standard	range(GHz)	duplex	data rate	modulation	architecture
GSM	0.935-0.96	FDD	14.4Kb/s	GMSK	zero-IF/ /high-IF/low-IF
DCS1800	1.805-1.88	FDD	14.4Kb/s	GMSK	1. zero-IF 2. low-IF/high-IF
IS-95	1.93-1.99	FDD	14.4Kb/s	QPSK, OQPSK	high-IF
WCDMA	2.11-2.17	FDD, TFD	2-10Mb/s	QPSK, 16QAM, 8PSK	zero-IF
DECT	2.4-2.48	TDD	1.152Mb/s	GFSK	1. low-IF 2. zero-IF/high-IF
Bluetooth	2.4-2.48	TDD	0.7232Mb/s	GFSK	low-IF/zero-IF
802.11b(g)	2.4-2.48	TDD	11(54)Mb/s	BPSK, QPSK (OFDM)	1. zero-IF 2. low-IF/high-IF
802.11a	5.15-5.825	TDD	54Mb/s	BPSK, QPSK	1. zero-IF 2. low-IF/high-IF
UWB	3-10	-	600Mb/s	BPSK, QPSK, OFDM	-

For example, mobile devices implementing the GSM standard employ zero-IF [26,34,37,41], low-IF [52,54] and high-IF [21] architectures. On the other hand, mobile devices that implement the WCDMA standard employ mostly a zero-IF topology [30,34,35,38,40,41] as the problem of DC-offset is relaxed due to a large channel bandwidth.

3.2 Signal and Spectral Transformations

Combining complex signal processing techniques with signal mathematical and spectral presentations is a powerful tool to both characterize and understand various phenomena related to RF front-ends [6,8]. An all-encompassing spectral analysis method in the form of a spectrum and signal transformation [9] is introduced in this section. It addresses the issue of consistent presentation of signals and their spectra in the receive path of an RF front-end. The signal spectral and mathematical transformation broadens the insight into the high-level modelling of the RF front-ends, and can be used as a useful shorthand that facilitates the analysis of RF front-end systems of any complexity.

The transformation of signals and their spectra is derived for the quadrature downconverter model shown in Fig. 3.8.

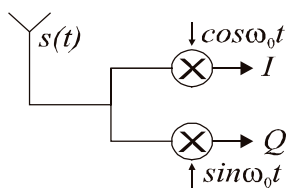


Figure 3.8: A quadrature downconverter (a simplified model).

The input modulated quadrature signal (denoted as $s(t)$) is defined by Eq. (3.1). The components $A(t)$ and $B(t)$ are the modulating signal components of the desired signal at an angular (carrier) frequency ω_{RF}, and $C(t)$ and $D(t)$ are the modulating components of the image signal with a carrier at an angular frequency ω_{IM} [58,75].

$$s(t) = A(t)\cos\omega_{RF}t - B(t)\sin\omega_{RF}t + C(t)\cos\omega_{IM}t - D(t)\sin\omega_{IM}t \quad (3.1)$$

Eq. (3.1) can be used for the representation of various modulation schemes. For example, a QPSK (digitally-modulated) signal is generated by using a carrier that is modulated by the digital signal components $A(t)$ and $B(t)$ [58]. Most of today's wireless communication systems use digital modulation schemes (e.g., QPSK, MSK, GMSK, GFSK, 16QAM) [57,58].

A visualisation of the spectrum of the signal $s(t)$ is shown in Fig. 3.9. A continuous spectrum around the corresponding central frequencies (ω_{RF} and

ω_{IM}) can be assumed [57,58,76-78] for digital modulation schemes. For the sake of clarity, we have chosen a triangle-like spectrum for the desired signal and a square-like spectrum for the image signal.

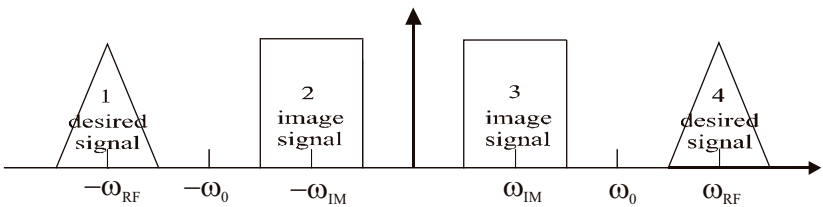


Figure 3.9: The spectra of the desired and the image signals.

The spectra of the quadrature local-oscillator signal components are shown in Fig. 3.10, where ω_0 is the oscillator angular frequency. The spectrum of the *cosine* function is referred to the real axis, and the spectrum of the orthogonal *sine* function to the imaginary axis [6] (see Eq. (3.2)).

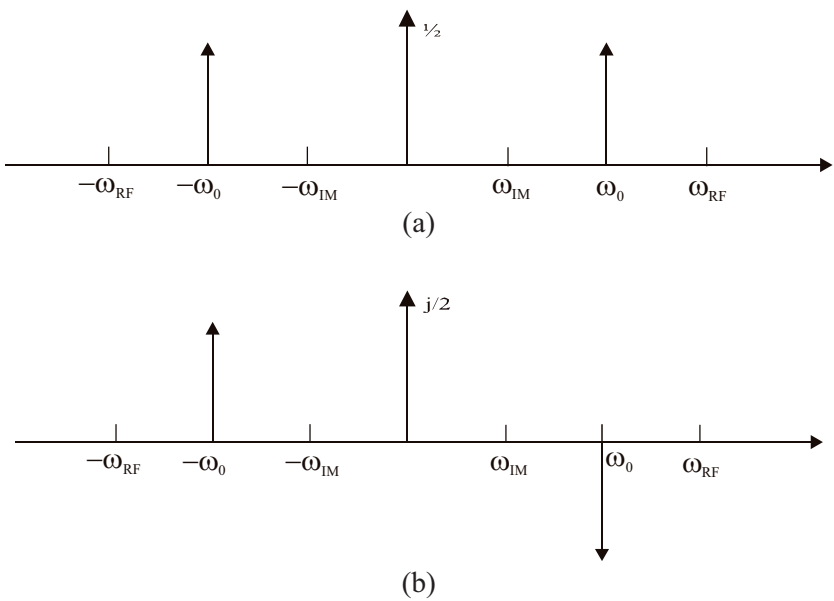


Figure 3.10: Spectra of the local oscillator signals: (a) $cos\,\omega_0 t$, (b) $sin\,\omega_0 t$.

For the sake of brevity, we will simplify the notation with $A=A(t)$, $B=B(t)$, $C=C(t)$ and $D=D(t)$. To facilitate the mathematical representation of the signal transformation, the following well-know identities (Eqs. (3.2)-(3.3)) are applied:

$$2\cos\omega_0 t = e^{j\omega_0 t} + e^{-j\omega_0 t} \qquad j2\sin\omega_0 t = e^{j\omega_0 t} - e^{-j\omega_0 t}, \tag{3.2}$$

$$R = \sqrt{A^2 + B^2}, \quad \theta = \operatorname{atan}\frac{B}{A} \qquad \mathrm{M} = \sqrt{C^2 + D^2}, \quad \psi = \operatorname{atan}\frac{D}{C}. \tag{3.3}$$

With the aid of Eq. (3.2), the complex notation [61,62] of the input signal $s(t)$ becomes

$$2s(t) = (A + jB)e^{j\omega_{RF}t} + (A - jB)e^{-j\omega_{RF}t} + (C + jD)e^{j\omega_{IM}t} + (C - jD)e^{-j\omega_{IM}t}, \tag{3.4}$$

whereas with the aid of Eq. (3.3) the complex notation transforms into

$$2s(t) = R \cdot e^{j(\omega_{RF}t+\theta)} + R \cdot e^{-j(\omega_{RF}t+\theta)} + M \cdot e^{j(\omega_{IM}t+\psi)} + M \cdot e^{-j(\omega_{IM}t+\psi)}. \tag{3.5}$$

Components $A+jB$ and $C+jD$ are often referred to as *complex envelopes* of the modulated signals [58].

In the following analysis, we will independently investigate the I and Q paths (i.e., the downconversion with the $cos\omega_O t$ and $sin\omega_O t$, respectively).

After the mixing of the input signal $s(t)$ (Eq. (3.5)) with the quadrature components of the oscillation signal (Eq. (3.2)), the downconverted in-phase (I) and quadrature-phase (Q) components become

$$2I = LowPassFilter[s(t)(e^{j\omega_0 t} + e^{-j\omega_0 t})] = R \cdot \cos(\omega_{IF}t + \theta) + M \cdot \cos(\omega_{IF} - \psi), \tag{3.6}$$

$$2Q = LowPassFilter[js(t)(e^{-j\omega_0 t} - e^{j\omega_0 t})] = -R \cdot \sin(\omega_{IF}t + \theta) + M \cdot \sin(\omega_{IF} - \psi) \tag{3.7}$$

where $\omega_{IF}=\omega_{RF}-\omega_0$ is an angular intermediate frequency.

The mixing of the LO signal and the modulated signal $s(t)$ is equivalent to a convolution of the spectral representation of the $cos\omega_0 t$ and $sin\omega_0 t$ functions (Fig. 3.10) with the spectral representation of the input signal (Fig. 3.9). The downconverted spectra of the I and Q paths obtained are given by Figs. 3.11 and 3.12.

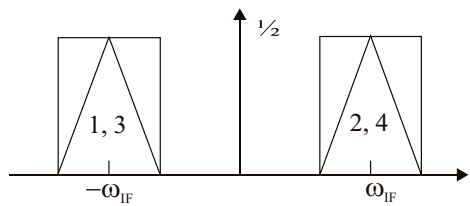


Figure 3.11: The spectrum in the I channel after low-pass filtering.

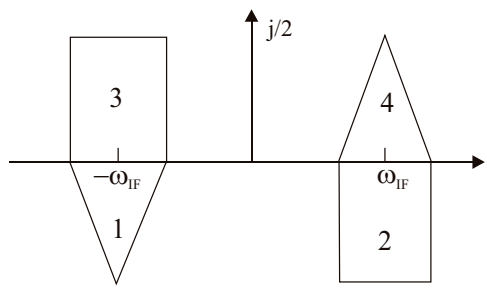


Figure 3.12: The spectrum of the Q channel after the low-pass filtering.

It is tacitly assumed that each portion of the downconversion is followed by a portion of the filtering (low pass or band-pass). This implies that only the downconverted parts of the spectra are considered.

Finally, the complex downconverted signal that consists of the orthogonal I and Q components becomes

$$2(I + jQ) = (A - jB)e^{-j\omega_{IF}t} + (C - jD)e^{j\omega_{IF}t} . \tag{3.8}$$

We will refer to Eq. (3.8) as the *signal-presentation* model. Here, the term *signal* is referred to the *mathematical representation* of the signal. According to Eq. (3.8), the downconverted signals are situated at the negative frequencies (desired signal) and the positive frequencies (image signal), respectively.

After the transformation of the *Q*-spectrum (Fig. 3.12) into the *jQ*-spectrum, which is similar to the mathematical transformation of the *Q* path, the resulting *spectral presentation* referring to the complex signal presentation *I*+*jQ* is obtained (Fig. 3.13).

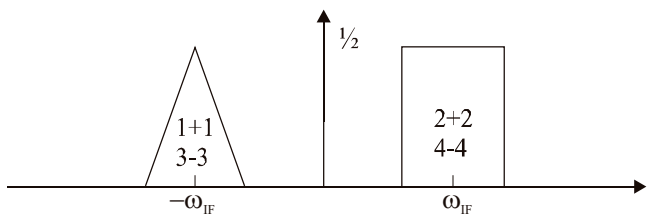


Figure 3.13: The spectrum of the downconverted signal (*I*+*jQ*).

By combining Eq. (3.8), (signal presentation) and Fig. 3.13 (spectral presentation), an explicit relationship between the spectral and the mathematical presentations of the signal downconverted, called the *spectrum-signal* (SS) *presentation*, is obtained. The SS presentation is shown in Fig. 3.14. Transformation of signals and spectra using SS presentation is referred to as the *SS transformation.*

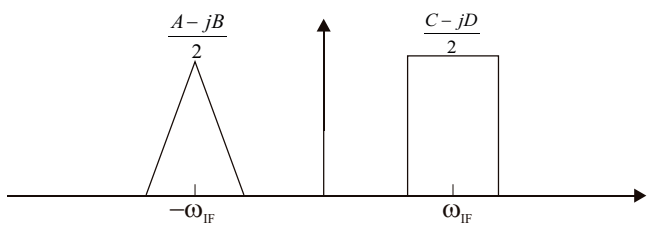


Figure 3.14: The spectrum-signal presentation.

After frequency conversion, the desired signal is situated around an angular frequency $-\omega_{IF}$ and its complex presentation has a form $(A-jB)e^{-j\omega_{IF}t}$ (the complex envelope and the carrier), where $A-jB$ is a mathematical interpretation of the desired quadrature signal entering the receiver. The complex-envelope $C-jD$ is referred to the image signal situated around the positive intermediate angular frequency, ω_{IF}.

Not surprisingly, this form is the same as that of the signal entering the receiver. The components of the signal can be still distinguished as signal orthogonality is preserved. *The desired signal is characterized by both a spectrum position* (*a central angular intermediate frequency* $-\omega_{IF}$) *and its content* (*the orthogonal modulation signals* $A(t)$ *and* $B(t)$).

To keep track of both the spectrum and the signal content, the spectrum-signal presentation of Fig. 3.14 can be applied to the analysis of receiver topologies of any complexity. SS presentation can be considered as a quadrature-downconverter "shorthand", facilitating a description of the complex RF front-end architectures. Different receiver topologies will be analyzed in the next section using the SS presentation.

3.3 Mixer-Oscillator Models

Prior to detection (demodulation), an input receive signal is downconverted to an intermediate (low) frequency in accordance with one of the schemes outlined in Section 3.1.

A high-IF receiver (Fig. 3.1) downconverts a receive signal (e.g., $s(t)$ in Eq. (3.1)) by an oscillation signal (e.g., $cos\omega_0 t$) to an IF.

On the other hand, a quadrature receiver (Figs. 3.4 and 3.6) downconverts an input signal with two oscillation signals ($sin\omega_0 t$ and $cos\omega_0 t$) that are in quadrature. The downconverted IF signal consists of two orthogonal (quadrature) components. What is more, a double-quadrature downconverter (Fig. 3.6) converts an IF quadrature signal (obtained after the first quadrature downconversion) to a baseband quadrature signal.

In order to facilitate the mathematical description of these various downconversion schemes, a complex notation is used [8]. Accordingly, the quadrature (orthogonal) signals are represented with two-dimensional vectors [9,58,75], i.e., complex variables (see Eq. (3.8)). For example, $A+jB$ stands for a quadrature-modulating signal (complex-modulating envelope), whereas $I+jQ$ is a quadrature downconverted signal.

The mixer-oscillator (MO) models are introduced in this section relying on the (complex) spectrum-signal presentation. They allow for a compact description and a high-level modelling of the receiver topologies. The MO models are classified based on the type of the signal (real or complex) before and after the mixer-oscillator (down)conversion.

- Double-real mixer-oscillator (DR-MO) converts a real input into a real output.
- Single-complex mixer-oscillator (SC-MO) converts a real (complex) input into a complex (real) output.
- Double-complex mixer-oscillator (DC-MO) converts a complex input into a complex output.

The MO models allow for a comprehensive analysis of various RF front-end topologies. Moreover, a number of receiver phenomena can be straightforwardly interpreted by means of the presented MO models, as will be shown hereafter.

3.3.1 Double-Real Mixer-Oscillator Model

A double-real mixer-oscillator (DR-MO) structure is shown in Fig. 3.15. This simple model can be found in (super)heterodyne architectures (Fig. 3.1). Common to this architecture, the desired signal and the image signal cannot be distinguished after the first downconversion without previous image filtering. This will be exemplified by using the SS transformation.

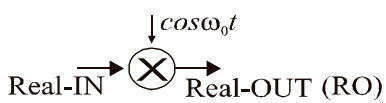


Figure 3.15: A double-real mixer-oscillator model.

If SS forms of the input signal $s(t)$ and the LO signal ($cos\omega_0 t$) are shown in Fig. 3.16, the SS form after the downconversion will be as shown in Fig. 3.17.

The DR-MO transforms a real input signal into a real output signal, accordingly performing a *real-to-real* transformation. As can be seen from

Fig. 3.17, the spectra of the desired and the image signals overlap after the downconversion, i.e., the image distorts the desired information.

This can be apprehended by referring to the content of the signal. Namely, the signal consists of the components at both the positive and the negative frequencies.

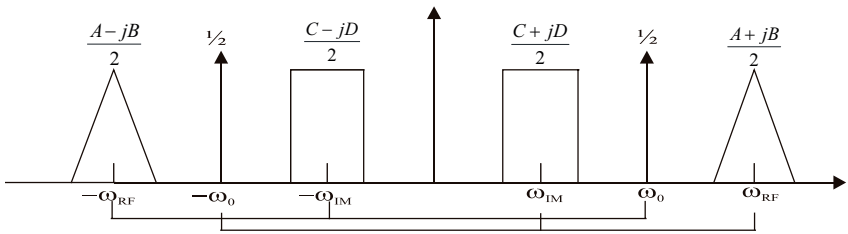


Figure 3.16: DR-MO spectrum-signal form before downconversion.

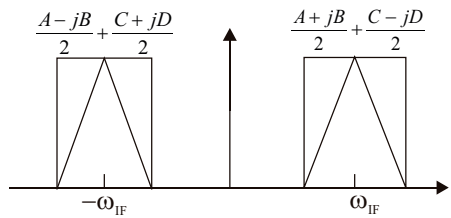


Figure 3.17: DR-MO spectrum-signal form after downconversion.

In the case of the DR-MO, the output signal component (RO in Fig. 3.15) will be

$$2\mathrm{RO} = (A - jB)e^{-j\omega_{IF}t} + (C - jD)e^{j\omega_{IF}t} + (A + jB)e^{j\omega_{IF}t} + (C + jD)e^{-j\omega_{IF}t}, \quad (3.9)$$

$$\mathrm{RO} = (A + C)\cdot\cos\omega_{IF}t - (B - D)\sin\omega_{IF}t\,. \quad (3.10)$$

Eq. (3.10) shows that the desired information indeed cannot be recovered with a single downconversion without previous image filtering (see Fig. 3.1).

Note that in the context of the transformation of the spectra, the term signal is referred to the mathematical representation of the signal. Further, the

complex representation $A+jB$ implies that the modulating signals $A(t)$ and $B(t)$ are orthogonal, thus distinguishable. On the other hand, $A+B$ refers to an non-orthogonal signal, where it can not be distinguished between the components $A(t)$ and $B(t)$. In this case, the information about these components is lost and cannot be retrieved.

The first generation Motorola cordless phone [22] is an example of a superheterodyne architecture where the DR-MO models can be employed.

3.3.2 Single-Complex Mixer-Oscillator Model

For real input and complex output signals, a real-to-complex transformation model is introduced, whereas for complex input and real output signals, a complex-to-real transformation is considered.

3.3.2.1 Real-to-Complex Transformation

A real input signal can be transformed into a complex output signal by means of two DR-MOs, as shown in Fig. 3.18a. A symbol of the single-complex mixer-oscillator model (SC-MO), i.e., quadrature downconverter, is shown in Fig. 3.18b.

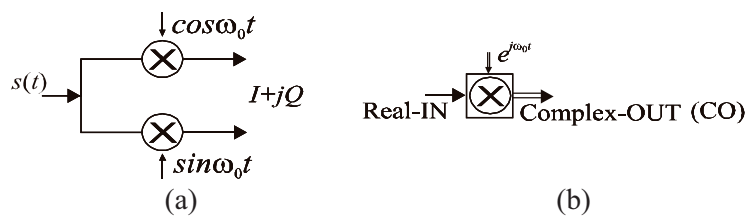


Figure 3.18: (a) Single-complex mixer-oscillator model, (b) symbol.

The "shorthand" for the quadrature downconverter is already discussed in Section 3.1 (the SS form shown in Fig. 3.14). In this section we will just briefly summarize the properties of the SC-MO model.

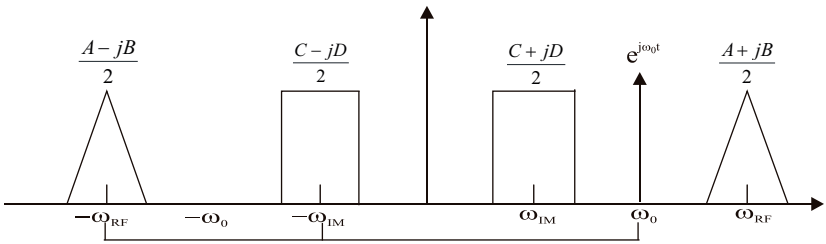


Figure 3.19: SC-MO spectrum-signal form before downconversion.

The SS form of the input signal (Fig. 3.19) is transformed by the complex LO signal $e^{-j\omega_0 t}$ [8] into the output SS form, as shown in Fig 3.20.

The *content* of the output *complex signal* (Fig. 3.20) can be found as

$$\mathrm{CO} = \frac{A - jB}{2} e^{-j\omega_{IF} t} + \frac{C - jD}{2} e^{j\omega_{IF} t} . \tag{3.11}$$

Referring to either negative or positive frequencies, the frequency independent *complex presentation of the signal content* becomes

$$\mathrm{CO}@(-\omega_{IF}) = (A - jB + C + jD)/2 . \tag{3.12}$$

This suggests that the phase sequences [62] of the desired signal (*A-jB*) and the signal of image (*C+jD*) are of different polarities. The phase sequence of the desired signal is positive, whereas that of the image signal is negative. Polyphase filters (see Fig 3.6) can distinguish between the desired and image signals after the quadrature downconversion as they discriminate between the opposite phase sequences of these signals.

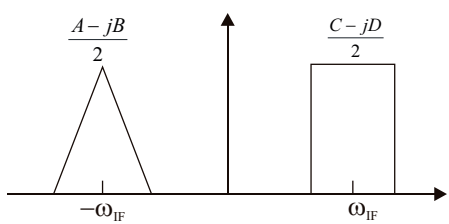


Figure 3.20: SC-MO spectrum-signal form after downconversion.

The polyphase filters are both the phase and the frequency discriminative. Fig. 3.20 and Eqs. (3.11) and (3.12) just prove that, whichever domain we refer to, the image can still be filtered out after the quadrature downconversion, i.e., it is still distinguishable. For example, the Hartley image-reject architecture (Fig. 3.5b) consists of a SC-MO topology and a polyphase filter (90º shifter) that is responsible for the final image rejection.

A zero-IF Philips receiver for paging applications [43] is an example where the SC-MO model can be used for the description of the spectral transformations.

3.3.2.2 Complex-to-Real Transformation

A complex input signal can be transformed into a real signal as shown in Fig. 3.21a. The accompanying symbol of this single-complex mixer-oscillator is shown in Fig. 3.21b. This intuitive symbol infers a transformation of a complex input signal (square in the symbol) into a real output signal (circle in the symbol). Other symbols are constructed applying the same rules.

If the complex input signal and the complex LO signal are shown in Fig. 3.22, the final downconverted signal will be as shown in Fig. 3.23. In this example, the input complex signal is situated around an angular frequency ω_{IF}, the oscillation signal at an angular frequency ω_{02} and the downconverted signal around an angular frequency ω_{IF2}.

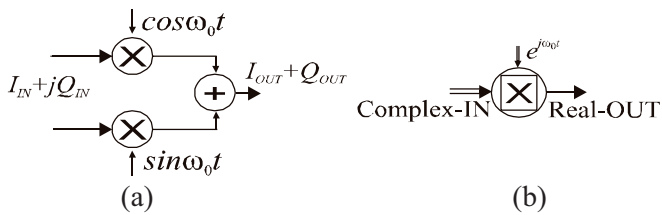


Figure 3.21: (a) Single-complex mixer-oscillator model, (b) symbol.

Note that the signal content referred to Fig. 3.19 is real, whereas the signal content shown in Fig. 3.22 is complex. Therefore, the input of a complex-to-real SC-MO model can be provided as the output of a real-to-complex SC-MO model.

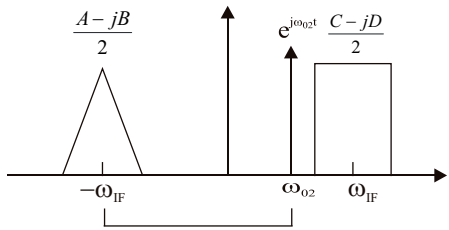


Figure 3.22: SC-MO spectrum-signal form before downconversion.

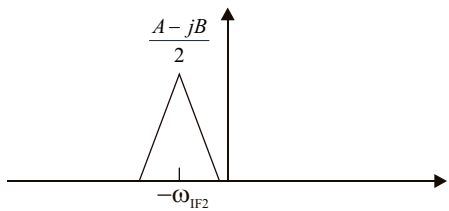


Figure 3.23: SC-MO spectrum-signal form after downconversion.

The complex-to-real SC-MO model have application in both upconversion and downconversion architectures. It can be used for a single-sideband (SSB) modulation of the input signals if the input signal I_{IN} is a Hilbert transform counterpart (90^0 phase-shifted equivalent) of the input signal Q_{IN} [58]. On the other hand, various digital modulation schemes can be obtained if I_{IN} and Q_{IN} (Fig. 3.21) are the binary signals [58]. Finally, SC-MO model of Fig. 3.21 can be employed for the final downconversion in the Weaver receiver architecture (see Fig. 3.5).

3.3.3 Double-Complex Mixer-Oscillator Model

Figure 3.24 shows a part of a double-quadrature downconverter that is shown in Fig. 3.7. This double-complex mixer-oscillator (DC-MO) topology transforms an input complex signal (e.g., obtained after a quadrature downconversion with a SC-MO) into a complex signal at the output. The symbol of the DC-MO is shown in Fig. 3.24b.

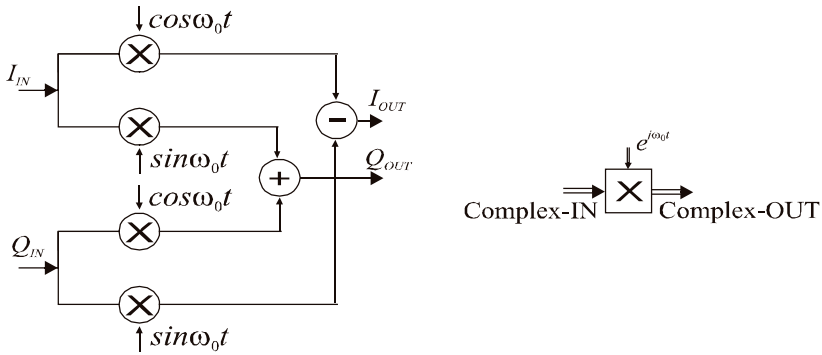


Figure 3.24: (a) Double-complex mixer-oscillator model, (b) symbol.

In this section we will introduce a "shorthand" for the DC-MO model and then examine it with the already described DR-MO and SC-MO models.

First, let us derive the relationship between the input and output complex signals. By mixing and combining I_{IN} and Q_{IN} with $cos\omega_0 t$ and $sin\omega_0 t$, as shown in Fig. 3.24, the output signals I_{OUT} and Q_{OUT} can be calculated as

$$2I_{OUT} = 2I_{IN}\cos\omega_0 - 2Q_{IN}\sin\omega_0 t = I_{IN}(e^{j\omega_0 t} + e^{-j\omega_0 t}) + jQ_{IN}(e^{j\omega_0 t} - e^{-j\omega_0 t}), \tag{3.13}$$

$$2Q_{OUT} = 2I_{IN}\sin\omega_0 + 2Q_{IN}\cos\omega_0 t = -jI_{IN}(e^{j\omega_0 t} - e^{-j\omega_0 t}) + Q_{IN}(e^{j\omega_0 t} + e^{-j\omega_0 t}), \tag{3.14}$$

$$I_{OUT} + jQ_{OUT} = (I_{IN} + jQ_{IN})e^{j\omega_0 t}. \tag{3.15}$$

As suggested by Eq. (3.15) the two quadrature LO signals (Fig. 3.24) can be presented with the complex LO signal $e^{j\omega_0 t}$ [8]. This further implies that the same transformation rules can be applied for both the SC-MO (real-to-complex; Fig. 3.22) and the DC-MO models. Fig. 3.25a shows the spectrum-signal form of the complex input signal and the complex LO signal, where it is assumed that the first downconversion has already been done with a quadrature downconverter (Section 3.3.2.1 and Fig. 3.20). The SS form referring to the complex downconverted signal is now simply obtained as shown in Fig. 3.25b.

The SS presentation "shorthand" for the DC-MO model will be verified through an all-encompassing spectral analysis of a double-quadrature

downconverter, shown in Fig. 3.26a, by applying the SS transformation rules of the DR-MO and SC-MO models.

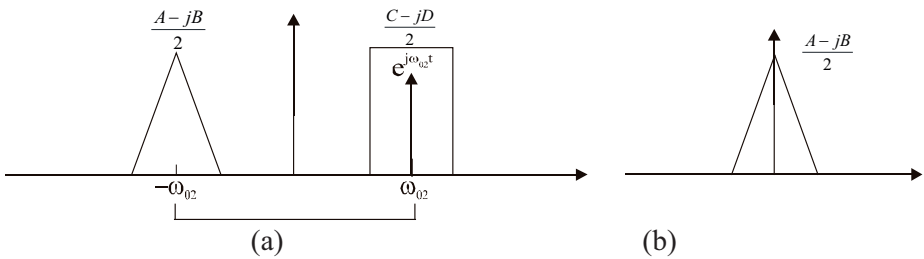


Figure 3.25: DC-MO SS form:
a) after the quadrature conversion, b) after the double-quadrature conversion.

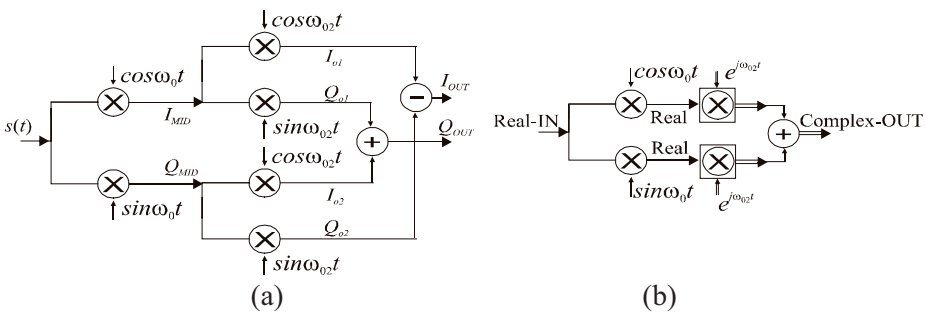


Figure 3.26: (a) Double-quadrature downconverter, (b) MO model.

A double-quadrature downconverter can be equivalently represented with two DR-MOs and two SC-MOs, as shown in Fig. 3.26b. The spectrum-signal form of the input signal $s(t)$ and the LO signal is shown in Figs. 3.9 and 3.10. Applying the transformation rules of the DR-MO model, the SS form of the real signals I_{MID} and Q_{MID} is obtained (Figs. 3.27a and 3.27b).

Applying the SS transformation rules of the SC-MO (see Figs. 3.19 and 3.20) to the SS form of Fig. 3.27 results into the complex signals $C_{OUT1}=I_{O1}+jQ_{O1}$ and $C_{OUT2}=I_{O2}+jQ_{O2}$, shown in Figs. 3.28a and 3.28b, and the output complex signal $I_{OUT}+jQ_{OUT}=C_{OUT1}+jC_{OUT2}$, shown in Fig. 3.29.

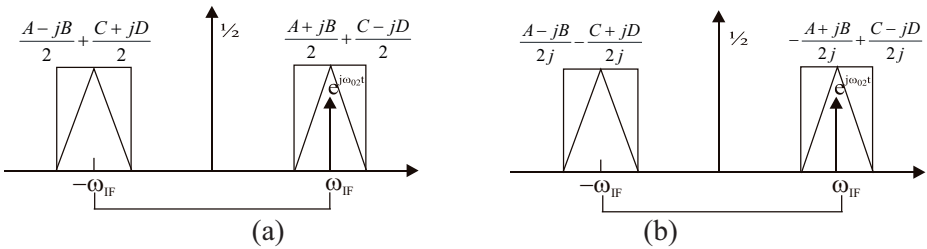


Figure 3.27: Spectrum-signal form after the first downconversion
a) I_{MID} path, b) Q_{MID} path.

Expectedly, the image is suppressed after the final downconversion. Furthermore, the equality of the resulting spectra of Figs. 3.29 and 3.25b proves the validity of the proposed spectrum-signal form of the DC-MO model.

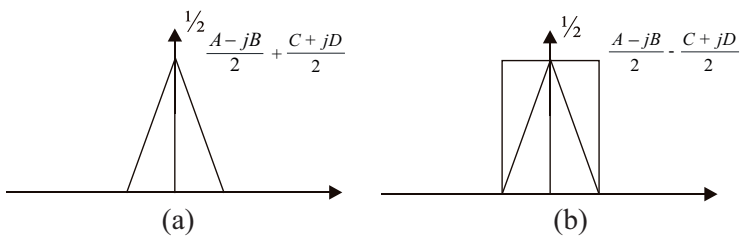


Figure 3.28: Spectrum-signal form after second downconversion
(a) $C_{OUT1}=I_{O1}+jQ_{O1}$ (b) $C_{OUT2}=I_{O2}+jQ_{O2}$.

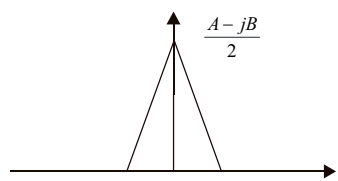


Figure 3.29: $I_{OUT}+jQ_{OUT}$.

With the advantage of the DC-MO model (Fig. 3.25) we can manipulate content and spectra of signals in a simpler manner compared to the transformations shown in Figs. 3.27, 3.28 and 3.29, or even more complicated analysis found in [6,7].

3.4 Image-Rejection Ratio Model

The spectrum-signal presentation models allow for a straightforward derivation of various RF receiver performance parameters. Accordingly, this section elaborates on the image-rejection-ratio (IRR) of a quadrature downconverter [79] by means of MO models.

First, let us denote ε and φ as the amplitude and the phase mismatch of the oscillation signal, as shown in Fig. 3.30a.

Taking mismatch into account, the complex LO signal presentation becomes

$$(1+\varepsilon)\cos(\omega_0 t+\varphi)+j\sin\omega_0 t=[X_1(\varepsilon,\varphi)e^{j\omega_0 t}+X_2(\varepsilon,\varphi)e^{-j\omega_0 t}], \quad (3.16)$$

where X_1 and X_2 represent the desired and undesired (parasitic) complex LO signals, given by Eqs. (3.17) and (3.18), respectively.

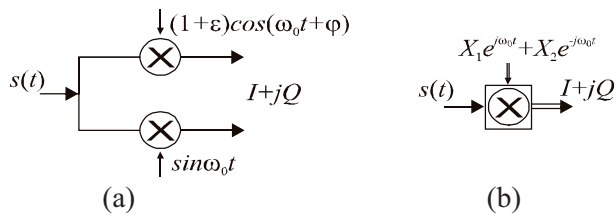


Figure 3.30: (a) Quadrature downconverter, (b) IRR model.

$$X_1(\varepsilon,\varphi)=(1+\varepsilon)e^{j\varphi}+1 \quad (3.17)$$

$$X_2(\varepsilon,\varphi)=(1+\varepsilon)e^{-j\varphi}-1 \quad (3.18)$$

Without loss of generality, the constants ½ and 2 that originate from the mixing with the LO signal are omitted, as we are only interested in the form of the signals as well as the position of their spectra, which is not affected using this simplification. Also, this does not affect the ratio of the signal quantities.

The IRR model is shown in Fig. 3.30b with the aid of Eq. (3.16) and a SC-MO model. We will determine the IRR by using a strictly mathematical interpretation of signals. Then, a method that relies on the spectrum-signal

presentation and transformation will be described proving to be simpler and more intuitive.

By mixing the input signal $s(t)$ (Eq. (3.1)) and the LO signal (Eq. (3.16)) the low-filtered version of the output signal becomes

$$\begin{aligned} I + jQ \propto & RX_1(\varepsilon,\varphi)e^{-j(\omega_{IF}t+\theta)} + MX_2(\varepsilon,\varphi)e^{-j(\omega_{IF}t-\psi)} + \\ & + RX_2(\varepsilon,\varphi)e^{j(\omega_{IF}t+\theta)} + MX_1(\varepsilon,\varphi)e^{j(\omega_{IF}t-\psi)} \end{aligned}, \tag{3.19}$$

where R and M are the magnitudes of the desired and the mirror signals, respectively (see Eq. (3.3)). The ratio of the power of the image and desired signals at either positive or negative frequencies can be now calculated as

$$IRR = \left| \frac{X_2(\varepsilon,\varphi)e^{-j(\omega_{IF}t-\psi)}}{X_1(\varepsilon,\varphi)e^{-j(\omega_{IF}t+\theta)}} \right|^2 = \left| \frac{-1+(1+\varepsilon)e^{-j\varphi}}{1+(1+\varepsilon)e^{j\varphi}} \right|^2, \tag{3.20}$$

$$IRR = \frac{1\text{-}2(1+\varepsilon)\cos\varphi + (1+\varepsilon)^2}{1+2(1+\varepsilon)\cos\varphi + (1+\varepsilon)^2}. \tag{3.21}$$

Not surprisingly, the well-known expression for the *IRR* [6] is obtained.

Let us now examine the same phenomenon by using the spectrum-signal analysis method described in the previous sections.

The SS forms of the input signal before the conversion and the SS form of the complex LO signal are shown in Fig. 3.31. The SS form of the downconverted signal is depicted by Fig. 3.32. From Fig. 3.32 it can be straightforwardly determined to what extent the image signal affects the desired signal. Referring to an angular frequency $-\omega_{IF}$, the *IRR* can readily be calculated by Eq. (3.22).

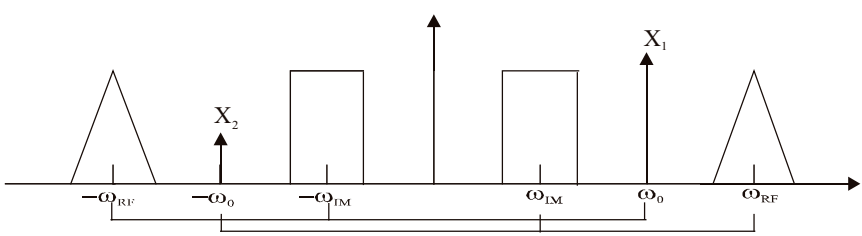


Figure 3.31: Spectrum-signal form before downconversion.

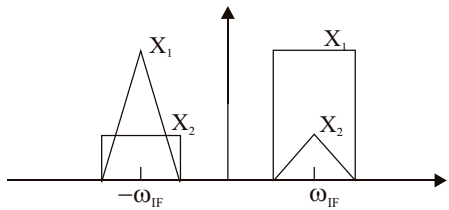


Figure 3.32: Spectrum-signal form after downconversion.

$$IRR = \left| \frac{X_2(\varepsilon,\varphi)}{X_1(\varepsilon,\varphi)} \right|^2 \tag{3.22}$$

Calculation of the IRR without the model proposed would be complicated if we consider the deviation in both quadrature LO signals, viz., the amplitude and the phase deviation (ε_1 and φ_1) of the *I*-phase and the amplitude and the phase deviation (ε_2 and φ_2) of the *Q*-phase components. However, by means of the functions X_1 and X_2 of the form

$$X_1(\varepsilon_1,\varphi_1,\varepsilon_2,\varphi_2) = (1+\varepsilon_1)e^{j\varphi_1} + (1+\varepsilon_2)e^{j\varphi_2}, \tag{3.23}$$

$$X_2(\varepsilon_1,\varphi_1,\varepsilon_2,\varphi_2) = (1+\varepsilon_1)e^{-j\varphi_1} - (1+\varepsilon_2)e^{-j\varphi_2}, \tag{3.24}$$

the *IRR* can be easily determined from Fig. 3.32 and Eq. (3.22).

The IRR model of Fig. 3.32 allows for efficient calculation of IRR in various quadrature topologies.

3.5 IRR Model of Double-Quadrature Downconverters

All the properties of the spectrum-signal presentation model can be examined with the image-reject double-quadrature downconversion architecture, shown in Fig. 3.26a (standard form) and Fig. 3.26b (mixer-oscillator model).

We will focus only on the derivation of the IRR by using the SS presentation.

Using the introduced mixer-oscillator models, a rather complex double-quadrature downconverter structure, Fig. 3.33a, especially for the calculation of IRR, reduces to the topology shown in Fig. 3.33b (Weaver topology). The

obtained IRR model consists of a real-to-complex SC-MO and a complex-to-real SC-MO.

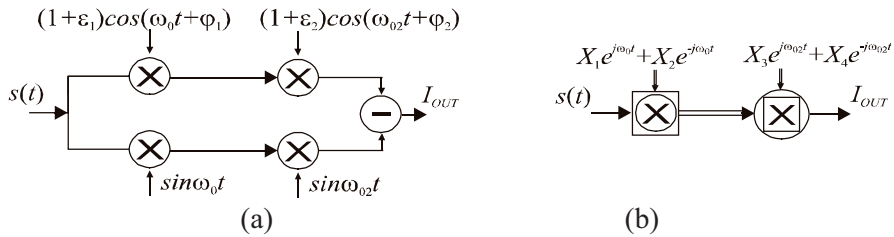


Figure 3.33: (a) Double-quadrature downconverter, (b) IRR model.

The result of the first downconversion with a SC-MO is already shown in Figs. 3.31 and 3.32. Final downconversion to the baseband is done with the second complex LO signal (X_3 and X_4), as shown in Figs. 3.34 and 3.35.

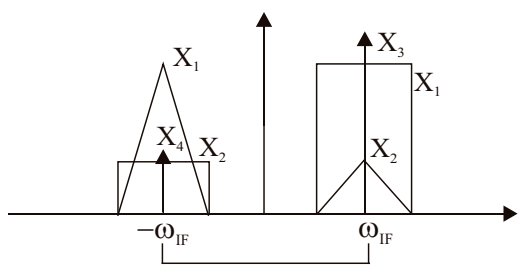


Figure 3.34: Spectrum-signal form before the second downconversion.

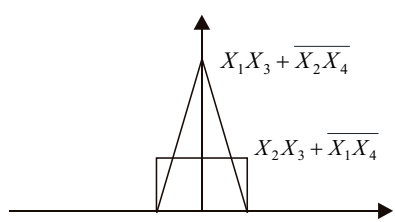


Figure 3.35: Spectrum-signal form after the second downconversion.

If the first LO signal is given by Eqs. (3.25)-(3.27), and the second LO signal by Eq. (3.28)-(3.30),

$$(1+\varepsilon_1)\cos(\omega_0 t+\varphi_1)+j\sin\omega_0 t=[X_1(\varepsilon_1,\varphi_1)e^{j\omega_0 t}+X_2(\varepsilon_1,\varphi_1)e^{-j\omega_0 t}], \tag{3.25}$$

$$X_1(\varepsilon_1,\varphi_1)=(1+\varepsilon_1)e^{j\varphi_1}+1, \tag{3.26}$$

$$X_2(\varepsilon_1,\varphi_1)=(1+\varepsilon_1)e^{-j\varphi_1}-1, \tag{3.27}$$

$$(1+\varepsilon_2)\cos(\omega_{02} t+\varphi_2)+j\sin\omega_{02} t=[X_3(\varepsilon_2,\varphi_2)e^{j\omega_{02} t}+X_4(\varepsilon_2,\varphi_2)e^{-j\omega_{02} t}], \tag{3.28}$$

$$X_3(\varepsilon_2,\varphi_2)=(1+\varepsilon_2)e^{j\varphi_2}+1, \tag{3.29}$$

$$X_4(\varepsilon_2,\varphi_2)=(1+\varepsilon_2)e^{-j\varphi_2}-1, \tag{3.30}$$

the resulting *IRR* can be calculated from the SS from of the finally downconverted signal, shown in Fig. 3.35. This is given by Eqs. (3.31) and (3.32).

$$IRR=\left|\frac{X_2X_3+\overline{X_1X_4}}{X_1X_3+\overline{X_2X_4}}\right|^2 \tag{3.31}$$

$$IRR=\frac{1\text{-}2(1+\varepsilon_1)(1+\varepsilon_2)\cos(\varphi_1-\varphi_2)+(1+\varepsilon_1)^2(1+\varepsilon_2)^2}{1+2(1+\varepsilon_1)(1+\varepsilon_2)\cos(\varphi_1+\varphi_2)+(1+\varepsilon_1)^2(1+\varepsilon_2)^2} \tag{3.32}$$

As stated in Section 3.3.2.1, the components that originate from the opposite frequencies are added in complement (Fig. 3.35) in Eq. (3.31). This result is in accordance with [6], which proves the validity of the application of the mixer-oscillator models for estimation of IRR.

The SS presentation, MO models, and IRR model are useful tools ("shorthands") for the analysis of signals and their spectra in receiver topologies of any complexity.

3.6 Conclusions

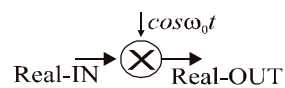
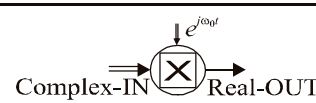
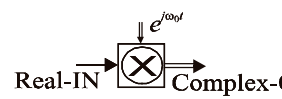
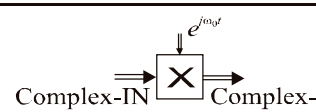
Combining complex signal processing techniques with signal and spectral presentations is a powerful tool to both characterize and understand various phenomena related to RF front-ends.

An all-encompassing spectral analysis method called the spectrum-signal transformation has been introduced in this chapter. It addresses the issue of consistent presentation of transformation of signals and their spectra in the receive path of an RF front-end.

The mixer-oscillator models proposed in this chapter are based on the spectrum-signal formulation and offer a comprehensive interpretation of how signals and their spectra are transformed from an RF range at the input up to a low-frequency range at the output of different receiver topologies. Table 3.2 summarizes the classification of the mixer-oscillator models introduced in this chapter.

The mixer-oscillator models allow for examination of various RF system phenomena. The application of these models to the calculation of the image-rejection ratio in quadrature downconverters is an example of their utility.

Table 3.2: Mixer-oscillator models.

DOUBLE-REAL MO-MODEL	
SINGLE-COMPLEX MO-MODEL	 
DOUBLE-COMPLEX MO-MODEL	

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Chapter 4

SELECTION OF PERFORMANCE PARAMETERS FOR RECEIVER CIRCUITS

A rigorous procedure to select specifications for individual blocks in a radio receiver system has not yet been established: choice of an optimal receiver specification frequently relies on the judgment of an experienced designer. In this chapter, we introduce methods for selection of performance parameters for receiver circuits.

A usual way to optimize receiver performance is to design each receiver circuit independently for minimum noise figure and good linearity. However, this approach requires more power than necessary, as a circuit optimized for good noise and linearity consumes more power than a circuit with moderate but satisfactory performance.

In this chapter, we introduce performance selection criteria, resulting in procedures for assigning the specifications to the receiver circuits. Due to complexity of a multi-objective performance selection problem (i.e., complex relationships between noise, linearity and power consumption between a receiver and its circuits), we bound the discussion to noise and linearity performance, and then relate the selection procedures developed to power consumption.

A method to allocate each performance parameter to receiver *blocks* is introduced first, resulting in equal performance (noise, linearity) contributions of all circuits to the system (noise and linearity) performance. In this case we refer to equilibrium criterion.

On the other hand, noise figure (*NF*) and third-order input-intercept point (*IIP*3) optimization procedures are not independent, as both the noise and linearity performance of a receiver depend on the gain of its circuits. By optimizing the *system* performance with respect to the ratio $(F\text{-}1)/P_{IIP3}$ (the relative noise power over the third-order power intercept point), a mutually dependent noise and linearity allocation

procedure is developed in this chapter, resulting in the noise and linearity requirements satisfied. We name this optimality criterion.

Furthermore, the assignment of the specifications to the receiver circuits for the equal *system* noise and linearity margins with respect to the requirements is proposed. In this case we refer to equality criterion.

This chapter is organized as follows. Some system considerations are discussed in the next section. Section 4.2 describes a procedure for selecting individual noise and linearity specifications for receiver circuits. The allocation of the mutually dependent noise and linearity performance parameters to receiver circuits is outlined in Section 4.3, by determining the condition for the optimal dynamic range of a receiver. The criterion for equal contribution of the noise and linearity performance to the receiver dynamic range is then derived. Section 4.4 compares the performance selection criteria proposed. The chapter continuous with a discussion on the "cost" (i.e., power consumption) of the introduced design criteria. Finally, some design trade-offs between performance parameters of an RF circuit are described by means of a K-rail diagram.

4.1 System Considerations

For the sake of simplicity, we will refer to a receiver as a system consisting of a low-noise amplifier (LNA), a mixer, and baseband (BB) circuitry (with channel selection filtering included), as shown in Fig. 4.1.

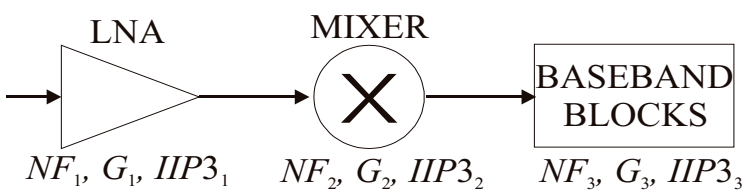

Figure 4.1: A simplified model of a receiver.

F, P_{IIP3} and *g* are the noise factor, input-referred third-order power intercept point, and power gain of the corresponding blocks. Their logarithmic equivalents are indicated in Fig. 1: *G* is power gain in dB, *NF* noise figure and *IIP*3 third-order input intercept point. This model can be extended for any other block, by considering it as a part of the blocks shown (e.g., an image-reject filter between the LNA and mixer can be included into either LNA or mixer by modifying their performance parameters).

Typical *G*, *NF*, and *IIP*3 values for the receiver blocks are shown in Table I [1,2,3].

Table 4.1: Typical performance parameters of the receiver blocks.

	T/R switch	**RF filter**	**duplexer**	**LNA**	**mixer**	**BB**
G [dB]	-1	-2	-3	10–20	5–15	40–60
NF [dB]	1	2	3	1–3	10–20	20–10
*IIP*3 [dBm]	100	100	100	-5–2	-5–5	20–10

The blocks preceding the LNA (between LNA and antenna), viz., a transmit/receive (T/R) switch, radio frequency preselect filter and duplexer, are not considered in the analysis (and Fig. 1) as the noise and linearity parameters of these circuits are known prior to integration of the receiver circuits and the allocation of the specifications (e.g., see Table 1). The specifications referred to the input of the LNA implicitly take into account the specifications of these blocks by adding/subtracting them from those referred to the antenna.

Design of receiver circuits imposes trade-offs between gain, noise, linearity, and power consumption. Goals of this multi-objective design problem are:

- provision of a sufficiently large gain in order to minimize noise contributions of the receiver circuits, while ensuring a sufficient signal-to-noise ratio at input of an analogue-to-digital converter;

- provision of a sufficiently small gain in order not to degrade linearity of a system (i.e., to avoid saturation and clipping);

- operation at a power-consumption level that ensures long time between battery charge cycles in a mobile device.

Technology constraints affect the design space as well, but considering them as already given to a circuit designer, we will not use them in the optimization analysis.

The total noise factor F referred to the input of a cascade of blocks (see Fig. 4.1) is given for convenience by Eq. (4.1) ([4], see Chapter 2),

$$F-1=F_1-1+\frac{F_2-1}{g_1}+\frac{F_3-1}{g_1 g_2}+\ldots, \tag{4.1}$$

where g_i and F_i are the power gains and noise factors of the corresponding stages. Similarly, the total third-order input-referred intercept power point of an n-stage cascaded network equals [5,6]

$$\frac{1}{P_{IIP3}}=\frac{1}{P_{IIP3,1}}+\frac{g_1}{P_{IIP3,2}}+\frac{g_1 g_2}{P_{IIP3,3}}+\ldots, \tag{4.2}$$

where $P_{IIP3,i}$ are the third-order input-referred intercept power points of the receiver blocks.

The selection of g_i, F_i and $P_{IIP3,i}$ for each receiver stage is usually done by extensively exercising Eqs. (4.1) and (4.2) for a large number of (g_i,F_i,$P_{IIP3,i}$) combinations until all the requirements are satisfied [7,8]. The performance objective is often consciously directed towards the a priori known capabilities of the employed technology (e.g., an LNA NF<2dB as a starting point). Another approach is (over)designing of the receiver circuits, i.e., optimizing each circuit independently for the good noise figure, linearity and gain [9], with penalties in power consumption.

In the following sections alternative criteria for the selection of performance parameters are proposed:

- (Section 4.2) by making equal the (input-referred) contributions of the noise and linearity performance parameters of each receiver block (the equilibrium criterion);

- (Section 4.3.1) by optimizing the system noise and linearity performance via the input referred (F-1)/P_{IIP3} ratio (the optimality criterion);

- (Section 4.3.2) by making equal the system noise and linearity performance margins with respect to the requirements (the equality criterion).

4.2 Independent Selection of *NF* and *IIP*3 Specifications

A procedure for the allocation of each performance parameter for the receiver sub-blocks is discussed in this section [10]. We introduce the equilibrium criterion by making the contributions of the noise and linearity parameters of receiver circuits equal.

We can apply the same analysis procedure to calculate the noise and linearity properties of a system using cascaded formulations of Eqs. (4.1) and (4.2). Therefore, we will first consider the (inverse) input-referred third-order power intercept point $1/P_{IIP3}$, and then apply the result obtained to the relative noise power F-1 (ratio of circuit input-referred noise power and source noise power).

From Eq. (4.2), the inverse of a third-order power intercept point of a receiver (see Fig. 4.1) can also be written as

$$P_{IIP3}^{-1} = P_{IIP3,1}^{-1} + P_{IIP3,2-1}^{-1} + P_{IIP3,3-1}^{-1} = \alpha \cdot P_{IIP3,E}^{-1} + \beta \cdot P_{IIP3,E}^{-1} + \gamma \cdot P_{IIP3,E}^{-1}. \quad (4.3)$$

Here, $P_{IIP3,1}^{-1}$, $P_{IIP3,2-1}^{-1}$, and $P_{IIP3,3-1}^{-1}$ refer to the (inverse) linearity contributions of each block in the receive chain with respect to the input of the receiver. $P_{IIP3,E}^{-1}$ is the linearity *equilibrium point* and the coefficients α, β and γ represent the linearity deviations of the LNA, mixer and baseband circuitry from it. The equilibrium $P_{IIP3,E}^{-1}$ refers to a third-order power intercept point of each receiver block referred to the input of the receiver when the block linearity contributions are equal. The equilibrium is calculated from Eq. (4.3), when $\alpha=\beta=\gamma=1$, as

$$P_{IIP3,E}^{-1} = P_{IIP3,D}^{-1} / n, \quad (4.4)$$

or

$$IIP3_E = IIP3_D + 10\log\ n. \quad (4.5)$$

$P_{IIP3,D}$ and $IIP3_D$ are the desired (which we also refer to as the required) performance parameters of the complete receiver, and n is the number of the considered receiver circuits (n=3 in Eq. (4.3)).

When circuit linearity parameters deviate from the equilibrium point, in order to satisfy the system specifications required ($IIP3_D$), the following condition is derived from Eq. (4.3) (for $IIP3$=$IIP3_D$).

$$10^{\frac{-IIP3_D}{10}} = 10^{\frac{10\log n - IIP3_E}{10}} = 10^{\frac{A-IIP3_1}{10}} + 10^{\frac{B-IIP3_2}{10}} + 10^{\frac{C-IIP3_3}{10}} \tag{4.6}$$

Here, A=10logα, B=10logβ and C=10logγ (in dB). For a three-block system, Eq. (4.6) can be transformed into Eq. (4.7).

$$B = 10\log\left(3 - 10^{A/10} - 10^{C/10}\right) \tag{4.7}$$

The relationship between the deviations A and B is graphically shown in Fig. 4.2a, C being the third parameter. A linear counterpart of Eq. (4.7) is simply given by Eq. (4.8),

$$\alpha + \beta + \gamma = 3\,, \tag{4.8}$$

and Fig. 4.2b. Even though rather simple, Eqs. (4.7) and (4.8), and Fig. 4.2 determine a complete design space for receiver circuits (a shaded area in Fig. 4.2). More insight and knowledge about the performance of the receiver and its blocks can be gained from Eqs. (4.3), (4.4), and (4.8) than from Eq. (4.2), as will be demonstrated hereafter.

The circuits linearity parameters depend equally on α (A) and β (B) (see Eq. (4.3)); deviation A depends on deviation B in the same way deviation B depends on A. From Eq. (4.9),

$$\frac{\partial A}{\partial B}\Big|_{C=const} = \frac{\partial B}{\partial A}\Big|_{C=const}\,, \tag{4.9}$$

and with the aid of Eq. (4.7), A and B are in balance for

$$A = B\,, \tag{4.10}$$

as expected from an equiproportional relationship between these variables. For this condition, the *slopes* of both deviation dependences are the same: A and B balance each other at this point, as can be seen from Fig. 4.2. Having taken $\gamma(C)$ as a parameter, we distinguish between the two extreme cases, γ=0 (C–>-∞) and γ=1 (C=0).

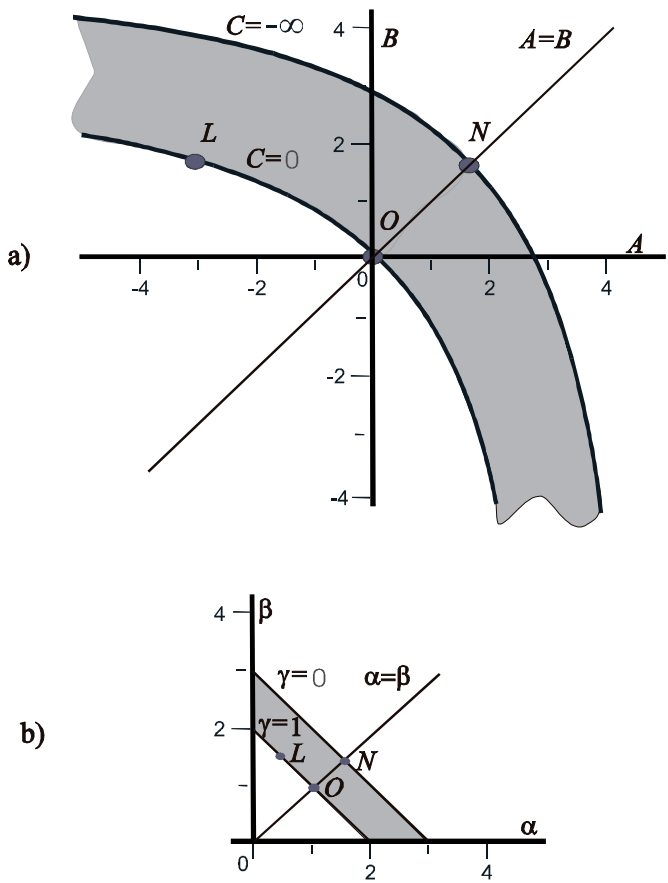

Figure 4.2: Deviation of the linearity (noise) performance of a mixer $\beta(B)$ with respect to deviation of the linearity (noise) of an LNA $\alpha(A)$; deviation of baseband circuitry $\gamma(C)$ taken as a parameter.

First, if C=0 (i.e., the linearity performance of the baseband block is in the equilibrium), Eq. (4.10) reads A=B=0 (point O in Fig. 4.2), being the already defined equilibrium point.

In case of a negligible contribution of the baseband circuitry to the equivalent input linearity of the receiver (C–>-∞), Eq. (4.7) results in A=B=1.76, being the equilibrium for a two-block system (point N in Fig. 4.2). In other words, n=3, C–>-∞ and A=B=1.76 coincides with n=2 and A=B=0.

The result of Eq. (4.10) can also be justified as follows. A negative deviation from the equilibrium point (A<0, B<0, and/or C<0) results in an improvement of a block performance that is always smaller than an improvement in the overall receiver performance. For example, improving the linearity contribution of an LNA by 3dB (A=–3dB; point L) with respect to the equilibrium design point relaxes the linearity requirement of a mixer for B=1.76dB (if C=0). This results in 3dB–1.76dB=1.24dB over-design of the linearity performance required for the mixer, given the same overall required $IIP3$ of the receiver. At this level of discussion, we assume the same cost (e.g., power consumption) of the LNA and mixer performance. On the other hand, degrading the linearity of an LNA for A=3dB would require a theoretically infinite improvement in linearity of the mixer, having C=0. In a more extreme case, where the LNA is designed much better than required (i.e., A<<0), the corresponding performance parameter B of the mixer is relaxed only slightly (i.e., B<3).

The rather common practice of referring to a two-block front-end, and taking into account the linearity parameters of the LNA and mixer only (i.e., C–>-∞), would result in the 1.76dB relaxed third-order input intercept points of the circuits (point N). This under-estimation could in the end lead to a design not satisfying the specifications of a complete receiver chain, i.e., an LNA-mixer-baseband circuit configuration. It is neither a two- nor a three-block system that has be considered, but a system with as many blocks as preceding a conversion into digital domain. That is to say, at least a system shown in Fig. 4.1 has to be used, with each of the three blocks encompassing other neighbouring sub-blocks (e.g., a baseband filter and amplifier could be merged into a single baseband block).

Finally, given Eqs. (4.3) and (4.7), the third-order input-intercept points of the receiver circuits under consideration can be calculated as

$$IIP3_1 = IIP3_E - A_{IIP3}, \tag{4.11}$$

$$IIP3_2 = IIP3_E + G_1 - B_{IIP3}\,, \tag{4.12}$$

$$IIP3_3 = IIP3_E + G_1 + G_2 - C_{IIP3}\,. \tag{4.13}$$

The same set of expressions and figures (Eqs. (4.3-4.13) and Fig. 4.2) result for the relative noise power (ratio of the noise and source power; *F*-1) of the receiver and its circuits. Note that when denormalized for source noise power, *F*-1 turns into input noise power of a block. Introducing variable *F*' for relative noise power *F*-1, Eq. (4.1) can be transformed into Eq. (4.14). It has the same form as Eq. (4.3).

$$F' = F_1' + F_{2-1}' + F_{3-1}' = \alpha \cdot F_E' + \beta \cdot F_E' + \gamma \cdot F_E' \tag{4.14}$$

F_1', F_2', and F_3' stand for noise contributions of each block in the receive chain with respect to the input of the receiver, and F_E' is for the *noise* equilibrium point defined in dB as

$$NF_E' = NF_D' - 10\log\, n = 10\log(F_E - 1) = 10\log(F_D - 1) - 10\log\, n\,. \tag{4.15}$$

Index $_D$ always refers to the desired performance. The analysis of noise performance follows the same line as the linearity analysis, thus, Eqs. (4.4-4.13) and Fig. 4.2 could be all used by just referring to the parameter *F*'=*F*-1, instead. This in the end results in the relative noise figure of the receiver circuits, as given by Eqs. (4.16-4.18).

$$10\log(F_1 - 1) = 10\log(F_E - 1) + A_{NF'} \tag{4.16}$$

$$10\log(F_2 - 1) = 10\log(F_E - 1) + G_1 + B_{NF'} \tag{4.17}$$

$$10\log(F_3 - 1) = 10\log(F_E - 1) + G_1 + G_2 + C_{NF'} \tag{4.18}$$

Indices *NF'* and *IIP*3 refer to the deviations from the noise and linearity equilibrium points. Eqs. (4.7-4.18) establish the relationship between the linearity/noise parameters of the receiver circuits, while satisfying the system performance required.

Whether the equilibrium design point is also power efficient or realizable depends on the power budget, technology and circuit topology chosen. Only

at the circuit level, can the relationship between the gain, linearity, noise, and power consumption be explicitly determined. At this point, we just conclude that by improving receiver circuits specifications by more than a few dB from the equilibrium point (*O* and *N* in Fig. 4.2), the requirements for the other circuits in the receive chain don't relax much (e.g., A–>-∞ and C=0 result in B<3 only). This implies that (over)designing (i.e., design for the best NF and IIP3) of each circuit may outperform a rather moderate design with the equilibrium criterion specification selection scheme, but with possible penalties in power consumption.

However, it could also be that an LNA topology with fewer components (i.e., transistors) than a mixer topology is still power efficient even if A<<0. In this case, it would be advantageous to relax the mixer performance, decreasing the absolute power consumption of a system.

Example 4.1:

As an illustration of the selection procedure outlined, we will now show an example with an NF and IIP3 over-designed LNA.

Given the NF' and IIP3 of the receiver and LNA (for a system shown in Fig. 4.1) as NF'_D=10dB (NF=10.4dB), $IIP3_D$=–10dBm, NF'_1=2dB (NF=4.1dB), and $IIP3_1$=–1dBm, we will allocate the noise and linearity parameters to the mixer.

With the aid of Eqs. (4.5) and (4.15), the equilibrium NF' and IIP3 equal NF'_E=5.3dB and $IIP3_E$=–5.3dBm. If we assume G_1=12dB, and $C_{NF'}$=–10dB and C_{IIP3}=–10dB, the noise and linearity parameters of the mixer will be $IIP3_2$=2.85dB and NF'_2=21dB, as calculated from Eqs. (4.7), (4.12) and (4.17).

This noise and the linearity over-designed LNA allows for the relaxed noise and linearity performance of the mixer, while still satisfying the required specifications. The contributions of the mixer noise and linearity at the input of the receiver (input of the LNA for the model in Fig. 1) are 9dB>>NF'_1 and –9.15dBm<<$IIP3_1$, respectively.

In order to determine the gain of the mixer, let us assume that the baseband circuitry hardly affects the equivalent input NF' or IIP3 (i.e., γ<<1; e.g., γ=0.1 and C=–10dB). Now, from Eq. (4.18), G_2=8dB for NF'_3 to be negligible, and from Eq. (4.13), G_2=–2dB for $IIP3_3$ to be dominant. Here, we assumed typical values for the baseband performance, being NF'_3=15dB, $IIP3_3$=15dBm and G_3=70dB [11,12].

Choosing G_2=8dB results in C_{IIP3}=0dB (B_{IIP3}=2) and $C_{NF'}$=–10dB ($B_{NF'}$=4), with the required values for $IIP3_2$=5dBm and NF'_2=21dB. For G_2=–2dB,

C_{NF}=0dB (B_{NF}=1.75) and C_{IIP3}=–10dB (B_{IIP3}=4.15), the requirements are NF'_2=18.75dB and $IIP3_2$=2.85dBm. The (G_2,NF'_2,$IIP3_2$) combination (8dB,21dB,5dBm) requires a larger gain, a better linearity, and tolerates a higher noise figure than the combination (–2dB,18.75dB,2.85dBm). The designer will make the final choice for the mixer performance parameters, having available circuit topology and power consumption information. This issue is discussed in more detail in Section 4.5.

This illustrative example of the performance selection procedure completes the discussion on the equilibrium design criterion.

4.3 Mutually Dependent Selection of *NF* And *IIP*3 Specifications

When assigning the system specifications to each circuit in the receive chain, it is common practice to consider each performance parameter separately [13,14]. However, as both the noise and the linearity depend on the gain of the corresponding circuits, optimizations of noise figure and third-order intercept point are not mutually exclusive. Because there has not yet been developed an exact optimization procedure, Eqs. (4.1) and (4.2) are employed for a large number of (g,F,P_{IIP3}) combinations, until all the requirements are satisfied. As there are many combinations that satisfy the required specifications, the experience of the designer is what usually guides to the final decision, giving this fundamental problem a speculative rather than a scientific dimension.

We will develop a procedure for assigning NF and IIP3 specifications not by optimizing the system performance with respect to NF and IIP3, but to the ratio (F-1)/P_{IIP3} (*NF'-IIP*3 in dB). This appears to be a logical optimization parameter, establishing a relationship with the spurious free dynamic range (SFDR) of the system that is proportional to P_{IIP3}/F (*IIP*3-*NF* in dB). Being inversely related to the *SFDR*, but also the dynamic range, we will refer to the (F-1)/P_{IIP3} as to the *inverse dynamic range* (linear term *idr;* logarithmic term *IDR=NF'-IIP*3).

4.3.1 The Optimality Criterion

We introduce the optimality criterion by minimizing the ratio of the relative noise power and third-order power intercept point, (F-1)/P_{IIP3}, referred to the

input of the receiver. For the sake of easier interpretation of the optimization procedure, we will resort to a two-block receiver system, consisting of an LNA and a mixer (e.g., assuming high performance baseband circuitry). For systems dominated by third- rather than second-order intermodulation-distortion, combining Eqs. (4.1) and (4.2), the inverse dynamic range can be expressed as

$$idr = \frac{F-1}{P_{IIP3}} = \left(F_1 - 1 + \frac{F_2 - 1}{g_1} \right) \left(\frac{1}{P_{IIP3,1}} + \frac{g_1}{P_{IIP3,2}} \right). \tag{4.19}$$

Assuming that for any (NF_1,$IIP3_1$) and (NF_2,$IIP3_2$) performance parameters combination there *exists* an optimal gain value $g_{1,OPT}$, then it can be found by solving Eq. (4.20).

$$\left. \frac{\partial idr}{\partial g_1} \right|_{g_1 = g_{1,OPT}} = 0 \tag{4.20}$$

This optimum gain $G_{1,OPT}$ (in dB) equals

$$G_{1,OPT}[dB] = \frac{NF_2^{'} + IIP3_2 - NF_1^{'} - IIP3_1}{2}. \tag{4.21}$$

We refer to (NF_1,$IIP3_1$,$G_{1,OPT}$) and (NF_2,$IIP3_2$) as to the optimal design point. Substituting the optimum gain into Eq. (4.19), the optimum inverse dynamic range IDR_{OPT} (*NF'-IIP*3) becomes

$$IDR_{OPT} = 20\log\left(10^{\frac{NF_1^{'} - IIP3_1}{20}} + 10^{\frac{NF_2^{'} - IIP3_2}{20}} \right). \tag{4.22}$$

The optimum gain $G_{1,OPT}$ of an LNA, Eq. (4.21), provides the receiver with the optimum inverse dynamic range, Eq. (4.22) (i.e., the maximum dynamic range). The lower the *IDR,* the larger the dynamic range.

Figure 4.3 shows an *inverse dynamic range* (IDR) *diagram* for an optimal dynamic range design point. The IDR diagram describes graphically the distribution of noise and linearity parameters throughout the receive chain. It

is used as a tool for visualization of different selection criteria and design choices on the system performance.

The noise parameter is positioned above the linearity parameter so as to map their difference as defined by the IDR. However, their position with respect to each other in the diagram is not quantitatively related (i.e., *NF'* is not necessarily a larger number than *IIP*3). Each step (or level) in the IDR diagram corresponds to one stage of the receive chain, indicated by LNA and MIXER at the top of Fig. 4.3. The sloped transition indicates a transformation (gain) between the stages, which is also shown in Fig. 4.3. When referred to the LNA input via the gain $G_{1,\mathrm{OPT}}$, the NF' and IIP3 of the mixer (NF'_2 and $IIP3_2$) become $NF'_{2\text{-}1}$ and $IIP3_{2\text{-}1}$.

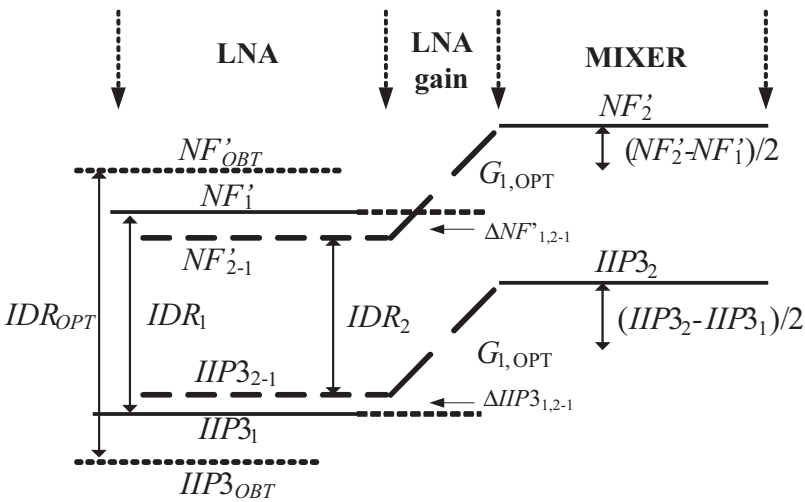

Figure 4.3: The inverse dynamic range diagram for an optimal dynamic range design point.

As can be seen from Fig. 4.3, input referred noise and linearity of each receiver block (or IDR_1, IDR_2) *balance* the equivalent *IDR*, and accordingly the dynamic range of the optimal system [15,16]. Namely, the relative noise figure of the mixer referred to the input of the LNA ($NF'_{2\text{-}1}$) relates to that of the LNA (NF'_1) as

$$\Delta NF'_{1,2-1} = NF'_1 - NF'_{2-1} = NF'_1 - (NF'_2 - G_{1,OPT}) = \\ = \frac{NF'_1 - NF'_2}{2} + \frac{IIP3_2 - IIP3_1}{2} \quad . \tag{4.23}$$

The IIP3 of the mixer referred to the input of the LNA ($IIP3_{2\text{-}1}$) relates to $IIP3_1$ as

$$\Delta IIP3_{1,2-1} = IIP3_1 - IIP3_{2-1} = IIP3_1 - (IIP3_2 - G_{1,OPT}) = \\ = -\frac{NF'_1 - NF'_2}{2} - \frac{IIP3_2 - IIP3_1}{2} \quad . \tag{4.24}$$

Comparing Eqs. (4.23) and (4.24), we obtain

$$\Delta IIP3_{1,2\text{-}1} = -\Delta NF'_{1,2\text{-}1} \, . \tag{4.25}$$

This suggests that the relationship between the noise parameters of the LNA and mixer referred to the input of the receiver is the same as the relationship between the linearity parameters of these circuits referred to the input of the receiver, but with the opposite sign. $\Delta IIP3_{1,2\text{-}1}$ and $\Delta NF'_{1,2\text{-}1}$ are shown in Fig. 3. Depending on the circuits performance, Eqs. (4.23) and (4.24) can be either positive or negative, which in the end determines whether $IIP3_{2\text{-}1} > IIP3_1$ ($NF'_{2\text{-}1} < NF'_1$) or $IIP3_{2\text{-}1} < IIP3_1$ ($NF'_{2\text{-}1} > NF'_1$).

Note at this point that for $\Delta IIP3_{1,2\text{-}1} = -\Delta NF'_{1,2\text{-}1} = 0$, the optimal design point becomes the equilibrium design point. Another interesting relationship between the linearity and noise parameters can be obtained after rearranging Eq. (4.25) as

$$NF'_1 + IIP3_1 = NF'_{2-1} + IIP3_{2-1} \tag{4.26}$$

implying that the sum of the input referred noise and linearity parameters of the optimal receiver blocks are equal. We will detail on this result latter in this section.

Let us now elaborate in more detail on the simultaneous noise and linearity performance optimization procedure (i.e., IDR optimization).

The optimum IDR design point doesn't always satisfy the individual noise and linearity specifications, even though it provides the receiver (prior to the LNA) with the maximum dynamic range. The condition that provides

optimum IDR and satisfies the system specifications can be derived from Eqs. (4.1) and (4.2). Namely, with the aid of Eq. (4.21), the system F' and P_{IIP3} can be written as

$$F-1=\sqrt{(F_1-1)P_{IIP3,1}}\left[\sqrt{\frac{F_1-1}{P_{IIP3,1}}}+\sqrt{\frac{F_2-1}{P_{IIP3,2}}}\right], \tag{4.27}$$

$$\frac{1}{P_{IIP3}}=\frac{1}{\sqrt{(F_1-1)P_{IIP3,1}}}\left[\sqrt{\frac{F_1-1}{P_{IIP3,1}}}+\sqrt{\frac{F_2-1}{P_{IIP3,2}}}\right]. \tag{4.28}$$

The condition for the IDR_{OPT} that also satisfies the system requirements is obtained by substituting Eq. (4.22) into Eqs. (4.27) and (4.28), which gives

$$2NF'_{OBT}=NF'_1+IIP3_1+IDR_{OPT}<2NF'_D, \tag{4.29}$$

$$2IIP3_{OBT}=NF'_1+IIP3_1-IDR_{OPT}>2IIP3_D. \tag{4.30}$$

NF'_{OBT} and $IIP3_{OBT}$ are the noise and linearity parameters obtained.

Suppose that the noise and the linearity of the LNA are known, then the above conditions (and Eq. (4.22)) can be transformed into Eqs. (4.31) and (4.32) that give an explicit relationship between the (NF'_1,$IIP3_1$) and (NF'_2,$IIP3_2$) pairs.

$$NF'_2-IIP3_2<20\log\left(10^{\frac{2NF'_D-NF'_1-IIP3_1}{20}}-10^{\frac{NF'_1-IIP3_1}{20}}\right) \tag{4.31}$$

$$NF'_2-IIP3_2<20\log\left(10^{\frac{-2IIP3_D+NF'_1+IIP3_1}{20}}-10^{\frac{NF'_1-IIP3_1}{20}}\right) \tag{4.32}$$

Conditions (4.29)-(4.32) obey condition (4.33) as well.

$$NF'_1+IIP3_1=NF'_{OBT}+IIP3_{OBT} \tag{4.33}$$

Equation (4.33) has the same form as Eq. (4.26), and implies that for a receiver with an optimal dynamic range, the combined relative noise figure and third-order input-intercept point of the receiver circuits with respect to the receiver input are equal. In the remainder of this chapter we will often refer to the above conditions as to the optimality criterion.

Given the specifications of receiver blocks partly, the optimality criterion allows the selection of undetermined performance parameters while providing maximal dynamic range.

Example 4.2:

Let us clarify the optimality selection procedure with an example of a noise-figure limited system.

Given NF'_D=10dB, $IIP3_D$=–10dBm, NF'_1=9dB, $IIP3_1$=5dBm, the relative noise figure and third-order input-intercept point of the mixer must satisfy the inequality NF'_2–$IIP3_2$<–7.7dB (Eqs. (4.31) and (4.32)), in order to provide the system with the required specifications. Pair NF'_2=10dB and $IIP3_2$=17.7dBm can be, for example, an IDR optimal design point, resulting in an optimum gain $G_{1,OPT}$=6.85dB and IDR_{OPT}=6dB. As will be explained in the next section, for a system with poor noise or linearity performance, as it is the case in this example (poor noise figure), the optimum design point can be rather unrealistic with respect to the requirements that it imposes on the system blocks (e.g., $IIP3_2$=17.7dBm).

4.3.2 The Equality Criterion

Making equal the system noise and linearity performance margins with respect to the requirements, we introduce the equality criterion. With this criterion we balance the optimization procedures of these two performance parameters. In this section, we will determine the relationships between the circuit performance for the equivalent improvements in the noise and linearity parameters from the required receiver specifications NF'_D and $IIP3_D$ (referred to the input of the LNA).

The *IDR* equivalent-contribution gain $G_{1,EQ}$ can be found from Eqs. (4.34) and (4.35), or when combined from Eq. (4.36).

$$NF'_D - NF'_{OBT} = -\Delta \tag{4.34}$$

$$IIP3_{\mathrm{OBT}} - IIP3_D = -\Delta \tag{4.35}$$

$$NF'_{OBT} + IIP3_{OBT} = NF'_D + IIP3_D \tag{4.36}$$

$\Delta \tilde{<} 0$ (in dB) stands for the improvement (margin) in both the NF' and the IIP3 of the receiver, with the obtained specifications being always better than the required ones (i.e., $NF'_{OBT} < NF'_D$ and $IIP3_{OBT} > IIP3_D$). The range of the margin Δ is

$$\Delta \in (\max\{IIP3_D - IIP3_1, NF'_1 - NF'_D\}, 0]. \tag{4.37}$$

Given, for example, NF'_1 and $IIP3_1$, the range of NF'_2 –$IIP3_2$ values can be determined by modifying Eqs. (4.1) and (4.2). This is shown by Eqs. (4.38) and (4.39),

$$\frac{F_2 - 1}{g_{1,EQ}} \cong \delta(F_D - 1) - (F_1 - 1), \tag{4.38}$$

$$\frac{g_{1,EQ}}{P_{IIP3,2}} = \frac{\delta}{P_{IIP3,D}} - \frac{1}{P_{IIP3,1}}, \tag{4.39}$$

where $\Delta = 10\log\delta$. Now, a combination of the noise and linearity performance of the mixer that satisfies the system specifications can be determined from Eq. (4.40), which is obtained by combining Eqs. (4.38) and (4.39).

$$NF'_2 - IIP3_2 = 10\log\left(10^{\frac{\Delta + NF'_D}{10}} - 10^{\frac{NF'_1}{10}}\right) + 10\log\left(10^{\frac{\Delta - IIP3_D}{10}} - 10^{\frac{-IIP3_1}{10}}\right) \tag{4.40}$$

Similarly, the equivalent gain $G_{1,EQ}$ of the first receiver block (LNA) is calculated from Eqs. (38) and (39) as

$$G_{1,EQ} = NF'_2 - 10\log\left(10^{\frac{\Delta + NF'_D}{10}} - 10^{\frac{NF'_1}{10}}\right) \tag{4.41}$$

and

$$G_{1,EQ} = IIP3_2 + 10\log\left(10^{\frac{\Delta - IIP3_D}{10}} - 10^{\frac{-IIP3_1}{10}}\right). \tag{4.42}$$

If the performance parameters of the LNA and mixer are selected as suggested by Eqs. (40)-(42), both the noise and linearity performance contribute equally to the dynamic range (i.e., the obtained *NF'* and *IIP*3 are equally improved by Δ as given by Eqs. (4.34) and (4.35)). The following example and the IDR diagram shown in Fig. 4.4 illustrate this.

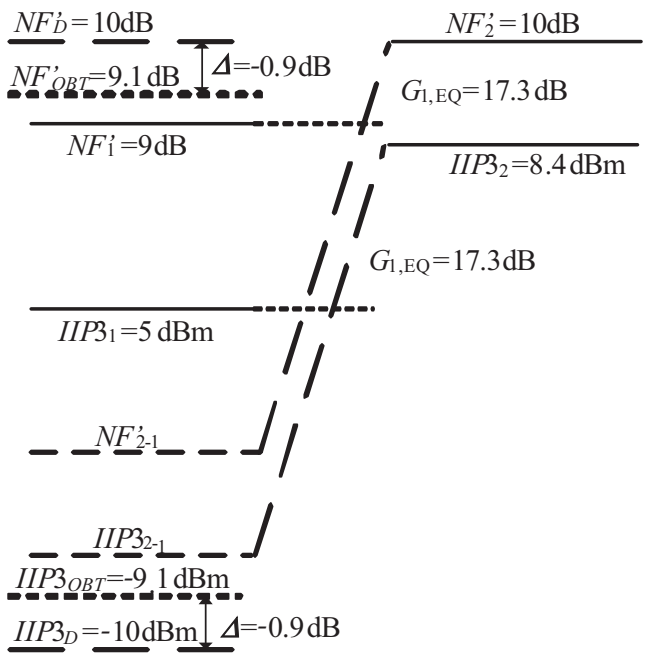

Figure 4.4: The inverse dynamic range diagram for the equivalent noise and linearity margins with respect to the inverse dynamic range requirement.

Example 4.3:

Referring to the example for the optimum design point (Example 4.2), the following is obtained from the equality conditions: NF'_2–$IIP3_2$=1.6dB for the chosen Δ=–0.9dB ($\Delta\in(-1,0]$). One solution, NF'_2=10dB and $IIP3_2$=8.4dBm with the gain $G_{1,EQ}$=17.3dB, provides the system with the IDR_{EQ}=18.2dB (NF'_{OBT}=9.1dB and $IIP3_{OBT}$=–9.1dBm), thus, with an equal improvement of 0.9dB for both the relative noise figure and the third-order input-intercept point. The corresponding performance parameters are shown in Fig. 4.4.

4.3.3 Optimality vs. Equality

As suggested in Section 4.3.1, for systems with poor noise and/or linearity from one circuit, the optimum design point can be rather unrealistic, i.e., "expensive" with respect to the requirements that it imposes on other circuits. This becomes obvious if we reconsider Example 4.2. The IDR diagram for the optimal receiver in this case is shown in Fig. 4.5.

In this example of a noise-limited system (a poor *NF'* of the LNA), which also satisfies the system performance, a mixer with very high linearity is required for the optimum IDR. This is suggested by Eqs. (4.31) and (4.32): the larger the NF'_1, the more negative the difference NF'_2–$IIP3_2$ required, or in other words, the better the $IIP3_2$ required. For the example considered, the optimality condition, NF'_2–$IIP3_2$<–7.7dB, requires an $IIP3_2$=17.7dBm for a moderate relative noise figure NF'_2=10dB (see OP-1 in Table 4.2). As given by Example 4.2, this results in $G_{1,OPT}$=6.85dB, IDR_{OPT}=6dB, and the system noise and linearity NF'_{OBT}=10dB and $IIP3_{OBT}$=4dB. This system just satisfies the noise requirement, but it is over-designed for linearity, given NF'_D=10dB and $IIP3_D$=–10dBm.

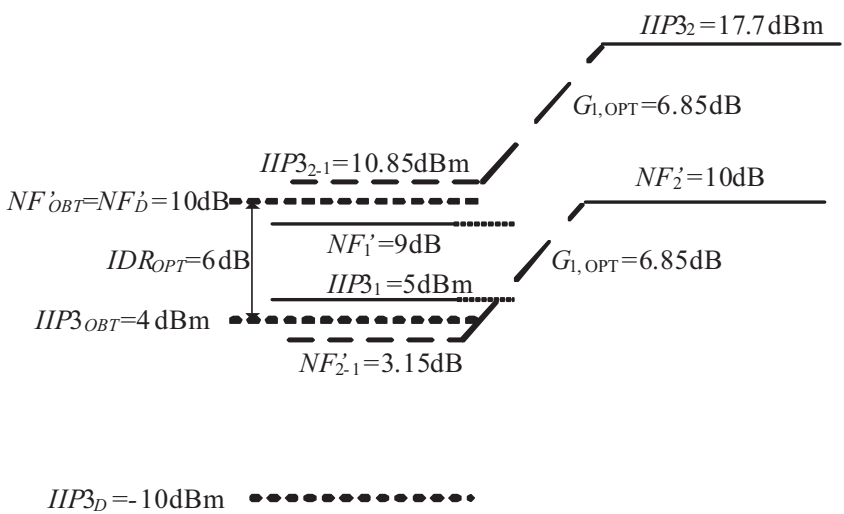

Figure 4.5: IDR diagram for a demanding optimum design point.

Table 4.2: Block performance for NF'_D=10dB, $IIP3_D$=−10dBm, NF'_1=9dB, and $IIP3_1$=5dBm.

	NF'_2 [dB]	$IIP3_2$ [dBm]	G_1 [dB]	NF'_{OBT}[dB]	$IIP3_{OBT}$	IDR_{OBT}
OP-1	10	17.7	6.85	10	4 dBm	6 dB
OP-2	10	8.4	2.2	11.5	2.6 dBm	8.9 dB
EQ	10	8.4	17.4	9.1	-9.1 dBm	18.2 dB

OP-1: optimum design point for satisfied system requirements;
OP-2: optimum design point for unsatisfied system requirements;
EQ: equality design point for satisfied system requirements.

However, by choosing for a moderate linearity of the mixer, $IIP3_2$=8.4dB and NF'_2=10dB, as suggested by example in Section 4.3.3, results in $G_{1,OPT}$=2.2dB, IDR_{OPT}=8.9dB, NF'_{OBT}=11.5dB and $IIP3_{OBT}$=2.6dBm (see OP-2 in Table 4.2). This suggests that violating conditions (4.31) and (4.32), the unsatisfactory noise performance of the system is obtained.

These findings imply that the optimum design point imposes moderate requirements on circuits in the vicinity of conditions (4.33) and (4.36). The further from these conditions, the more demanding the design requirements result from the optimality conditions, Eqs. (4.31) and (4.32). The equality criterion could be considered in such situations, as given by Example 4.3 and EQ in Table 4.2.

4.4 Equilibrium, Optimality and Equality Criteria

In this section we will determine relationships between the criteria introduced for selection of performance parameters for receiver circuits. With the aid of Eq. (4.33), being the optimality criterion, and Eq. (4.36), being the equality criterion, the condition where these criteria meet has a form,

$$NF_1' + IIP3_1 = NF_D' + IIP3_D\,, \tag{4.43}$$

with conditions (4.29), (4.30), (4.34) and (4.35) satisfied.

This condition can be obtained by substituting the optimal design point, Eqs. (4.29) and (4.30), into the conditions for the equivalent performance

margins, Eqs. (4.34) and (4.35). Accordingly, the simultaneous optimality and equality criteria impose the condition

$$NF_D' - \frac{NF_1' + IIP3_1 + IDR_{OPT}}{2} = \frac{NF_1' + IIP3_1 - IDR_{OPT}}{2} - IIP3_D, \quad (4.44)$$

which is equal to Eq. (4.43), as expected.

A property of this optimality-equality condition (Sections 4.3.1 and 4.3.2) is that it coincides with the condition for the independent selection of performance parameters (Section 4.2). Namely, if condition (4.43) is satisfied, the equilibrium design point (the equal contributions of each block performance parameters to the system performance) encompasses the optimum design point (maximum inverse dynamic range) and the equality point (equal contribution of the relative noise figure and the third-order input-intercept point to the IDR). The IDR diagram for the simultaneously satisfied equilibrium-optimum-equality condition is shown in Fig. 4.6.

Complying with Eq. (4.43), the allocation of all the specifications to each of the blocks in the receive chain is controlled by means of the conditions derived in this section.

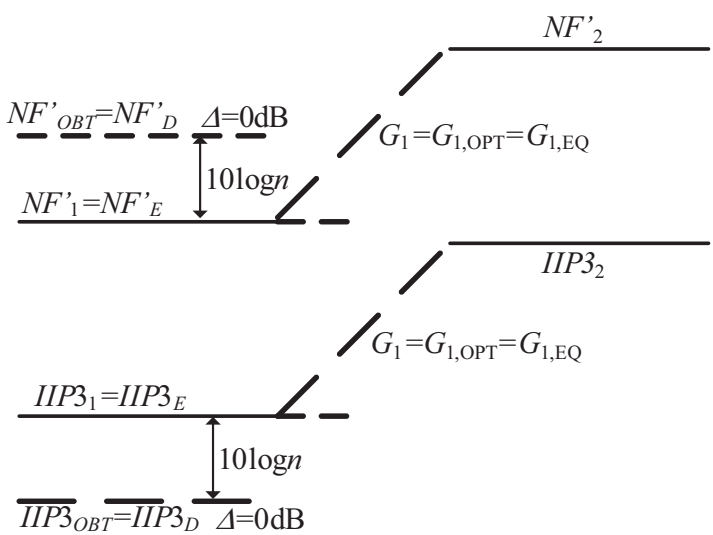

Figure 4.6. The inverse dynamic range diagram for the simultaneously satisfied equilibrium, optimum, and equality conditions.

Example 4.4:

We will illustrate the aforementioned findings by an example of the simultaneously satisfied equilibrium, optimality and equality conditions. The required specifications are NF'_D=10dB and $IIP3_D$=–10dBm.

The performance parameters allocated to the LNA according to Eqs. (4.5) and (4.10) result in a design point satisfying all the design criteria, i.e., the optimal distribution of both the individual and the mutually dependent specifications. From Eq. (4.5), NF'_E=7dB and $IIP3_E$=–7dBm, if n=2 (LNA and mixer). Referring to Eqs. (4.11) and (4.16), the performance parameters of the LNA become NF'_1=7dB and $IIP3_1$=–7dBm.

From Eq. (4.40), the equality condition is NF'_2–$IIP3_2$=14dB. Choosing, for example, for NF'_2=16dB and $IIP3_2$=2dBm results in $G_{1,EQ}$=9dB.

On the other hand, the optimum IDR condition is determined from Eq. (4.31) to be NF'_2–$IIP3_2$<19dB. The already determined mixer parameters automatically satisfy this condition. From Eq. (4.21), the optimum gain equals $G_{1,OPT}$=9dB, being the same as $G_{1,EQ}$.

Finally, referring the noise and linearity parameters of the mixer to the input of the receiver we obtain: $NF'_{2\text{-}1}$=16–9=7dB and $IIP3_{2\text{-}1}$=2–9=–7dBm, being the equilibrium quantities already calculated by Eq. (4.5).

In the remainder of this section we will discuss the implications of not being at the equilibrium on the dynamic range.

4.4.1 Optimal SFDR of Receiver Circuits

The dynamic range of a system where the spurious response is minimal is referred to as the spurious free dynamic range. The higher end of the SFDR is determined by the signal power level (P_{MAX}) at which the (output) third-order intermodulation product is equal to the noise level (N_O) [1]. Input and output maximal signal power levels of a system are given by Eqs. (4.45) and (4.46) [1,17],

$$P_{MAX}^3 = nf \cdot P_{IIP3}^2 \tag{4.45}$$

$$P_{OMAX}^3 = N_O \cdot P_{OIP3}^2 \tag{4.46}$$

where P_{OIP3} stands for the output third-order intercept power point, and nf for the noise floor defined as

$$nf = N_O / g = 10\log KTB + NF \,. \tag{4.47}$$

K for Boltzmann constant, T for the absolute temperature, and B for the bandwidth.

The lower end of the SFDR is related to the minimum detectable signal, i.e., a signal power level (P_{MIN}) that allows for detection with a desired signal-to-noise ratio and accordingly desired error probability (or bit-error rate).

The SFDR is defined by Eq. (4.48) [1,17].

$$SFDR = \frac{1}{SNR}\left(\frac{P_{IIP3}}{nf}\right)^{\frac{2}{3}} \tag{4.48}$$

Let us now consider a situation where $IIP3_1$ of an LNA is better than equilibrium $IIP3_E$.

Maximum signal power at output of an LNA ($P_{OMAX,1}$) and input of a mixer ($P_{IMAX,2}$) is given by Eqs. (4.49) and (4.50),

$$P_{OMAX,1} = \sqrt[3]{nf \cdot g_1 \cdot P_{OIP3,1}^2} \,, \tag{4.49}$$

$$P_{IMAX,2} = \sqrt[3]{nf \cdot g_1 \cdot P_{IIP3,2}^2} \,, \tag{4.50}$$

where the noise floor at output of the LNA (or input of the mixer) is $nf{\cdot}g_1$. If the LNA $IIP3$ is better than the equilibrium,

$$P_{OIP3,1} > P_{IIP3,2} = g_1 \cdot P_{IIP3,E} \,, \tag{4.51}$$

then the maximum output power of the LNA is larger than the maximum input power expected from the mixer. This is derived from Eqs. (4.49) and (4.50), as given by Eq. (4.52).

$$P_{OMAX,1} = g_1 \cdot P_{IMAX,1} > P_{IMAX,2} \tag{4.52}$$

Figure 4.7 depicts the spurious-free dynamic range of the mixer, as it would be in a receiver, in the described situation (for simplicity, SNR=0dB assumed). For the maximal LNA signal, as given by Eq. (4.52), the SFDR at the output of the mixer in the receiver is lower than the equilibrium SFDR

($SFDR_{1\text{-}2}<SFDR_E$). This implies that improving the linearity performance of an LNA beyond equilibrium actually degrades the SFDR of a system for the maximum input signal anticipated for which the LNA is (over)designed.

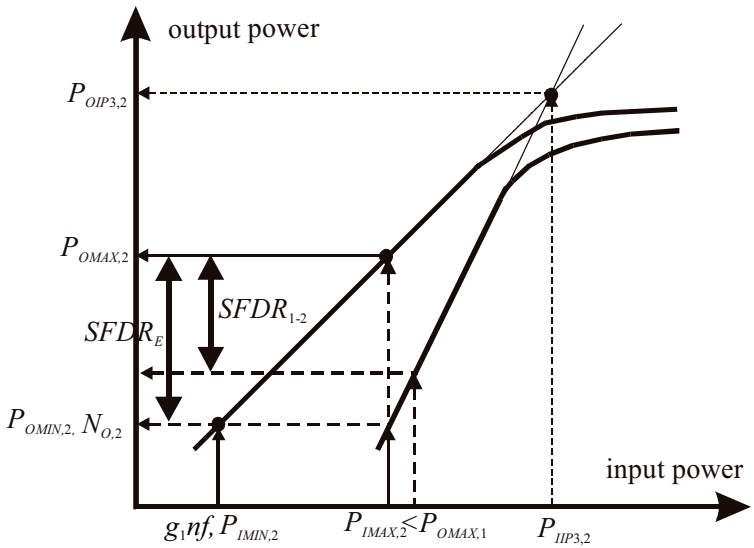

Figure 4.7: Spurious-free dynamic range of a mixer in a receiver.

Figure 4.8 depicts the SFDR of an LNA in another situation: $IIP3_1$ is worse than $IIP3_E$. Here, the SFDR at the input of an LNA is degraded ($SFDR_{2\text{-}1}<SFDR_E$) for the maximum mixer signal power acceptable, when referred to the input of an LNA.

$$P_{IMAX,1} < P_{IMAX,2} / g_1 \tag{4.53}$$

From Eqs. (4.52) and (4.53) and Figs. 4.7 and 4.8, we conclude that the equilibrium design of all circuits lends itself to the best usage of the dynamic range throughout a receiver chain, as already implied by previous sections (and Fig. 4.6).

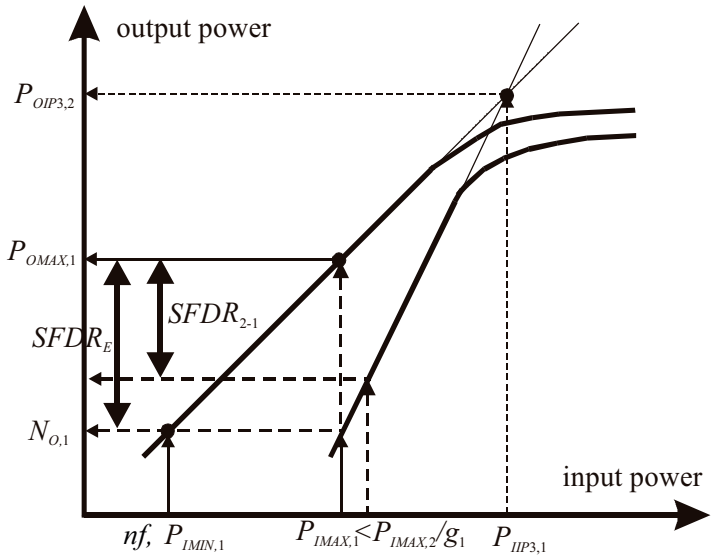

Figure 4.8: Spurious-free dynamic range of an LNA in a receiver.

4.5 Notes on Power Consumption

In the foregoing discussion, the selection of specifications for receiver circuits is considered without explicitly addressing the power consumption issue. Namely, whether the equilibrium point, the optimum point, and the equality point are also power-consumption efficient depends upon a number of factors. The available power budget and the chosen circuit implementation and production technology are just some of them.

In Sections 4.2 and 4.3 it has been advocated for the *desired* (*NF',IIP3,G*) combination of each circuit block. However, only at the circuit level, the relationship between the four parameters, viz., *NF', IIP3, G,* and power consumption, can be exactly determined. Whether the *obtained* specifications coincide the *desired* specifications depends on the available power budget.

For example, whereas a combination (0,0,0) of *A, B*, and *C* deviations provides an optimal allocation of noise and linearity performance for receiver circuits, optimal power consumption of a receiver may result from a different (*A,B,C*) combination. Power consumption of a complete receiver may be determined as a function of (*A,B,C*) combinations satisfying system performance (for each (*A,B*) combination, there is a unique *C*), while

assuming realistic deviation values (e.g., $-5<A,B,C<5$ for a three-block system). Then, a combination of deviations can be determined that provides a system with the minimum power consumption.

As a qualitative example, consider a two-block system, consisting of an inductively degenerated single-ended low-noise amplifier [18,19] and a Gilbert mixer [20]. Referring to Example 4.4, the equilibrium point of the LNA could be determined: NF'_1=7dB, $IIP3_1$=–7dBm, and G_1=9dB, with $A_{NF'}=A_{IIP3}=0$ and power consumption PC_1. The mixer equilibrium point is obtained as NF'_2=16dB, $IIP3_2$=2dBm, with $B_{NF'}=B_{IIP3}=0$ and power consumption PC_2. We will assume that $PC_2>>PC_1$, as the mixer has more transistor branches compared to the LNA (which has only one branch) as well as far better third-order input-intercept point.

As a result of a large difference in power consumptions between the receiver circuits, some improvement in LNA noise and linearity performance ($A_{NF'}<0$ and $A_{IIP3}<0$) would still result in $PC_2>PC_1+\Delta PC_1$, ΔPC_1 being the increase in the LNA power consumption [19,21,22]. On the other hand, the relaxed mixer performance requirements resulted ($B_{NF'}<0$ and $B_{IIP3}<0$) would allow for reduction in the mixer power consumption, PC_2-ΔPC_2. For similar deviations A and B, it could be expected that $\Delta PC_2>\Delta PC_1$, thus, the system specifications satisfied with possible benefits in power consumption.

In Chapter 7 of this book we will apply the selection procedure outlined in this chapter to determine the performance parameters for receiver circuits according to the requirements of the 2.1GHz-WCDMA standard [23].

4.6 Performance Trade-offs in an RF Circuit

There is just a rough impression of how RF circuits trade power consumption for performance. Moreover, if the key circuit parameters are set by a communication system in an adaptive way and not fixed by a hardware design, many concepts fail due to incomplete knowledge of how the change of one parameter is reflected in the others.

Various phenomena and concepts related to RF circuits can be both qualitatively and quantitatively interpreted by means of the K-rail diagrams that are introduced in this section. K-rail diagrams allow for the performance characterization of circuits, and describe (i.e., visualize) relationships and trade-offs between their performance parameters: these are voltage swing, tank conductance, power consumption, phase noise and loop gain for

oscillators as well as noise figure, linearity, gain and power consumption for amplifiers.

In the remainder of this section, trade-offs between the performance parameters of an inductively-degenerated (ID) [19] low-noise amplifier are discussed with the aid of the K-rail diagram, shown in Fig. 4.9. The design of LNAs imposes many trade-offs between gain, noise figure, linearity, and power consumption. Some of the challenging goals of the multi-objective LNA design procedure are:

- provision of a sufficient gain in order to minimize noise contribution of the receiver circuits proceeding an LNA, while not degrading system linearity.

- optimization of amplifier's noise figure with simultaneous noise and power match at input of an LNA.

- operation at low power-consumption levels in order to ensure long battery life of a mobile device.

The relationships between the noise figure, linearity, gain, optimum source resistance, input impedance, and power consumption of an ID-LNA are described in Fig. 4.9 [24].

The arrows in the diagram perpendicular to the corresponding axes represent lines of constant gain, NF, IIP3, input impedance, optimum source impedance, and power consumption. Namely, each point in the design space (in this case a line; the k-rail) corresponds to a set of design parameters that are obtained as a normal projection of the design point on the rail to the indicated axes.

For example, a point that corresponds to the optimum of the minimum noise figure (minimum noise figure under noise-matched conditions) is shown as OPT-MIN. Parameters of this point are noise figure $NF_{OPT\text{-}MIN}$, voltage gain $VG_{OPT\text{-}MIN}$, linearity $IIP3_{OPT\text{-}MIN}$, and optimum (noise) source resistance and input impedance R_S (both equal to source resistance). A parameter $k_{OPT\text{-}MIN}$ is related to power consumption.

With the aid of the K-rail diagram, we can describe the effects of a particular design choice on the performance of amplifiers.

Consider a situation where radio-channel conditions improve, i.e., a receive signal is much larger than noise and interferers (large input signal-to-noise-and-interference ratio). Here, the LNA doesn't have to operate with the best noise figure and gain and accordingly waste power. It is possible to operate at a moderate gain to the extent that the noise figure and sensitivity of a receiver

are not degraded, with power savings in turn. This situation corresponds to point LOW in the K-rail diagram.

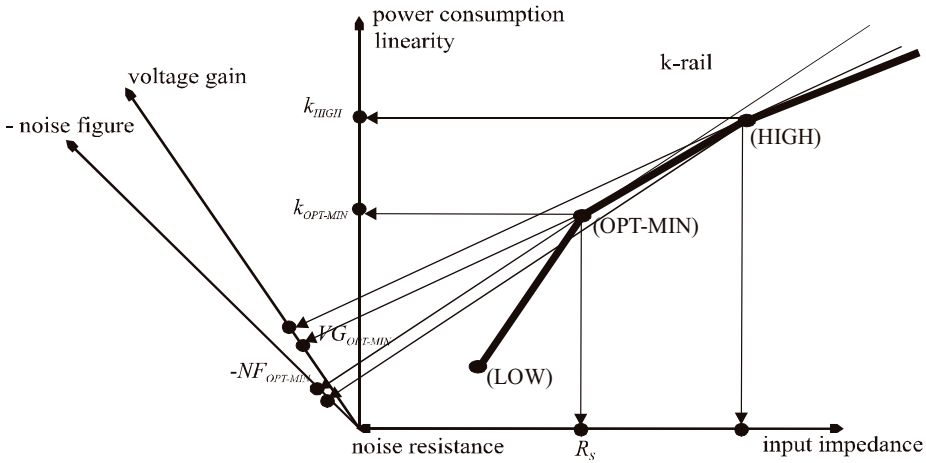

Figure 4.9: LNA K-rail diagram.

On the other hand, a weak receive signal requires large amplification and low noise figure from an LNA in order to achieve the desired signal-to-noise ratio at the end of a receive chain. In this situation, a HIGH design point can be chosen.

Finally, point OPT-MIN has the advantage of lower *NF* and power consumption, but at the cost of lower gain and *IIP*3 compared to point HIGH. Compared to point LOW, better gain, *NF* and linearity and higher power consumption result.

Similarly, design trade-offs for other RF circuits can be mapped onto corresponding K-rail diagrams [25]. K-rail diagrams for low-noise amplifiers and voltage-controlled oscillators are detailed in Chapters 5 and 6, respectively.

4.7 Conclusions

The procedure for allocation of the performance parameters to the receiver circuits has been introduced in this chapter.

It has been shown that there exists an equilibrium design point for which the contributions of each block performance parameters to the system performance are equal. The assignment of the specifications to the receiver circuits for the equal noise and linearity margins with respect to the dynamic range has been proposed as another method. By optimizing the system performance with respect to the ratio $(F\text{-}1)/P_{IIP3}$, the optimal dynamic range design point has been found which satisfies both the noise and the linearity requirements. Furthermore, it has been shown that the equilibrium design choice may coincide with both design for the optimal dynamic range and design for the equal margins of each performance parameter with respect to the required specifications. The selection procedures proposed improve the understanding of relationships and trade-offs between the performance of a receiver and receiver circuits.

Finally, some design trade-offs in a single RF circuit are discussed using the K-rail diagram.

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Chapter 5

ADAPTIVITY OF LOW-NOISE AMPLIFIERS

The wireless telecommunication transceivers of both today and the future have to be broadband [1], low power [2], and adaptive [3]. Broad bandwidth supports the high data rates demanded by emerging applications. Adaptivity accommodates varying channel conditions and application requirements, while consuming as little energy as possible ensures long talk time on one battery charge.

However, receiver circuits are typically designed to perform one specific task, while key parameters such as dynamic range, bandwidth and selectivity are fixed by hardware design and not by the communication system in an adaptive way. As a result, today's receiver topologies are designed to function under the most stringent conditions, which increases circuit complexity and power consumption.

The variant nature of radio-channel conditions and accordingly variable requirements imposed on receiver circuits in the direct signal path urge for designs that can respond to such changes "on-the-fly".

Adaptivity figures of merit (AFOM) (i.e., adaptivity models) of low-noise amplifiers are derived in this chapter. They reveal the relationships and trade-offs between the performance parameters of an adaptive low-noise amplifier, viz., noise figure, gain, linearity and power consumption. Moreover, adaptivity models form the basis for the design of low-noise amplifiers that operate across multiple standards.

This chapter is organized in the following way. Adaptivity of amplifiers is discussed next. The subject of Section 5.2 is performance characterization of low-noise amplifiers: input-impedance (power-matching) model, gain-model and noise-model parameters are determined. Adaptivity models are derived in Section 5.3, giving insight into the extent to which LNA performance parameters can vary while not degrading overall system performance. The relationships between the performance and power consumption of adaptive

low-noise amplifiers are graphically described by means of the amplifier K-rail diagram.

5.1 Adaptivity Phenomena of Amplifiers

In order to understand how the change in one performance parameter is reflected to the others, we introduce adaptivity phenomena and their models [4].

Some of the low-noise amplifier adaptivity phenomena are: noise-figure, linearity, gain, and input-impedance tuning. Corresponding adaptivity figures of merit are shown in Fig. 5.1 on the amplifier K-rail diagram: input- and optimum source-resistance tuning ranges (*RITR* and *RSTR*), voltage-gain tuning range (*VGTR*), noise-figure tuning range (*NFTR*), and tuning range of input-referred third-order intercept point (*IIP*3*TR*). Adaptivity phenomena and their figures of merit describe the change of circuit performance with respect to power consumption (which is related to parameter *k*). For example, *NFTR* relates to noise-figure difference for different biasing conditions.

The amplifier K-rail diagram is constructed for an inductively-degenerated low-noise amplifier (ID-LNA) [5,6], shown in Fig. 5.2, following the rules outlined in the previous chapter. This amplifier topology allows for simultaneous input power and noise matching: real parts of optimum source (noise) impedance and amplifier input impedance could be adjusted independently, whereas their imaginary parts cancel simultaneously [6].

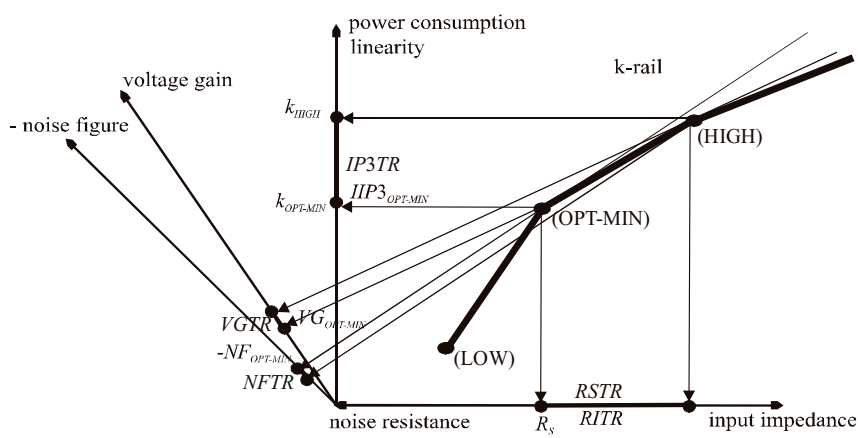

Figure 5.1: K-rail diagram for an adaptive LNA.

Points LOW and HIGH of the K-rail diagram have already been defined in Section 4.6. We refer to the noise-figure difference between points HIGH and OPT-MIN (or OPT-MIN and LOW) as the noise-figure tuning range: it corresponds to change of amplifier's noise figure with respect to power consumption. Designing for noise figure of an amplifier that covers a noise-figure tuning range NF_{HIGH}-$NF_{OPT\text{-}MIN}$ (shown as *NFTR* in Fig. 5.1) accounts for different operating conditions and satisfies LNA performance over a certain range rather than in a fixed design point only. This is an example of the application of the design for adaptivity to amplifiers.

Furthermore, this K-rail diagram shows that an increase in power results in an improvement of noise figure and voltage gain, but only to the levels determined by $k_{OPT\text{-}MIN}$ (point OPT-MIN), and k_{HIGH} (point HIGH corresponds to maximum transit frequency of input transistor Q_1 in Fig. 6.2), respectively. Due to shallow nature of the noise figure (small *NFTR*) near the optimum-minimum noise-figure point for ID-LNAs, considerable power savings (point LOW) as well as linearity improvements (point HIGH) could be achieved.

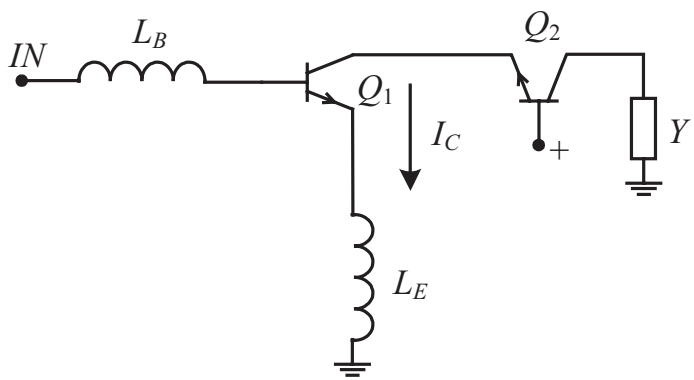

Figure 5.2: Inductively-degenerated LNA: L_E and L_B stand for the emitter and base matching inductors; biasing not shown.

Relationships between power consumption and input impedance, gain, noise figure and linearity are determined next. The adaptivity models (and adaptivity tuning ranges) are described analytically latter in this chapter, forming a base for design of adaptive LNAs.

5.2 Performance Parameters of Inductively-Degenerated Low-Noise Amplifiers

In this section, we will derive adaptivity models for the ID-LNA. This amplifier topology, shown in Fig. 5.2, is a traditional cascode configuration, where Y stands for the load admittance of the amplifier, and L_E and L_B for the degenerative emitter and base inductors, respectively. Performance of this amplifier topology (i.e., gain, noise, and linearity) is characterized. The following analytical models are derived: an input-impedance model, a gain model, and a noise-figure model. Finally, an intuitive linearity model is elaborated.

5.2.1 Input-Impedance Model

The input circuit of the ID-LNA is shown in Fig. 5.3 (base resistance r_B and inductance L_B are not shown). Here, Y_{Π} is the base-emitter admittance (dominated by capacitance C_{Π} for high frequencies), C_{μ} the Miller capacitance, g_m the transconductance of input bipolar transistor Q_1, Y_{L} the input admittance of the cascoding stage (in this case the input admittance of the common-base transistor Q_2), and Y_{E} is the equivalent admittance in series with emitter of transistor Q_1. The transconductances of both transistors are assumed equal.

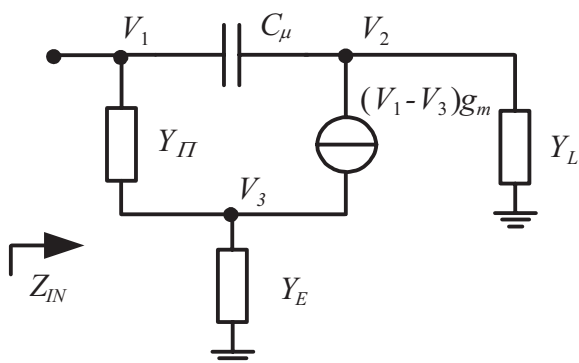

Figure 5.3: Input circuit of an ID-LNA (r_B and L_B not shown).

Applying Kirchoff's current law to the circuit shown in Fig. 5.3, the admittance at the input of transistor Q_1, $Y_{IN\text{-}Q1}$, is calculated as

$$Y_{IN-Q1} = Y_{\Pi}(1 - V_3/V_1) + sC_{\mu}(1 - V_2/V_1). \tag{5.1}$$

With the assumption that at the frequency of interest,

$$\omega C_{\mu} << g_m, \qquad \omega C_{\mu} << Y_L = g_m, \tag{5.2}$$

the admittance $Y_{IN\text{-}Q1}$ becomes

$$Y_{IN-Q1} = Y_{\Pi} \cdot f(Y_E) + sC_{\mu}[1 + g_m f(Y_E)/Y_L], \tag{5.3}$$

where $f(Y_E)$ is the *feedback function* equal to

$$f(Y_E) = 1 - V_3/V_1. \tag{5.4}$$

The input impedance can be estimated from Eq. (5.3) (it accounts for the feedback over capacitance C_{μ}) by determining the function $f(Y_E)$ (which neglects the Miller effect). From Fig. 5.3, the feedback function reads

$$f(Y_E) = \frac{Y_E}{Y_{\Pi} + Y_E + g_m}, \tag{5.5}$$

and hence the input impedance Z_{IN}, neglecting the Miller effect (C_{μ}=0), and taking into account the base inductance L_B (see Fig. 5.2), becomes

$$Z_{IN} = \omega_T L_E + j\left[\omega(L_E + L_B) - \frac{\omega_T}{\omega}\frac{1}{g_m}\right]. \tag{5.6}$$

where ω_T stands for the transit frequency of transistor Q_1.

The condition for the power match at the input of the amplifier can now be derived from Eq. (5.6). The power matching condition can be formulated as follows: the real part of input impedance equals the source resistance (R_S), and the imaginary part of input impedance is canceled (the source impedance is assumed real). This is given by Eqs. (5.7) and (5.8) (transistor's parasitic resistances are neglected).

$$\mathrm{Re}\{Z_{IN}\} = 2\pi f_T L_E = R_S \tag{5.7}$$

$$\mathrm{Im}\{Z_{IN}\} = \omega_0(L_E + L_B) - \frac{\omega_T}{\omega}\frac{1}{g_m} = 0 \tag{5.8}$$

Another option for power matching is discussed in Appendix B.

5.2.2 Gain Model

From Figs. 5.2 and 5.3, and the feedback function given by Eq. (5.5), the effective transconductance g_{EFF} and voltage gain *vg* (from the source) of the ID-LNA can be expressed as

$$g_{EFF} = -g_m \frac{(1 - V_3/V_1)}{1 + Y_\Pi / Y_S(1 - V_3/V_1)} = -g_m \frac{f(Y_E)}{1 + Y_\Pi / Y_S f(Y_E)}, \tag{5.9}$$

$$vg = -g_m Z \frac{(1 - V_3/V_1)}{1 + Y_\Pi / Y_S(1 - V_3/V_1)} = -g_m Z \frac{f(Y_E)}{1 + Y_\Pi / Y_S f(Y_E)}, \tag{5.10}$$

where Y_S represents the total admittance between the source generator and base, and *Z* is the load impedance.

For the input power match given by conditions (5.7) and (5.8), the effective transconductance and the voltage gain of the ID-LNA become

$$g_{EFF} = -\frac{g_m}{Y_\Pi}\frac{1}{Z_{IN} + R_S} = -\frac{1}{2R_S}\frac{\omega_T}{\omega}, \tag{5.11}$$

$$|vg| = \left|\frac{g_m}{Y_\Pi}\right| \frac{Z}{Z_{IN} + R_S} = \frac{1}{2}\frac{\omega_T}{\omega}. \tag{5.12}$$

For the sake of simplicity, the source and load impedances are assumed identical $Z=R_S$.

It is convenient to relate the performance parameters of ID-LNAs to the ratio ω_T/ω, as it establishes a direct relationship between the gain and other performance parameters (e.g., noise figure). Eq. (5.13) refers to this ratio as *x*,

$$x = \frac{\omega_T}{\omega}. \tag{5.13}$$

The voltage gain now transforms into

$$|vg| = \frac{1}{2}x. \tag{5.14}$$

5.2.3 Noise-Figure Model

In the following sections, we will calculate the noise-related parameters that are used for derivation of amplifier adaptivity models. These are the noise factor (F), the optimum source resistance ($R_{S,OPT}$) providing minimum noise factor, the minimum noise factor (F_{MIN}) (see Chapter 2), and the optimum of the minimum noise-factor ($F_{OPT\text{-}MIN}$; the minimum noise factor under the noise-matched condition $R_S = R_{S,OPT}$).

5.2.3.1 Noise Factor

The noise circuit model of the amplifier is shown in Fig. 5.4, where $\overline{V}_N$ and $\overline{I}_N$ are the equivalent input noise sources of a transistor in common-emitter configuration [6-8].

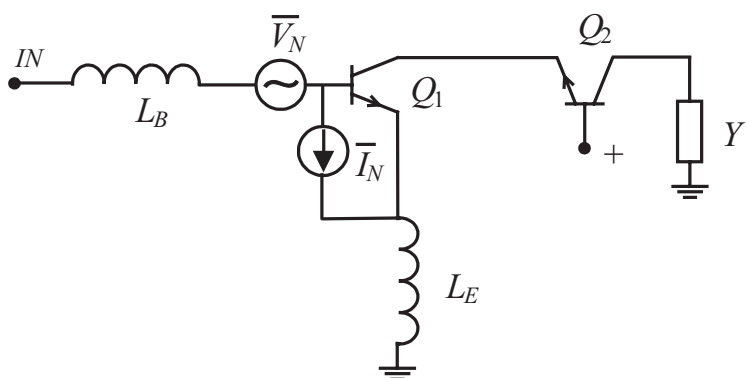

Figure 5.4: Noise model of the ID-LNA.

Applying the Blakesley transformation to the voltage noise source and splitting the current noise source, at the same time keeping track of their polarity, the voltage noise source at the input of the LNA is calculated.

$$\overline{V}_{N,EQ} = 4KTR_S + \overline{V}_N + (Z_S + Z_E + Z_B)\overline{I}_N \tag{5.15}$$

$Z_S=R_S$, $Z_E=j\omega L_E$ and $Z_B=j\omega L_B$.

The equivalent common-emitter transistor noise sources are given by Eqs. (5.16)-(5.18) [7].

$$\overline{V}_N = \overline{V}_B - B_N\overline{I}_C + (r_B + r_E)(\overline{I}_B - D_N\overline{I}_C), \tag{5.16}$$

$$\overline{I}_N = \overline{I}_B - D_N\overline{I}_C, \tag{5.17}$$

$$\overline{I}_B^2 = 2qI_B \quad \overline{I}_C^2 = 2qI_C \quad \overline{V}_B^2 = 4KT(r_B + r_E), \tag{5.18}$$

where $\overline{I}_B$ is the base-current shot noise, $\overline{I}_C$ the collector-current shot noise, $\overline{V}_B$ the base and emitter resistance (r_B+r_E) thermal noise. I_B and I_C are the input transistor base and collector currents, B_N=-1/g_m and D_N=-(1/β_F+$j\omega/\omega_T$) the input transistor transmission parameters [7], K is Boltzmann's constant and T the absolute temperature. Yet, $B_F(\cong\beta_F)$ and β_F are the DC and AC transistor current gain factors, respectively.

With the aid of Eqs. (5.15)-(5.18), the noise-factor model is derived [8].

$$F = \frac{\overline{V}_{N,EQ}^2}{4KTR_S} = 1 + k\delta + \frac{g_m}{2}\delta R_S + \frac{1 + 2k + k^2\delta + \delta L_G^2 - \dfrac{L_G\omega}{2\omega_T}}{2g_mR_S} \tag{5.19}$$

$$k = r_{EF}g_m(1 + 1/\beta_F) \tag{5.20}$$

$$L_G = g_m\omega L_{EB}(1 + 1/\beta_F) \qquad \delta = \frac{1}{\beta_F} + (\frac{\omega}{\omega_T})^2 \tag{5.21}$$

$$r_{EF} = r_B + r_E \qquad L_{EB} = L_E + L_B \tag{5.22}$$

This model is parameterized with respect to power consumption via the *biasing parameter k*, Eq. (5.20). The parameter *k* established the relationship between the amplifier performance and adaptivity figures of merit. Assuming r_{EF} is independent of current and $\beta_F >> 1$, parameter *k* is proportional to the biasing condition, i.e., power consumption, via $k \sim g_m \sim I_C$. Amplifier performance parameters, viz., gain, noise, and linearity, are controlled by the bias current I_C, shown in Fig. 5.2. This allows for adaptation of the amplifier performance to different conditions.

5.2.3.2 Minimum Noise Factor

Source resistance R_S that satisfies condition (5.23),

$$\left.\frac{dF}{dR_S}\right|_{R_S = R_{S,OPT}} = 0\,, \tag{5.23}$$

is the *optimum source resistance* $R_{S,OPT}$, providing an amplifier with the minimum noise factor at the desired frequency (optimum source reactance ($X_{S,OPT}$) and reactive part of input impedance of an ID-LNA are equal: this implies that $X_{S,OPT}$ is canceled [6,9], if the matching condition, Eq. (5.8), is satisfied). From Eq. (5.23), $R_{S,OPT}$ becomes

$$R_{S,OPT} = \frac{1}{g_m\sqrt{\delta}}\sqrt{1 + 2k + k^2\left(\frac{1}{\beta_F} + \frac{1}{x^2}\right) + \delta L_G^2 - \frac{L_G}{2x}}\,. \tag{5.24}$$

Assuming $\beta_F >> 1$ and omitting L_G, while making an acceptable error for the sake of a simpler formulation ($\delta L_G^2 - L_G/(2x) < 1$), Eq. (5.24) simplifies to

$$R_{S,OPT} = \frac{1}{g_m}\sqrt{\frac{1 + 2r_{EF}g_m}{1/\beta_F + (\omega/\omega_T)^2}}\,. \tag{5.25}$$

With the aid of Eqs. (5.19) and (5.24), the *minimum noise factor* is calculated as

$$F_{MIN} \cong 1 + k\delta + \sqrt{\delta(1 + 2k)}\,, \tag{5.26}$$

which for $k\delta << 1$ reduces to

$$F_{MIN} \cong 1 + \sqrt{(1 + 2r_{EF} g_m)[\frac{1}{\beta_F} + (\frac{\omega}{\omega_T})^2]} \,. \tag{5.27}$$

5.2.2.3 Optimum-Minimum Noise Factor

Once the noise-matching parameters are found, viz., the optimum noise resistance and the minimum noise factor, the optimum of the minimum noise factor can be obtained for a certain biasing condition. Namely, solving Eq. (5.28) results in a bias current (i.e., transconductance) providing the optimum of the noise factor under the noise-matched condition (i.e., optimum of F_{MIN}).

$$\left.\frac{dF_{MIN}}{dg_m}\right|_{g_m = g_{m,OPT-MIN}} = 0 \tag{5.28}$$

With the aid of Eqs. (5.27) and (5.28), the condition for the optimum of the minimum noise factor becomes

$$g_{m,OPT-MIN} \cong \omega C_{\Pi} \sqrt{\beta_F \left[1 + \frac{1}{r_{EF} g_{m,OPT-MIN}} \right]} \,. \tag{5.29}$$

The solution for the transconductance $g_{m,OPT\text{-}MIN}$ can be found iteratively from this equation.

The *optimum-minimum source resistance* now equals

$$R_{S,OPT-MIN} = \frac{1}{g_{m,OPT-MIN}} \sqrt{\beta_F (1 + k_{OPT-MIN})} \,, \tag{5.30}$$

where $k_{OPT\text{-}MIN} = r_{EF} g_{m,OPT\text{-}MIN}$.

From Eqs. (5.26)-(5.29), the optimum of the minimum noise factor is derived as

$$F_{OPT-MIN} = 1 + \frac{k_{OPT-MIN}(1 + 2k_{OPT-MIN})}{\beta_F (1 + k_{OPT-MIN})} + \sqrt{\frac{(1 + 2k_{OPT-MIN})^2}{\beta_F (1 + k_{OPT-MIN})}} \,, \tag{5.31}$$

or when simplified

$$F_{OPT-MIN} = 1 + \frac{1 + 2r_{EF} g_{m,OPT-MIN}}{\sqrt{\beta_F (1 + r_{EF} g_{m,OPT-MIN})}}. \quad (5.32)$$

After solving Eq. (5.29) for the optimum transconductance, i.e., optimum current density of a minimum dimension transistor, the final transistor dimensions as well as its current consumption are determined from Eq. (5.24) (e.g., by setting the resistance $R_{S,OPT}$ to a certain value, typically 50Ω). This is because parameters k and ω_T are assumed independent of transistor dimensions for the same current density.

However, the current for the optimum of the minimum noise factor does not coincide with the peak gain for the ID-LNA [9], and therefore if larger gain is desired, the minimum noise factor will not be at its optimum. Moreover, a 50Ω noise match (i.e., $R_{S,OPT}$=50Ω) often requires a large input transistor, and accordingly large current consumption for the determined optimum bias point (see Example 5.1). The choice of a smaller transistor would result in a larger $R_{S,OPT}$ and lower current consumption for the optimum of the minimum noise factor at the cost of the minimum noise factor increased [9]. If a degradation of noise factor is tolerable, a slight increase of the bias current provides a larger gain, and accordingly reduces the cascaded noise factor of a receiver.

5.2.4 Linearity Model

Algebraic expressions describing the third-order intercept point (IP3, linearity performance parameter) of an ID-LNA consist of many multidimensional terms: base-emitter diffusion capacitance, base-emitter junction capacitance, base resistance, emitter degenerative inductance, load impedance, and DC bias current [10]. Even though the dominant nonlinearities can be identified using the Volterra-series method [10-12], the relationships between these parameters and linearity are often not clear to the designer. However, the level of detail required to accurately describe transistor nonlinearity is adequately captured in modern Computer-Aided Design tools.

Some conclusions found in literature are reviewed here [12]. Emitter degeneration improves linearity of common-emitter transistors (i.e., the larger the inductance L_E (see Fig. 5.2), the better the linearity, but the lower the gain). The third-order intermodulation product for an inductively-degenerated common-emitter bipolar stage is inversely proportional to the cube of the DC bias current. When high linearity is desired, the bias current of an ID-LNA should be increased.

Example 5.1:
The introduced amplifier performance models are examined by comparing simulated and calculated performance of an inductively-degenerated LNA.

Referring to a 50GHz SiGe technology and frequency of operation f=2.4GHz, the dimensions of the amplifier transistors are 0.4x5um^2 (20 transistors), the collector current is 7mA, and the calculated inductor values in the emitter and base of the input transistor are L_B=3.2nH and L_E=0.36nH (this is an example of a power consuming 50Ω noise match). The simulation results of the ID-LNA performance are shown in Table 5.1. The results predicted by the calculations are shown in Table 5.2 (given the transistor dimensions, its parameters are determined).

Referring to these results, the validity of the introduced performance models is due. They can be readily used for the estimation of amplifier performance prior to extensive simulations.

Table 5.1: Simulated parameters of the matched ID-LNA.

f_T[GHz]	VG[dB]	$R_{S,OPT}$[Ω]	NF_{MIN}[dB]	$IIP3$[dBm]
26	16	60	1.2	1.5

Table 5.2: Calculated parameters of the matched ID-LNA.

f_T[GHz]	VG[dB]	$R_{S,OPT}$[Ω]	NF_{MIN}[dB]
29.6	15.8	59.3	1

5.3 Adaptivity Models of Low-Noise Amplifiers

Amplifier performance parameters models, Eqs. (5.11), (5.12), (5.25), (5.27), (5.30) and (5.32), are used to derive the following adaptivity figures of merit (adaptivity models; tuning models): noise-factor, gain, linearity, and input-impedance tuning ranges. These figures describe the relationship between performance parameters and power consumption of an ID-LNA: by changing power consumption, the noise factor, input impedance, gain, and linearity of amplifiers can be adapted to different operating conditions (e.g., different standards).

We will first introduce the gain related tuning parameters. From Eqs. (5.7) and (5.8), the tuning ranges of the real (*RITR*) and the imaginary part (*IITR*) of

the ID-LNA input impedance, for a $k/k_{OPT\text{-}MIN}$ times change in a biasing condition (i.e., power consumption), are found to be

$$RITR(k,k_{OPT-MIN}) = (\frac{x}{x_{OPT-MIN}} - 1)R_S, \tag{5.33}$$

$$IITR(k,k_{OPT-MIN}) = -\frac{x}{g_m} + \frac{x_{OPT-MIN}}{g_{m,OPT-MIN}}, \tag{5.34}$$

where index OPT-MIN refers to optimum-minimum condition (5.29).

The *voltage-gain tuning range* (*vgTR*), for the same power-consumption range ($PCR=k/k_{OPT\text{-}MIN}$), can be found from Eq. (5.12) as

$$vgTR(k,k_{OPT-MIN}) = \frac{x}{x_{OPT-MIN}}. \tag{5.35}$$

On the other hand, the noise related tuning parameters, being optimum noise-resistance tuning range (*RSTR*) and *optimum noise-factor tuning range* (*FTR*), can be found from Eqs. (5.25) and (5.30) as well as Eqs. (5.27) and (5.32), respectively.

$$RSTR(k,k_{OPT-MIN}) = \frac{k_{OPT-MIN}}{k}\sqrt{\frac{1+2k}{\beta_{F,OPT-MIN}(1+k_{OPT-MIN})(\beta_F^{-1}+x^{-2})}} \tag{5.36}$$

$$FTR(k,k_{OPT-MIN}) = \frac{1+\sqrt{(1+2k)(\beta_F^{-1}+x^{-2})}}{1+(1+2k_{OPT-MIN})/\sqrt{\beta_{F,OPT-MIN}(1+k_{OPT-MIN})}} \tag{5.37}$$

From the discussion of the previous section, the linearity parameter (*IIP*3) increases roughly by 5dB [12,13] when bias current is doubled in an ID-LNA.

In order to determine the range of adaptivity, the maximum and the minimum values of the biasing parameter k must be determined.

Accordingly, the minimum biasing point $I_{C,LOW}(k_{LOW})$ depends on both LNA and receiver *system specifications*: it is the power level that provides acceptable dynamic range and sensitivity of a complete system, with satisfactory noise figure, voltage gain and linearity of the amplifier. This mode of operation can be chosen when environmental (channel) conditions

improve, i.e., a receive desired signal is stronger and interference signals are weaker.

On the other hand, the maximum biasing point $I_{C,HIGH}$ (k_{HIGH}) depends on receiver worst-case condition specifications as well as the system *power budget*: how much power can be "burned" in the amplifier and receiver. This mode of operation can be chosen when, for example, a receive signal is rather weak.

The introduced adaptivity figures of merit provide a full control over the LNA performance parameters in any mode of operation. These tuning models show how low-noise amplifiers can trade performance for power consumption in an adaptive way. Moreover, tuning models form the basis for the design of LNAs that can operate across multiple standards: multistandard low-noise amplifiers.

Example 5.2:

The introduced adaptivity figures of merit are calculated in this example.

From the elaborated criteria for determining upper and lower bounds of the amplifier operation, the power-consumption ranges are PCR_{LOW}=1/2 and PCR_{HIGH}=2 (with respect to the optimum-minimum biasing point, Eq. (5.29)). Namely, for a 2.2V supply voltage, and 50Ω load impedance, cascoded transistors (see Fig. 5.2) operate in active region for bias currents lower than $I_{C,HIGH}$=14mA (i.e., PCR_{HIGH}=2). On the other hand, $I_{C,LOW}$ is a current level between 0 and the optimum biasing condition $I_{C,OPT\text{-}MIN}$=7mA. For the sake of simplicity, we choose for $I_{C,LOW}$=3.5mA (i.e., PCR_{LOW}=1/2). Note that high power consumption is due to the (close to) simultaneous 50Ω noise and power match in this example. Some design trade-offs are discussed in Section 5.2.3.

Referring to the ID-LNA (Fig. 5.2), an operation frequency f=2.4GHz and dimensions of transistor Q_1 as 20x(0.4x5)um^2, the parameters of the optimum-minimum point are: f_T=29.6GHz, C_{IT}=1.45pF, β_F=105 and r_{EF}=5.2Ω. The simulated (50Ω) power-matching parameters are L_B=2.8nH and L_E=0.28nH.

For a $k_{OPT\text{-}MIN}/k_{LOW}$=2 times reduction and a $k_{HIGH}/k_{OPT\text{-}MIN}$=2 times increase in power consumption, the corresponding tuning ranges of real and imaginary part of the input impedance, voltage gain, optimum noise resistance and optimum noise figure are given by Table 5.3 (for 50Ω source and load impedances). The performance of the optimum-minimum design point resembles the results shown in Tables 5.1 and 5.2, though they refer to somewhat different matching parameters.

Table 5.3: ID-LNA tuning ranges.

Range \ (k, $k_{OPT\text{-}MIN}$)	**(0.7, 1.4)**	**(2.8, 1.4)**
RITR [Ω]	-17	25
IITR [Ω]	12	-12
VGTR [dB]	-2.2	1.3
RSTR [Ω]	11	-15
NFTR [dB]	0.05	0.15

Altogether, over the whole range of the operation, i.e., 6dB change in power-consumption, the change in $Re\{Z_{IN}\}$ is around 40Ω, voltage gain around 3.5dB, noise figure around 0.15dB, and *IIP*3 around 10dB. Tuning ranges from Table 5.3 are indicated in Fig. 5.1.

To illustrate the relationships between the amplifier performance parameters and adaptivity models, an LNA *K-loop* diagram is shown in Fig. 5.5 [14] (a K-rail diagram with a "loop" formed between points 0 and 6). We will map different design requirements (resulting from different operating conditions or different standards) onto the design space of this diagram, and show how adaptivity can be employed to satisfy variable amplifier specifications.

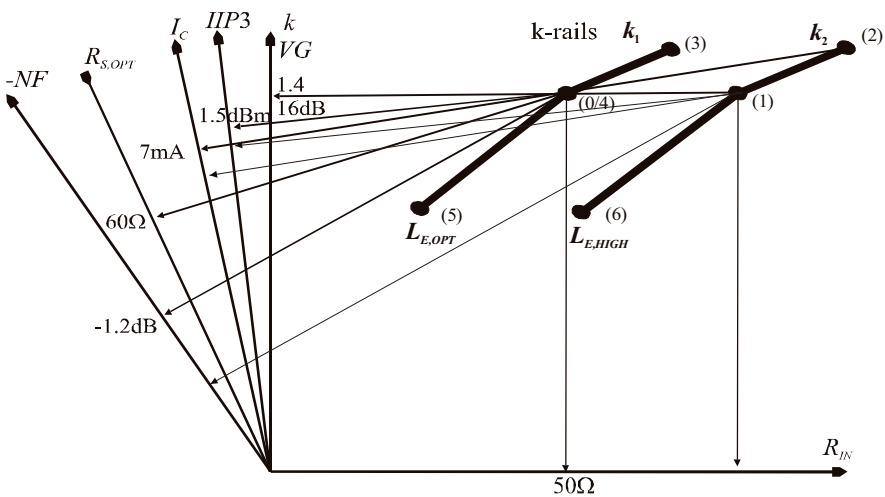

Figure 5.5: An LNA K-loop diagram.

The diagram in Fig. 5.5 has two rails (k_1 and k_2) that correspond to different dimensions of amplifier input transistors and accordingly different power-matching degenerative inductances: $L_{E,\mathrm{OPT}}$ is a low-impedance (e.g., 50Ω source) power-matching inductance with the optimum-minimum noise figure of the ID-LNA (i.e., its input transistor) at point (0); $L_{E,HIGH}$ is a large-impedance (e.g. 100Ω) power matching inductance with the optimum of the minimum noise figure at point (1). We assume that load impedances equal source impedances in both situations.

Let us focus on three characteristic points of the diagram, points (0), (1) and (2). Compared to noise and power matched point (0) (see Example 5.1), operating at point (1) has an advantage of lower power consumption and rather same voltage gain (Eq. (5.14)), at the cost of slightly degraded noise figure and worse linearity [9]. This low-power mode of operation can be chosen when a front-end receive signal is rather weak, necessitating a higher gain and a lower over-all noise figure.

On the other hand, operating at point (2) can be chosen when better linearity is required at the cost of increased power consumption compared to point (1). This design choice provides larger gain, and somewhat worse noise figure compared to design point (1) [9].

Operating at point (2) can be a design choice for the linearity (and power) demanding WCDMA standard, whereas point (6) can be a choice for the noise and linearity (and accordingly power consumption) relaxed DECT standard.

The K-loop diagram and Eqs. (5.33)-(5.37) provide control over amplifier performance parameters for designer. Given the tuning ranges (interpreted as tolerable performance degradations for single standard applications or as requirements for multistandard applications), the relationships between power consumption and performance parameters can be determined.

5.4 Conclusions

The varying nature of radio channels, and accordingly varying operating conditions of receiver circuits promote a design concept that responds to such changes by simultaneously offering power savings. The introduced amplifier adaptivity figures of merit show how low-noise amplifiers can trade performance for power consumption in an adaptive environment. It has also been shown what are the extremes of the performance tuning ranges within which a low-noise amplifier is still functional.

Furthermore, the presented impedance, gain, noise, and linearity models and the K-rail diagrams provide full control for designers over the amplifier performance parameters for a number of operating conditions.

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Chapter 6

ADAPTIVE VOLTAGE-CONTROLLED OSCILLATORS

Concept of designing for adaptivity of oscillators is introduced in this chapter. It establishes a procedure for performance characterization of adaptive oscillators with qualitative and quantitative descriptions of the relationships and trade-offs between oscillator performance parameters.

The organization of the chapter is as follows. The adaptivity of oscillators is discussed in the following section. Section 6.2 introduces an adaptive voltage-controlled oscillator (VCO). The phase-noise model of the adaptive oscillator is then described in Section 6.3. Section 6.4 discusses the phase-noise performance of the adaptive VCO. Adaptivity figures of merit, viz., phase-noise tuning range and frequency-transconductance sensitivity, are derived in Section 6.5. The subject of Section 6.6 is a comprehensive performance characterization of voltage-controlled oscillators by means of K-rail diagrams. An oscillator design problem is discussed in Section 6.7.

6.1 Adaptivity Phenomena of Oscillators

The importance of low-voltage and low-power design has resulted in circuits operating at the very edge of the required performance. Generally, analog receiver circuit designs are aimed at fulfilling a set of specifications resulting from specific, worst-case radio-channel conditions. However, radio channels are not fixed but variant. This should be taken into account in the design of receiver circuits. Concept of *designing for adaptivity* [1] is suitable for mobile equipment that supports various services and operates with variable workloads in a variety of environments.

Designing for adaptivity of oscillators encompasses phase-noise tuning and frequency-transconductance tuning phenomena. These are elaborated in the remainder of this section.

6.1.1 Phase-Noise Tuning

If the radio-channel conditions improve (or a relaxed communication standard is active), poorer phase noise of oscillators may be tolerable, leading to power savings. Responding to such a new situation, designing for adaptivity appears to be a solution as a standard, fixed design [2] is "blind" and "deaf" for volatile specifications set by communication systems.

By trading phase noise for power consumption, oscillators and oscillating systems can be adapted to varying conditions and satisfy the requirements of the complete receiver as well. The concept of phase-noise tuning [1] shows explicitly how phase noise and power consumption trade between each other in an adaptive way.

The analytical description of this adaptivity phenomenon is presented later in this chapter.

6.1.2 Frequency-Transconductance Tuning

For low-power voltage-controlled oscillators a design is usually aimed at a loop gain slightly larger than the necessary minimum of one (e.g., two). In such cases, an increase in the capacitance of the oscillator's LC-tank varactor in order to lower the oscillation frequency results in an increase of the effective tank conductance. If the design is "fixed" rather than adaptive, the oscillation condition deteriorates as the loop gain is lowered. Accordingly, this can bring a receiver to a halt, as there might be no oscillations.

In situations where power consumption is of less concern than oscillator phase noise, the repercussions are different but not less detrimental. The oscillation condition is rather relaxed, as the loop gain can be much larger than two. However, the voltage swing over the LC-tank will be reduced due to the increase in the effective tank conductance (increased varactor capacitance), resulting in potentially poorer phase-noise performance.

In both of these situations, the oscillator could still fulfill the requirements if the bias conditions of the transconductor transistors were adapted (i.e., modified in a controlled fashion). Thus, *frequency-transconductance* (C-g_m) tuning [1] is the control mechanism compensating for the change in the VCO LC-tank characteristic (conductance is changed due to frequency tuning) by varying the oscillator's bias conditions (e.g., transconductance g_m).

A figure of merit related to this adaptivity phenomenon is analytically described in Section 6.5.

6.2 An Adaptive Voltage-Controlled Oscillator

The quasi-tapped (QT) bipolar VCO [3], shown in Fig. 6.1, is used to implement the adaptive oscillator. It consists of a resonant LC tank and a cross-coupled transconductance amplifier (Q_1, Q_2) The bias tail-current source provides current I_{TAIL} and includes degenerative impedance Z_D.

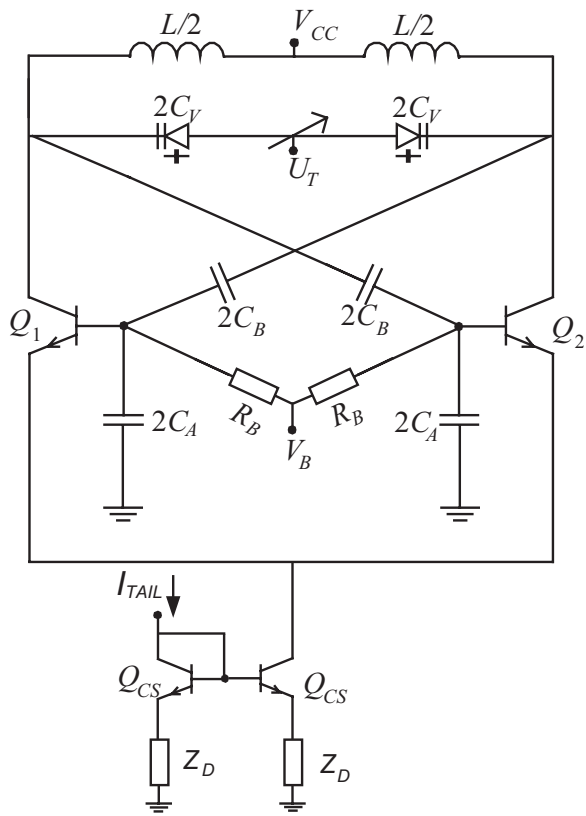

Figure 6.1: An LC-oscillator.

The relationships between the parameters of the oscillator are summarized in Table 6.1 (and given equation numbers). L is the tank inductance, C_V the tank varactor capacitance, R_L and R_C model the inductors and varactors series losses, G_{TK} the effective tank conductance, n the quasi-tapping factor, $-G_M$ the

small-signal transconductance of the active part of the oscillator, $-G_{M,TK}$ the small-signal conductance seen by the LC-tank, k the small signal loop gain, g_m the transconductance of bipolar transistors, C_{Π} the base-emitter capacitance of the transistors Q_1 and Q_2, ω_0 the oscillation angular frequency and V_T the thermal voltage.

The oscillator in Fig. 6.1 is the second-order negative resistance oscillator with a feedback via capacitors C_A and C_B between the resonant LC-tank and the transconductor. The capacitive feedback has a manifold role. First, it maximizes the voltage swing across the LC tank, while keeping active devices Q_1 and Q_2 far from heavy saturation. Moreover, freedom to set base bias V_B lower than the supply voltage V_{CC} allows for an even larger tank voltage, approaching the voltage swing of a CMOS implementation. Capacitors C_A and C_B allow direct coupling of the oscillation signal (oscillator) to the interfacing circuitry, obviating the need for decoupling capacitors. Finally, they determine the performance (power consumption, frequency, phase noise) of the oscillator together with the other elements in the *ac* signal path.

Table 6.1: Parameters of the LC-VCO.

parameter	expression	equation
G_{TK}	$\frac{R_L}{(\omega_0 L)^2} + R_C(\omega_0 C_V)^2$	(6.1a)
n	$1 + \frac{C_A + C_{\Pi}/2}{C_B}$	(6.1b)
G_M	$\frac{g_m}{2}$	(6.2a)
$G_{M,TK}$	$\frac{G_M}{n}$	(6.2b)
k	$\frac{G_{M,TK}}{G_{TK}}$	(6.2c)
g_m	$\frac{I_{TAIL}}{2V_T}$	(6.2d)
L_{TOT}	L	(6.3a)
C_{TOT}	$C_V + \frac{C_A C_B}{C_A + C_B}$	(6.3b)
ω_0	$1/\sqrt{L_{TOT} C_{TOT}}$	(6.3c)

A simplified model of LC oscillator is shown in Fig. 6.2. The oscillation condition is satisfied when the equivalent LC-tank loss conductance G_{TK} is compensated by the equivalent negative small-signal transconductance of the active part $-G_M$, after being transformed to the resonating tank over the capacitive divider, i.e., $G_{M,TK}=G_{TK}$. This condition is often referred to as the start-up condition of the oscillations. The safe operation of the oscillator is guaranteed for $G_{M,TK}/G_{TK}=k>1$ [4].

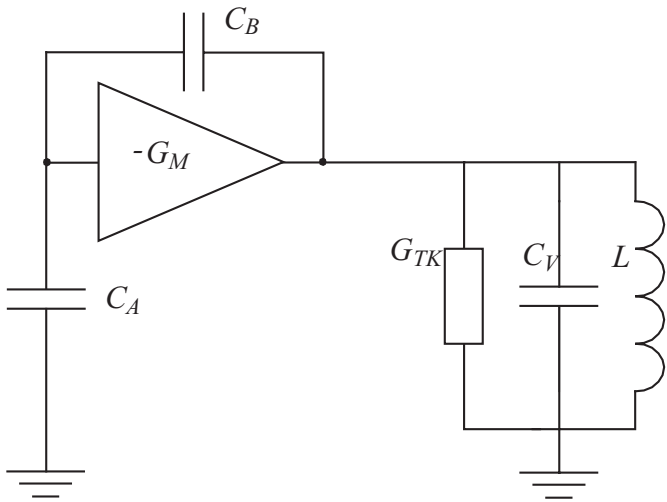

Figure 6.2: Simplified model of the LC oscillator with a capacitive divider.

6.3 Phase-Noise Model of LC Voltage-Controlled Oscillators

Phase noise ($\mathcal{L}$) of an oscillator is defined as the ratio of the phase-related noise power in a 1Hz bandwidth at an offset frequency $f_0+\Delta f$ to the carrier power [5],

$$\mathcal{L}=\frac{\overline{V}^2_{TK,TOT}}{v_S^2/2} \qquad \overline{V}^2_{TK,TOT}=\left|Z(f_0+\Delta f)\right|^2\overline{I}^2_{TK,TOT}=\frac{\overline{I}^2_{TK,TOT}}{\left(4\pi C_{TOT}\Delta f\right)^2} \quad . \quad (6.4)$$

$\overline{V}^2_{TK,TOT}$ and $\overline{I}^2_{TK,TOT}$ stand for the total phase-related voltage and current noise spectral densities at the output of the oscillator (LC-tank), $Z(f_0+\Delta f)$ is the equivalent tank impedance at an offset frequency Δf from the resonant frequency f_0, and v_S is the amplitude of the voltage swing across the LC-tank.

The noise sources of the LC-VCO with an undegenerated tail-current source (see Fig. 6.3) are given in Table 6.2. These are the tank conductance noise $\overline{I}_{GT}$, the base-resistance (r_B) thermal noise $\overline{V}_B$, the collector $\overline{I}_C$, and the base $\overline{I}_B$ current shot-noise sources, and the equivalent output current noise $\overline{I}_{CS}$ source of the current source transistor Q_{CS} (Eqs. (6.5-6.7)).

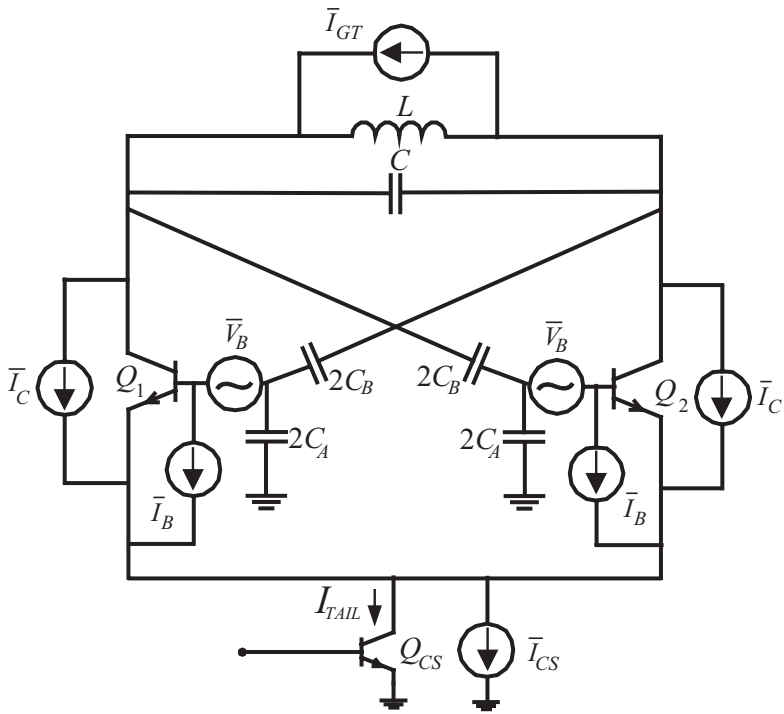

Figure 6.3: LC-VCO noise sources.

I_C and I_B stand for the collector and base currents, $g_{m,CS}$ is the transconductance and $r_{B,CS}$ the base resistance of transistor Q_{CS}, and K Boltzmann's constant.

Table 6.2: LC-VCO noise parameters.

parameter	expression	equation
$\overline{I}_{GT}^2$	$4KTG_{TK}$	(6.5)
$\overline{V}_B^2$	$4KTr_B$	(6.6a)
$\overline{I}_C^2$	$2qI_C$	(6.6b)
$\overline{I}_B^2$	$2qI_B$	(6.6c)
$\overline{I}_{CS}^2$	$4KT\frac{g_{m,CS}}{2}\left[1+2r_{B,CS}g_{m,CS}\right]$	(6.7)

The transformations of the indicated noise sources to the LC-tank ($\overline{I}_{TK,TOT}$) must be known for estimation of the phase noise of the VCO under consideration. Considering the transconductor as a nonlinear voltage-to-current converter (limiter) [6] allows for the inclusion of all the noise generating mechanisms in the oscillator. Namely, phenomena such as switching of the transconductor noise and the noise of the tail-current source, both resulting in the folding of noise [6,7], can be comprehended.

6.3.1 Time-Varying Transfer Function

The nonlinear voltage-to-current transfer function (referred to the LC-tank) of the transconductor and its equivalent time-varying transconductance in the presence of a large driving signal are shown in Fig. 6.4 [6].

As long as limiting of the oscillation signal (v_{IN}) doesn't occur, the transfer function of an accompanying small signal has a constant value, g. When limiting occurs, the small-signal (e.g., noise) gain reduces to zero. If the large signal oscillation period is $1/f_0$, the period of a small signal time-varying gain (g_{IN}) is $1/(2f_0)$. The gain g from the bases to collectors of the transconductor Q_1-Q_2 is $g_m/2$.

Let us first estimate the duty cycle d (Fig. 6.4) of the time-varying gain, before evaluating the contribution of the various noise sources to the phase noise of the oscillator.

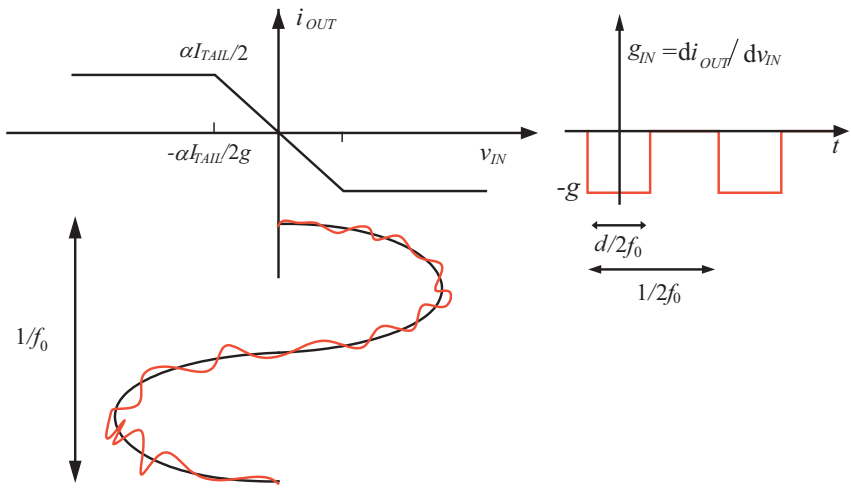

Figure 6.4: *V*-to-*I* and time-varying transfer functions.

If $v_{S,B}$ is the voltage swing of the oscillation signal across the bases of the transconductor, and $\pm 2\alpha V_T$ is the linear region of the transconductor, the duty cycle of the time-varying gain can be expressed as

$$d = \frac{2}{\pi}\arcsin\left(\frac{2\alpha V_T}{v_{S,B}}\right). \tag{6.8}$$

With the aid of Eq. (6.2), the voltage swing across the tank (a product of the tank resistance $1/G_{TK}$ and the first Fourier coefficient of the tail current I_{TAIL}) equals

$$v_S = \frac{8}{\pi} nkV_T = nv_{S,B}, \tag{6.9}$$

where k is for the small-signal loop gain of the oscillator and $v_{S,B}$ is the voltage swing of the oscillation signal across the bases of the transconductor transistors. Assuming a 100mV ($\pm 2V_T$) transconductor linear region [8] and a large loop-gain value ($k>>1$), the duty cycle d can be approximated as

$$d = \frac{1}{2k}. \tag{6.10}$$

6.3.2 Base-Resistance Noise Contribution

The noise from transistors Q_1 and Q_2 (both contributions) is switched on/off with the frequency of the time-varying gain g_{IN} ($2f_0$). Consequently, noise folding occurs, i.e., noise from a number of frequencies is converted into the noise at one frequency. The harmonic components of the noise from the base resistance (multiples of f_0) and the harmonic components of the time-varying transconductor gain are shown in Fig. 6.5.

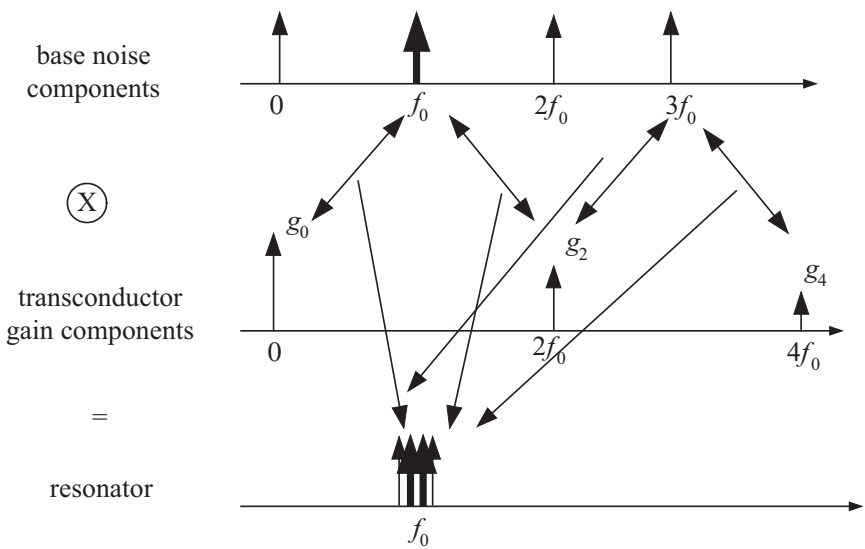

Figure 6.5: Base resistance noise folding.

As a result of the noise folding, the base noise ($2r_B$) at odd multiples of the oscillation frequency is converted to the LC-tank at the resonance frequency, as given by Eqs. (6.11) and (6.12).

$$\overline{I}^2_{TK,VB} = 2\left(g_0^2 + 2\sum_{m=1}^{\infty} \left| g_{2m} \right|^2 \right) \overline{V}^2_B \tag{6.11}$$

$$\sum_{m=-\infty}^{\infty} \left| g_{2m} \right|^2 = \frac{1}{T_2} \int_{-T_2/2}^{T_2/2} g_{IN}^2(t) dt \tag{6.12}$$

g_{2m} are the (complex) Fourier coefficients and T_2 is the period of the transfer function g_{IN} ($g=g_m/2$).

With the aid of Eq. (6.2), the base resistance noise density transferred to the LC-tank equals

$$\bar{I}^2_{TK,VB} = 4KT \cdot kn^2 r_B G^2_{TK} . \tag{6.13}$$

Now, the phase-noise related contribution of the base-resistance noise at the output (LC-tank) becomes

$$F_{TK,VB} = \frac{\bar{I}^2_{TK,VB}}{2KTG_{TK}} = nck \tag{6.14}$$

where $c=r_B g_{ms\text{-}up}$ and $g_{ms\text{-}up}$ is the start-up (k=1) small-signal transconductance of the active devices Q_1 and Q_2. This result is obtained from equality (6.15)

$$r_B G_{TK} = \frac{c}{2n}, \tag{6.15}$$

that is derived from Eq. (6.2).

6.3.3 Transconductor Shot-Noise Contribution

By splitting the current noise sources, the collector and base current shot noise transform to the resonator as given by Eq. (6.16).

$$\bar{I}^2_{TK,ICB} = \frac{\bar{I}^2_C}{2} d + \frac{1}{n^2}(1-\frac{d}{2})\bar{I}^2_B \tag{6.16}$$

The noise sources of both transistors are active for a fraction d of the period T_0 ($1/f_0$), whereas for the rest of the period the noise sources of only one transistor are active. With the aid of Eqs. (6.6), (6.10) and (6.16), the contribution of the transconductor's shot noise sources now becomes

$$F_{TK,ICB} = \frac{\bar{I}^2_{TK,ICB}}{2KTG_{TK}} = \frac{n}{2}. \tag{6.17}$$

The same result would be obtained if averaging of the equivalent shot noise were considered. Namely, the transconductor shot noise when both transistors are active turns on and off with the rate of the transfer function g_{IN} (Fig. 6.4 with g=1). Referring to Eq. (6.12), this would lead to Eq. (6.17) as well.

6.3.4 Tail-Current Source Noise Contribution

The harmonic components of the equivalent tail-current noise (multiples of f_0) and the harmonic components of an ideal switch (square-wave time function) are shown in Fig. 6.6.

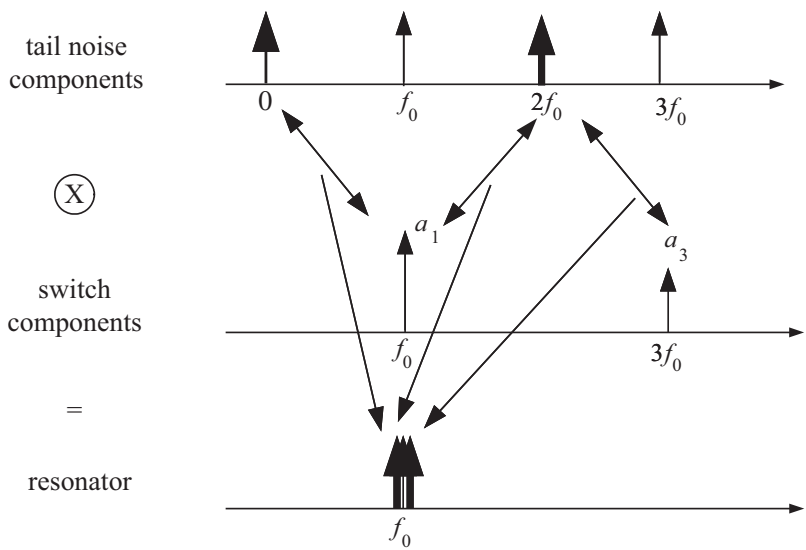

Figure 6.6: Tail-current noise folding.

The noise of the biasing current source is modulated by the oscillator switching action. Therefore, the tail-current noise (TCN) around even multiples of the resonant frequency is folded back to the resonator at the oscillation frequency, as approximately given by Eq. (6.18).

$$\overline{I}^2_{TK,CS} = \frac{1}{4} 2 \sum_{m=0}^{\infty} \left| a_{2m+1} \right|^2 \overline{I}^2_{CS} \tag{6.18}$$

Coefficients a_{2m+1} relate to the (complex) harmonic components of the square-wave. The factor ¼ originates from the active part transistors' load impedance ($1/2G_{TK}$).

Combining Eqs. (6.7) and (6.18), using the weights of the square-wave amplitude components [9],

$$\frac{\pi^2}{8} = 1 + \frac{1}{3^2} + \frac{1}{5^2} + \frac{1}{7^2} \ldots , \tag{6.19}$$

and taking into account the phase-noise contributing components only [6,10], the tail-current noise converts to the resonant LC-tank as

$$\overline{I}^2_{TK,CS} \cong KTg_m \left[1 + 2r_B g_m\right]/2 . \tag{6.20}$$

Finally, with the aid of Eqs. (6.2), (6.15) and (6.20), the contribution of the tail-current noise to the phase noise becomes

$$F_{TK,CS} = \frac{\overline{I}^2_{TK,CS}}{2KTG_{TK}} \cong k(\frac{n}{2} + nkc) . \tag{6.21}$$

6.3.5 Total Oscillator Noise

When assumed to be uncorrelated, all noise sources, viz., the tank conductance noise, the base resistance noise, the transconductor shot noise and the tail-current noise add to the equivalent output noise, as given by Eq. (6.22),

$$\overline{I}^2_{TK,TOT} = \overline{I}^2_{TK,GT} + \overline{I}^2_{TK,VB} + \overline{I}^2_{TK,ICB} + \overline{I}^2_{TK,CS} , \tag{6.22}$$

where $\overline{I}^2_{TK,GT} = 2KTG_{TK}$ is the phase-related noise power from the LC-tank. The noise factor F of the oscillator now equals

$$F = \frac{\overline{I}^2_{TK,TOT}}{2KTG_{TK}} = 1 + \frac{n}{2} + nck + k(\frac{n}{2} + nkc) . \tag{6.23}$$

It is important to note that Eq. (6.23) represents *worst-case* noise factor of the bipolar oscillator under consideration, thereby overestimating its phase noise. The loop-gain related contributions, viz., the base-resistance noise contribution of the transconductance cell, Eq. (6.14), and the base-resistance and the collector-current noise contributions, Eq. (6.21), of the tail-current source, are calculated without accounting for any bandwidth limitations. Namely, limited bandwidth of the devices and noise sources of the transconductor and tail-current source alleviate the effect of noise folding: noise power around higher harmonic components is expectedly small. Moreover, finite transconductor switching time (thus not an ideal square-wave function) reduces additionally the TCS noise contribution. Deviations of the calculated phase-noise contributions from those of a "real" oscillator design can be estimated using oscillator simulators.

However, the results of previous sections are intuitive and describe qualitatively a rather complex phase-noise generating mechanism in oscillators. The formulations obtained are amenable for making qualitative design decisions as they describe the oscillator phase-noise performance using electrical parameters.

For elaborate phase-noise modeling, we refer you to [6,10,11].

We observe from Eq. (6.23) that the contribution of the tail-current source noise to the phase noise of the voltage-controlled oscillator (Fig. 6.3) is larger than all other contributions together [12,13]. Denoting the contribution of the active part noise and the LC-tank resistance noise as $1+A_{AP}$, and the contribution of the tail-current noise as A_{CS}, we define the phase-noise difference (*PND*) as the ratio of the oscillator noise factors with noisy and noiseless tail-current source.

$$PND = 1 + \frac{A_{CS}}{1 + A_{AP}} \tag{6.24}$$

Referring to Eqs. (6.14), (6.17) and (6.21), the *PND* of the oscillator under consideration is

$$PND = 1 + \frac{k(\frac{n}{2} + nck)}{1 + \frac{n}{2} + nck}. \tag{6.25}$$

The *PND* is used to quantify the degradation of the phase noise due to the noise from the tail-current source. For example, if n=1.4 and c=0.1, then for a

loop gain k=10, PND=7.8: the tail-current source degrades the phase-noise performance of the VCO by around 9dB as calculated from Eq. (6.25).

6.3.6 Resonant-Inductive Degeneration of Tail-Current Source

It has been shown in the previous section that the contribution of noise from the bias tail-current source around even multiples of the oscillation frequency to the phase noise of the oscillator is larger than all other oscillator noise contributions combined.

Resonant-inductive degeneration [14] is a design procedure proposed to minimize the noise contribution of the oscillator tail-current source. It relies on forming a resonance between the inductor (L_{RID}) in the emitter of the tail-current source transistor Q_{CS} and its base-emitter capacitance $C_{\Pi,CS}$ at $2f_0$, as shown in Fig. 6.7. The fact that the tail-current noise around twice the oscillation frequency ($2f_0$) has the largest contribution to the phase noise of the oscillator, after being converted to the resonating LC-tank by the switching of transconductor Q_1-Q_2 (see Fig. 6.1), stems for the resonant frequency chosen.

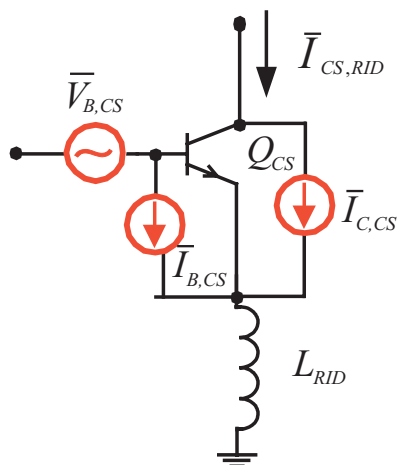

Figure 6.7: Resonant-inductive degenerated tail-current source transistor and its noise sources.

The resonant-inductive degeneration results in reduction of contributions of base-resistance thermal noise and collector-current shot noise of bias TCS to the oscillator phase noise. The high impedance in the emitter of Q_{CS} at resonance reduces the transconductance and gain from base-resistance thermal noise to the output, and impedes the flow of collector-current shot noise, making these noise contributions negligible.

We will determine the performance of resonant-inductive degeneration by calculating transfer functions from the base-resistance noise, base-current shot noise and collector-current shot noise sources to the output of the current source using a detailed schematic shown in Fig. 6.8. Then, using superposition, total output noise of the tail-current source with resonant-inductive degeneration will be found, and formulations for the oscillator noise factor adapted.

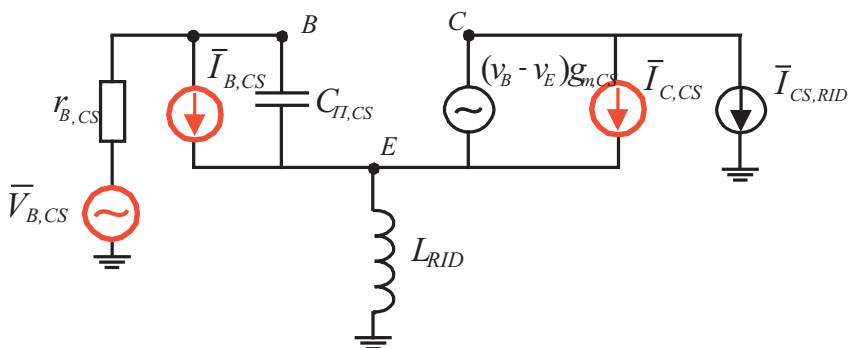

Figure 6.8: Circuit of a tail-current source with resonant-inductive degeneration.

In Fig. 6.8 are shown the base-resistance noise source $\bar{V}_{B,CS}$, base-current shot noise source $\bar{I}_{B,CS}$, and collector-current shot-noise source $\bar{I}_{C,CS}$. $\bar{I}_{CS,RID}$ models a total output current noise source of the TCS to be determined. The corresponding noise densities are given by Eqs. (6.26-6.28).

$$\bar{V}^2_{B,CS} = 4KTr_{B,CS} \tag{6.26}$$

$$\bar{I}^2_{C,CS} = 2qI_{TAIL} = 4KTg_{m,CS}/2 \tag{6.27}$$

$$\overline{I}^{2}_{B,CS} = 2qI_{B,CS} = 4KTg_{m,CS}/(2\beta_F) \tag{6.28}$$

6.3.6.1 Base Resistance Noise Transformation of the Resonant-Inductive Degenerated Tail-Current Source

The circuit of Fig. 6.8 resembles a circuit of an inductively-degenerated low-noise amplifier. Unlike an LNA, where noise at the input of a degenerated transistor is minimized, minimum of noise at the output of a degenerated transistor matters for a tail-current source in the oscillator of Fig. 1.

From Chapter 5 and [15,16], the input impedance of an inductively degenerated transistor is given as

$$Z_{IN}(f) = 2\pi f_{T,CS}L_{RID} + j\left[2\pi fL_{RID} - \frac{f_{T,CS}}{f}\frac{1}{g_{m,CS}}\right]. \tag{6.29}$$

The contribution of the noise from the base resistance to the output current noise density $\overline{I}_{CS,RID}$ of the degenerated tail-current source is given by Eq. (6.30).

$$\frac{\overline{I}_{CS,RID}}{\overline{V}_{B,CS}}(f) = -\frac{1}{Z_{IN}(f)}\frac{\omega_{T,CS}}{\omega} = \frac{1}{\omega_{T,CS}L_{RID} + j\omega L_{RID} + 1/j\omega C_{\Pi,CS}}\frac{\omega_{T,CS}}{\omega} \tag{6.30}$$

For the resonance at $2f_0$, the imaginary part of the input impedance is set to zero. Then,

$$R_{IN}g_{m,CS} = \left(\frac{f_{T,CS}}{2f_0}\right)^2, \tag{6.31}$$

where $f_{T,CS}$ is the transit frequency of Q_{CS} and $R_{IN}=2\pi f_T L_{RID}$ is equal to the real part of the impedance at the base of Q_{CS}.

The equivalent transconductance of the RID tail current-source transistor at $2f_0$ now equals (Chapter 5),

$$g_{EQ,CS} \cong -\frac{1}{R_{IN}}\frac{f_{T,CS}}{2f_0}, \tag{6.32}$$

and Eq. (6.30) becomes

$$\frac{\overline{I}_{CS,RID}}{\overline{V}_{B,CS}}(2f_0) = -g_{m,CS}\frac{2f_0}{f_{T,CS}}. \tag{6.33}$$

This suggests that a reduction of the tail-current source base-resistance thermal noise is possible for $2f_0/f_{T,CS}<1$. It is interesting to note that seen from base of the transistor Q_{CS}, inductor L_{RID} and base-emitter capacitor C_{Π} form a series-resonant circuit (see the denominator of Eq. (6.30)).

6.3.6.2 Base- and Collector-Current Shot Noise Transformations of the Resonant-Inductive Degenerated Tail-Current Source

The RID tail-current source transistor Q_{CS} operates in a common-base-like configuration at a resonance at twice the oscillation frequency. Referred to the output of transistor Q_{CS}, we expect to see the collector-current shot noise suppressed and the base-current shot noise present. This intuitive observation can be analytically confirmed with the aid of Fig. 6.8.

We will first determine the transfer function from collector-current shot noise $\overline{I}_{C,CS}$ to the output of the current source $\overline{I}_{CS,RID}$ by applying superposition (i.e., $\overline{I}_{B,CS}=0$ and $\overline{V}_{B,CS}=0$). In the analysis, we use symbols of noise sources, but consider them as independent AC current/voltage sources.

Let us first determine the gain from $\overline{I}_{C,CS}$ to $\overline{I}_{CS,RID}$. Kirchoff's current law equation for node *E* yields

$$\overline{I}_{C,CS} + g_{m,CS}v_{BE} = \frac{v_E}{sL_{RID}} - j\omega C_{\Pi,CS}v_{BE}, \tag{6.34}$$

where $v_{BE}=v_B-v_E$. Analyzing the *BE* branch of Fig. 6.8, we obtain

$$\frac{v_E}{r_{B,CS}} = -v_{BE}\left(\frac{1}{r_{B,CS}} + j\omega C_{\Pi,CS}\right). \tag{6.35}$$

Substituting Eq. (6.35) into Eq. (6.34), the relationship between the base-emitter voltage v_{BE} and the current $\bar{I}_{C,CS}$ becomes

$$I_{C,CS} = -v_{BE}\left[g_{m,CS} + j\omega C_{\Pi,CS} + \frac{1}{j\omega L_{RID}} + \frac{C_{\Pi,CS} r_{B,CS}}{L_{RID}} \right]. \tag{6.36}$$

From the current-law equation for node *C,*

$$\bar{I}_{CS,RID} = \bar{I}_{C,CS} + g_{m,CS} v_{BE}\,, \tag{6.37}$$

the transfer function from the collector-current noise source to the output of the TCS at $2f_0$ is

$$\frac{\bar{I}_{CS,RID}}{\bar{I}_{C,CS}}(f) = 1 - \frac{g_{m,CS}}{g_{m,CS} + \frac{C_{\Pi,CS} r_{B,CS}}{L_{RID}} + j\omega C_{\Pi,CS} + 1/\, j\omega L_{RID}}\,. \tag{6.38}$$

At the resonance ($2f_0$) between L_{RID} and $C_{\pi,CS}$, this simplifies to

$$\frac{\bar{I}_{OUT,CS}}{\bar{I}_{C,CS}}(2f_0) = 1 - \frac{1}{1 + r_{B,CS} g_{m,CS} (\frac{2f_0}{f_{T,CS}})^2} \cong 0\,. \tag{6.39}$$

As $r_{B,CS}g_{m,CS}$ is a small constant (equals *ck* for $r_{B,CS}$=$2r_B$) compared to $2f_0/f_{T,CS}$<<1, the collector-current shot noise can be suppressed from the output of the TCS using resonant-inductive degeneration.

In a similar manner, the transformation of the base-current shot noise to the output of the TCS is calculated from Fig. 6.8 ($\bar{I}_{C,CS} = 0$ and $\bar{V}_{B,CS} = 0$). The resulting transfer function equals

$$\frac{\bar{I}_{CS,RID}}{\bar{I}_{B,CS}}(f) = \frac{g_{m,CS}}{g_{m,CS} + \frac{C_{\Pi,CS} r_{B,CS}}{L_{RID}} + j\omega C_{\Pi,CS} + 1/\, j\omega L_{RID}}\,, \tag{6.40}$$

or at the resonance ($2f_0$)

$$\frac{\overline{I}_{CS,RID}}{\overline{I}_{B,CS}}(2f_0) = \frac{1}{1 + r_{B,CS} g_{m,CS} (\frac{2f_0}{f_{T,CS}})^2} \cong 1 . \tag{6.41}$$

This implies that the base-current shot noise is transferred completely to the output of the degenerated tail-current source.

It is worth mentioning that the inductor L_{RID} and base-emitter capacitor $C_{\Pi,CS}$ form a parallel-resonant circuit seen from the base- and collector-current noise sources (see the denominators of Eqs. (6.38) and (6.40)).

6.3.6.3 Total Output Noise of the Resonant-Inductive Degenerated Tail-Current Source

Combining the base-resistance noise and the base-current shot noise contributions, Eqs. (6.33) and (6.41), the total output current noise density of the resonant-inductive degenerated tail-current source becomes

$$\overline{I}^2_{CS,RID} = 4kT \frac{g_{m,CS}}{2} \left[0 + (\frac{f_{T,CS}}{2f_0})^2 \frac{1}{\beta} + 2r_{B,CS} g_{m,CS} \right] \left(\frac{2f_0}{f_{T,CS}} \right)^2 . \tag{6.42}$$

The noise factor of the tail-current source with resonant-inductive degeneration now equals

$$F_{TK,CS,RID} = k \cdot \left[\frac{n}{2\beta} \left(\frac{2f_{T,CS}}{f_0} \right)^2 + nkc \right] \left(\frac{2f_0}{f_{T,CS}} \right)^2 , \tag{6.43}$$

which is obtained from Eqs. (6.20) and (6.42), after referring to $2r_{B,CS}=r_B$ for a convenient formulation.

Resonant-inductive degeneration suppresses most effectively tail-current noise around second harmonic of the oscillation frequency by forming a resonance, but also TCS noise from higher harmonics ($4f_0$, $6f_0$, …). The TCS noise around $2f_0$ is responsible for around 70% of the total bias noise, which is reduced by a factor $(f_{T,CS}/2f_0)^2$ after the RID. The smaller portion of the TCS noise (~30%) originates from higher harmonics, which is reduced by forming a high impedance in emitter of the TCS transistor (~$4\omega_0 L_{RID}$ at $4f_0$, $6\omega_0 L_{RID}$ at

$6f_0$, …), that is, gain for thermal base-resistance noise to the output of the TCS is small and the flow of collector-current shot noise impeded for higher harmonics. This allows us to formulate the noise factor of the oscillator with RID TCS by Eq. (6.42).

In order to estimate the improvement achieved, Eq. (6.43) is compared to the output current noise density of the TCS without degeneration, given by Eq. (6.18), and for convenience, Eq. (6.44).

$$\overline{I}_{CS}^2 = 4kT\frac{g_{m,CS}}{2}\left[1+0\bullet(\frac{f_{T,CS}}{2f_0})^2\frac{1}{\beta}+2r_{B,CS}g_{m,CS}\right] \tag{6.44}$$

A comparison between Eqs. (6.42) and (6.44) suggests that by applying resonant-inductive degeneration, the contribution of the tail-current source noise from $2f_0$ is reduced more than $(f_{T,CS}/2f_0)^2$,

$$F_{TK,CS,RID} < \left(\frac{2f_0}{f_{T,CS}}\right)^2 F_{TK,CS}\,, \tag{6.45}$$

as it can be assumed that $\beta > (f_{T,CS}/2f_0)^2$.

For example, a factor 25 reduction of the TCS noise is possible for $f_{T,CS}=10f_0$. Minimizing or eliminating the noise contribution of the TCS improves phase noise performance of the oscillator, or it permits operation at a lower bias current for the same performance of the oscillator under consideration.

Before closing this section, let us inspect Eqs. (6.42) and (6.44) from another perspective. Whereas the base- and collector-current shot noise contributions of the tail-current source are fixed by the supply current, the base-resistance thermal noise is determined by transistor dimensions ($r_{B,CS}$ is inversely proportional to length l of the transistor). Therefore, for the TCS without degeneration, we opt for a large transistor in order to reduce $r_{B,CS}$ and the contribution of the base-resistance noise, as suggested by Eq. (6.44).

However, for the TCS with RID, it is not $r_{B,CS}$, but a ratio $r_{B,CS}/f_{T,CS}^2$ that matters, as implied by Eq. (6.42). As $r_{B,CS}\sim 1/l$ and, for a given current consumption, $f_{T,CS}\sim 1/l$, the ratio $r_{B,CS}/f_{T,CS}^2 \sim l$. Thus, for the TCS with RID, we opt for a small transistor, which provides a larger transition frequency for a given tail current I_{TAIL}, shown in Fig. 6.1.

These findings stress the opposing requirements on the design of a tail-current source with and without degeneration.

6.3.6.4 Noise Factor of Oscillators with Resonant-Inductive Degeneration

The noise factor of the bipolar LC oscillator with resonant-inductive degenerated tail-current source is now obtained from Eq. (6.23), accounting for the reduction of the TCS noise achieved. The noise factor reads

$$F = 1 + \frac{n}{2} + nkc + k \cdot \left[\frac{n}{2\beta} \left(\frac{2 f_{T,CS}}{f_0} \right)^2 + nkc \right] \left(\frac{2 f_0}{f_{T,CS}} \right)^2, \quad (6.46)$$

or in the worst case ($\beta = f_{T,CS}/2f_0$, which is rather unrealistic),

$$F = 1 + \frac{n}{2} + nkc + k\left(\frac{n}{2} + nkc\right) \left(\frac{2 f_0}{f_{T,CS}} \right)^2. \quad (6.47)$$

For $2f_0/f_{T,CS} << 1$, which is readily achievable, the TCS noise contribution can be eliminated.

6.3.6.5 Advantages of Resonant-Inductive Degeneration

Resonant-inductive degeneration suppresses most effectively tail-current noise around second harmonic of the oscillation frequency by forming a resonance, but also TCS noise from higher harmonics ($4f_0$, $6f_0$, …). The total contribution of the bias source to the phase noise is reduced by a factor $(f_{T,CS}/2f_0)^2$ by applying resonant-inductive degeneration.

This noise reduction method is suitable for low-voltage applications, as it requires no D.C. voltage headroom. Moreover, the RID inductor is in the low-nH range for GHz-range applications and, as such, occupies a relatively small chip area when fabricated using the multiple layers of metal available in modern silicon VLSI technologies.

6.3.7 Resistive Degeneration of Tail-Current Source

Resistive degeneration [17] of a tail-current source suppresses the tail-current noise equally at all frequencies, opposite to RID that is frequency selective. Merit of the resistive degeneration is a suppression of the low-frequency

noise, which is converted to the resonator and then phase noise via AM-to-FM conversion in the LC-tank varactor [10].

However, as the resistor in the emitter of the TCS transistor requires D.C. voltage headroom, this method of noise suppression has limited use to systems with large supply voltages only (>3V).

The circuit diagram of the resistive degenerated (RD) TCS is shown in Fig. 6.9. The noise performance of this circuit is discussed next.

The collector-current shot noise of the resistively-degenerated TCS is suppressed while the base-current shot noise is transferred to the output of the current source, as was the case with the RID TCS. Moreover, the base-resistance and the degenerative-resistor (R_{RD}) noise sources are transferred to the output of the current-source transistor with the equivalent transconductance $g_{EQ,CS}=1/R_{RD}$, assuming $R_{RD}>>1$.

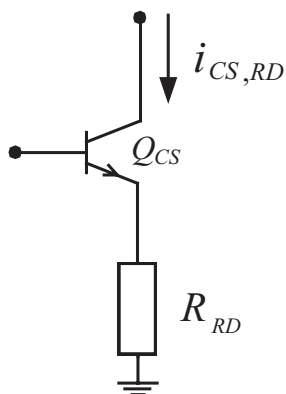

Figure 6.9: Resistive-degenerated tail-current source.

Accounting for the contributions of the base-resistance noise, base-current shot noise and degenerative resistor noise, the output current-noise density of the RD TCS equals

$$\bar{I}^2_{CS,RD} = 4KT\frac{g_{m,CS}}{2}\left[\frac{1}{\beta_F} + 2r_{B,CS}\frac{1}{g_{m,CS}R_{RD}}\left(\frac{1}{r_{B,CS}} + \frac{1}{R_{RD}}\right)\right]. \qquad (6.48)$$

For a realistic assumption $R_{RD}>>r_B$, this becomes

$$\overline{I}^{2}_{CS,RD} = 4KT\frac{g_{m,CS}}{2}\left[\frac{1}{\beta_F}+\frac{2}{g_{m,CS}R_{RD}}\right]. \tag{6.49}$$

This result can now be directly compared to the total output current noise power of the RID TCS, Eq. (6.42). The resonant-inductive degeneration is more effective than the resistive degeneration, if condition (6.50) is satisfied.

$$\left(\frac{f_{T,CS}}{2f_0}\right)^2\frac{1}{r_{B,CS}g_{m,CS}} > g_{m,CS}R_{RD} \tag{6.50}$$

As $r_{B,CS}g_{m,CS}$ is a small constant (equals c for Q_{CS} 2x larger than Q_1, Q_2) and $2f_0/f_{T,CS}>>1$, the resonant-inductive degeneration can be considered as a better solution than the resistive degeneration for low-supply voltages (e.g., $V_{CC}<3.3$V). For example, for $c=0.1$ (a high-performance LC-tank), and $f_{T,CS}=10f_0$, the resistive degeneration would be a noise reduction method of choice if a loop gain of the RD transistor is impractically large for low supply voltages, $g_{m,CS}R_{RD}>250$.

However, if a high supply voltage were available (e.g., $V_{CC}>3$V), the RD would be preferable, as its implementation is rather straightforward.

6.3.8 Adaptive Phase-Noise Model

From Eq. (6.47), the noise factor of the VCO with resonant-inductive degeneration of the bias tail-current source reduces to

$$F = 1+\frac{n}{2}+nck\,. \tag{6.51}$$

When the noise contributed by the bias circuit is negligible, the oscillator phase-noise performance depends on the components in the *ac* signal path, viz., transconductance cell and resonator. With the aid of Eqs. (6.4), (6.9), (6.22) and (6.51), the adaptive phase-noise model now becomes

$$\mathcal{L} \propto \frac{1+n/2+nck}{n^2k^2}\,. \tag{6.52}$$

This model is parameterized with respect to power consumption via the *small-signal loop gain k*. Unlike fixed, hardware determined design parameters, the loop gain and voltage swing can be varied by changing current I_{TAIL}, shown in Fig. 6.1. This allows adaptation of the oscillator phase noise to different conditions. Parameter $k=G_{M,TK}/G_{TK}$ defines how far the oscillator is from the start-up condition. As this is a key parameter used in the forthcoming analysis, let us explain in more detail its meaning and importance.

In its simplest form k is the small-signal loop gain of the oscillator considered as a positive feedback amplifier. In addition, k relates to the excess of the negative conductance necessary for the compensation of the losses in the LC-tank. Namely, if the tank conductance is G_{TK}, then for the start-up of the oscillations, the equivalent negative conductance seen by the LC-tank must be $G_{M,TK}=kG_{TK}$, with k larger than one (for a guaranteed start-up usually set to a value of two).

6.4 Phase-Noise Performance of Quasi-Tapped Voltage-Controlled Oscillators

The performance of the oscillator with a capacitive voltage divider in a feedback loop (quasi-tapped VCO) will be characterized by comparing it to a non-tapped VCO. A non-tapped (NT) VCO is an oscillator with a directly coupled LC-tank and active part (n=1), i.e., the oscillator shown in Fig. 6.1 with C_A=0 and C_B=∞. The LC-tanks of both oscillator types are assumed identical.

Referring to Eq. (6.52), the phase noise of a QT-VCO (n>1) and an NT-VCO (n=1) can be written as

$$\mathcal{L}_{QT} \propto \frac{1+n/2+nc_{QT}k}{n^2k^2}, \tag{6.53}$$

$$\mathcal{L}_{NT} \propto \frac{1+1/2+c_{NT}k}{k^2}, \tag{6.54}$$

where $c_{QT}=nc_{NT}=nr_Bg_{ms\text{-}up,NT}$, with $g_{ms\text{-}up,NT}$ being the start-up (k_{NT}=1) small-signal transconductance of an NT-VCO.

Now, the *ratio* between the *phase noise* of a non-tapped and a quasi-tapped oscillator, *PNR* (k_{QT},k_{NT}), can be defined as

$$PNR(k_{QT},k_{NT}) = \frac{\mathcal{L}_{QT}(k_{QT})}{\mathcal{L}_{NT}(k_{NT})}, \tag{6.55}$$

$$PNR(k_{QT},k_{NT}) = \frac{1+n/2+nc_{QT}k_{QT}}{n^2k_{QT}^2} \ \frac{k_{NT}^2}{1+1/2+c_{NT}k_{NT}}. \tag{6.56}$$

For n=1 and k_{QT}=k_{NT}, the QT-VCO reduces to the NT-VCO, and obviously, the ratio *PNR* becomes equal to one.

The operating conditions used for the comparison of oscillators are: k_{NT}=nk_{QT} (the same power consumption), and k_{NT}=k_{QT} (the same distance from the start-up condition). The latter because loop gain is an important oscillator parameter.

From Eq. (6.56), the phase-noise ratio for the same power consumption, k_{NT}=nk_{QT}=nk, equals

$$PNR(k,nk) = \frac{1+n/2+n^2c_{NT}k}{1+1/2+nc_{NT}k}. \tag{6.57}$$

Ratio (6.57) implies that a non-tapped oscillator has better performance than a quasi-tapped oscillator, with respect to the phase noise for the same power consumption. For example, if n=2, k=2 (the safety start-up condition), r_B=40Ω and $g_{ms\text{-}up,NT}$=4.1mS, there is a phase-noise difference or around 1.8dB in favor of the non-tapped oscillator (calculated result). This result can be beneficiary used in the design of oscillators. Namely, as quasi-capacitive tapping already allows for an increased voltage swing across the LC-tank by an independent base biasing of transconductor transistors, the reduced power consumption and better phase noise can be achieved by setting n close to one.

In a similar manner, the phase-noise ratio for the same excess negative conductance (k_{NT}=k_{QT}=k) is given as

$$PNR(k,k) = \frac{1+n/2+n^2c_{NT}k}{n^2(1+1/2+c_{NT}k)}. \tag{6.58}$$

This result shows that a quasi-tapped oscillator has better performance than a non-tapped oscillator, with respect to the phase noise for the same loop gain. Referring to r_B=40Ω, $g_{ms\text{-}up,NT}$=4.1mS, n=2 and k=6, an *PNR* of around –2.2dB results from the calculations.

6.5 Adaptivity Figures of Merit of Voltage-Controlled Oscillators

Adaptivity phenomena can be qualitatively and quantitatively described by means of theirs figures of merit. Phase-noise tuning range describes phase-noise adaptivity of an oscillator with respect to power consumption. Frequency-transconductance sensitivity describes the effect of compensating for the change in the LC-tank characteristic due to frequency tuning. Both metrics are analytically derived in the remainder of this section.

6.5.1 Phase-Noise Tuning Range

Before detailing on the phase-noise tuning, let us broaden the meaning of the corner-stone parameter k. As in the oscillator under consideration, the start-up condition is also referred to the minimum power condition, apart from defining how far an oscillator is from this state, the parameter k also characterizes the increase in power consumption. Namely, k-times larger negative conductance of the active part of the oscillator requires a k-times increase in power consumption, with respect to the start-up condition. Power consumption is controlled by the tail current I_{TAIL}, shown in Fig. 6.1.

The figure of merit describing the oscillator's adaptivity to phase noise is the *phase-noise tuning range* (*PNTR*). For a k_2/k_1-times change in power consumption, and with the aid of the idealistic model of Eq. (6.52), the phase-noise tuning range for the QT-VCO under consideration is defined as

$$PNTR(k_1,k_2) \propto \frac{k_1^2}{k_2^2}\frac{1+n/2+nck_2}{1+n/2+nck_1}. \tag{6.59}$$

We will first determine the loop gain k_{MAX} (related to the best phase noise) in order to estimate the achievable phase-noise tuning range. The start-up condition corresponds to k_{MIN}=1, whereas the guaranteed start-up to k_{MIN}=2.

For the maximum voltage swing across the LC tank that satisfies

$$v_{S,MAX} \le \frac{2n}{n+1}(V_{CC}-V_B+V_{BE}-V_{CE,SAT}), \tag{6.60}$$

the detrimental effects of both hard saturation of the transistors in the active part of the oscillator and the additional current noise of their forward biased

base-collector junctions are circumvented [18,19]. Here, V_{CC} is the supply voltage, V_B the base potential of the core transistors, V_{BE} their base-emitter voltage and $V_{CE,SAT}$ their collector-emitter saturation voltage. Assuming that the bases of the transistors are, for the sake of the simplicity, at the maximum supply voltage, i.e., $V_{CC}=V_B$, the maximum voltage swing across the LC-tank ($V_{CE,SAT}$=0V) equals $v_{S,MAX1}=1.5n/(n+1)$ (it is assumed that V_{BE}=0.75V). On the other hand, the maximum voltage swing corresponding to the non-saturation condition ($V_{CE,SAT}$=0.3V) is $v_{S,MAX2}=0.9n/(n+1)$. Compromising between larger voltage swing on the one hand and weaker saturation on the other we opt for a maximum voltage swing across the tank $v_{S,MAX}=(v_{S,MAX1}+v_{S,MAX2})/2$.

Now, with the aid of Eq. (6.9), and for n=2, the maximal loop-gain value is found to be k_{MAX}=6.

For example, if k_{MIN}=2 (the safety start-up condition) and k_{MAX}=6 (expected best phase noise), c=0.65, and n=2, the control ranges of power consumption and phase noise are calculated as

$$P_{MAX} / P_{MIN} = k_{MAX} / k_{MIN} = 3\,, \tag{6.61}$$

$$PNTR(2,6) = \mathcal{L}_{MIN} / \mathcal{L}_{MAX} \cong -6.3 \text{ dB}\,. \tag{6.62}$$

P_{MAX} and P_{MIN} stand for maximum and minimum power consumption, and $\mathcal{L}_{\text{MAX}}$ and $\mathcal{L}_{\text{MIN}}$ represent the maximum and the minimum phase noise corresponding to the values of k_{MAX} and k_{MIN}, respectively.

This result shows that for the oscillator under consideration and with equal supply and transconductor base voltages, a phase-noise tuning range in excess of 6dB can be expected with a factor of three reduction (change) in power consumption.

6.5.2 Frequency-Transconductance Sensitivity

Because of a change in frequency due to tuning of the LC-tank varactor capacitance (C_V), the loop gain, the voltage swing and the phase noise of the oscillator change as well [20]. If the oscillator is designed at the very edge of the required specifications, the change of the oscillation condition (i.e., reduced loop gain) or the change of the noise produced (i.e., degraded phase noise) puts the oscillator out of correct operation. In order to preserve desired operation of oscillators, it is necessary to apply a control mechanism to the bias current I_{TAIL} (i.e., g_m).

The concept of C-g_m tuning illustrates the relationship between the varactor diode tuning voltage U_T and the biasing tail current I_{TAIL}, both indicated in Fig. 6.1. The objective is to find the relationship between the tuning voltage U_T and the effective tank conductance G_{TK} on the one hand and the relationship between the tank conductance and the biasing tail current I_{TAIL} on the other. The resulting sensitivity of the tail current to the tuning voltage will show to what extent the biasing condition should be changed in response to a change in the frequency, in order to keep the oscillator operating under the specified conditions.

The sensitivity of the LC-tank conductance to a change in a tuning voltage is defined as

$$S_{U_T}^{G_{TK}}\Big|_{U_T=U_{T0}} = \frac{\partial G_{TK}}{\partial C_V}\frac{\partial C_V}{\partial U_T}, \tag{6.63}$$

where tuning voltage U_{T0} corresponds to the resonant frequency f_0.

With the aid of Eqs. (6.1) and (6.3), the sensitivity of the LC-tank conductance to a change in varactor capacitance C_V can be expressed in terms of LC-tank parameters,

$$S_{C_V}^{G_{TK}} = \omega_0^2\left[2C_V R_C\left(1-\frac{C_V}{2C_{TOT}}\right)+C_{TOT}R_L\right]. \tag{6.64}$$

If the varactor capacitance is related to a tuning voltage U_T as

$$C_V(U_T) = \frac{C_{V0}}{\left(1+\dfrac{V_{CC}-U_T}{\varphi}\right)^{1/a}}, \tag{6.65}$$

where C_{V0}, φ and a are the parameters of the varactor shown in Fig. 6.1, the sensitivity of the varactor capacitance to a tuning voltage equals

$$S_{U_T}^{C_V} = \frac{C_V}{a(V_{CC}-U_{T0}+\varphi)}. \tag{6.66}$$

Note that the capacitance C_V is related to the tuning voltage U_{T0} and the frequency f_0.

Linearizing the sensitivity characteristics calculated around resonance, the change in the effective tank conductance can be related to the change in the tuning voltage as

$$\Delta G_{TK} = S_{U_T}^{G_{TK}} \Delta U_T , \tag{6.67}$$

where the relating sensitivity has a form

$$S_{U_T}^{G_{TK}} = \frac{2}{a(V_{CC} - U_{TO} + \varphi)} \left[R_C \left(1 - \frac{C_V}{2C_{TOT}} \right) + \frac{C_{TOT} R_L}{2C_V} \right] (\omega_0 C_V)^2 . \tag{6.68}$$

To compensate for such a change in the tank characteristic, the conductance seen by the tank ($-G_{M,TK}$) should be changed by the same amount. From Eq. (6.2), the relationships between the tail current, the transistors transconductance and the conductance seen by the LC-tank are determined:

$$\Delta I_{TAIL} = 2V_T \Delta g_m , \tag{6.69}$$

$$\Delta g_m = 2n \cdot \Delta G_{M,TK} . \tag{6.70}$$

Combining these results, the change in the tail current relates to the change in the absolute value of the conductance seen by the LC-tank as

$$S_{G_{M,TK}}^{I_{TAIL}} = 4n \cdot V_T . \tag{6.71}$$

Satisfying Eq. (6.72) (see Eq. (6.2)),

$$\Delta G_{M,TK} = k \Delta G_{TK} , \tag{6.72}$$

the sensitivity of the tail current to the tuning voltage, referred to the increase or the reduction in the tail current (power consumption) in order to sustain the desired loop-gain value (oscillation condition) is calculated as

$$S_{U_T}^{I_{TAIL}} = S_{G_{M,TK}}^{I_{TAIL}} S_{G_{TK}}^{G_{M,TK}} S_{U_T}^{G_{TK}} . \tag{6.73}$$

With the aid of Eqs. (6.68), (6.71), (6.72) and (6.73), we finally obtain

$$S_{U_T}^{I_{TAIL}} = \frac{8k \cdot n \cdot V_T}{a(V_{CC} - U_{TO} + \varphi)} \left[R_C \left(1 - \frac{C_V}{2C_{TOT}} \right) + \frac{C_{TOT} R_L}{2C_V} \right] (\omega_0 C_V)^2 . \quad (6.74)$$

For the oscillator under consideration, we can now estimate to what extent the tail current should be changed as a result of a change in the tuning voltage, i.e., frequency, in order to keep the oscillator operating under the required conditions.

For example, a sensitivity $S_{U_T}^{I_{TAIL}}$ =0.25mA/V infers that in order to sustain the oscillations under the same condition (i.e., the same loop gain) the tail current should be either increased or reduced (depending on the direction of the frequency tuning) by 0.25mA for a 1V change in a varactor voltage. The counterpart of the *C*-g_m tuning in the circuitry is a simple amplitude control mechanism, as constant loop gain means constant amplitude of the signal across the LC-tank of the oscillator.

6.6 K-Rail Diagrams – Comprehensive Performance Characterization of Voltage-Controlled Oscillators

The existing figures of merit [21,22], giving insight into the performance of oscillators operating under fixed conditions, have been reformulated in order to be useful for the performance characterization of adaptive circuits: phase-noise tuning range and frequency-transconductance sensitivity. These adaptivity figures of merit as well as other phenomena related to voltage-controlled oscillators can be both qualitatively and quantitatively interpreted by means of the K-rail diagrams. There are two types of oscillator K-rail diagrams: *K-rails* and *K-loop* diagrams, both using the construction rules outlined in Chapter 4.

The K-rails diagram is used as a tool for the comprehensive performance *comparison* of different voltage-controlled oscillators. In this section, a non-tapped VCO and a quasi-tapped VCO are used as an example.

The K-loop diagram is used for the performance *characterization* of adaptive voltage-controlled oscillators. Namely, K-loop diagrams show how the oscillator performance parameters (e.g., phase noise, loop gain, power consumption, voltage swing and tank conductance) relate to each other at any point of the design space. Moreover, these diagrams describe the effects of the particular design choice on the performance of oscillators.

In the following section, the concept of phase-noise tuning is described with a K-rail diagram. Then, a qualitative comparison of different VCOs is made using the K-rails (multiple K-rail) diagram. The concept of frequency-transconductance tuning and the accompanying K-loop diagram close the discussion on oscillators K-rail diagrams. Finally, it is shown by an example how performance parameters of an oscillator can be mapped onto these diagrams.

6.6.1 K-Rail Diagram

In the following analysis, we will refer to the adaptive oscillator shown in Fig. 6.1. Parameters of the oscillator have already been defined in Section 6.2, and Eqs. (6.1)-(6.3).

Generally, K-rail diagrams reveal trade-offs between oscillators performance parameters. As suggested by the name of the diagram, the parameter k is given the role of the cornerstone parameter in the analysis. Defined as $k=G_{M,TK}/G_{TK}$, it equally represents the small-signal loop gain, the excess conductance seen by the LC-tank as well as the excess power consumption. For the start-up condition it has a value of $k=1$, while for guaranteed (safe) oscillation a value $k>1$.

Let us consider phase-noise tuning range (*PNTR*), an adaptivity performance parameter aimed not at a particular, but rather a set of operating conditions. Given by Eq. (6.51), this adaptivity figure of merit stands for a change in the oscillator phase noise between two different biasing (design) points.

This phenomenon can be qualitatively described by means of the K-rail diagram [23] shown in Fig. 6.10. It is illustrated how the oscillator performance parameters, being loop gain, power consumption, phase noise and signal amplitude, relate to each other in an adaptive manner.

The arrows perpendicular to the corresponding axes represent lines of constant loop gain, phase noise and power consumption. Namely, each point in the design space (in this case a line; the k-rail) corresponds to a set of design parameters that are obtained as a normal projection of the design point on the rail to the indicated axes. Take, for example, point MAX on the k-rail. Its corresponding parameters are phase noise PN_{MAX}, loop gain k_{MAX}, and voltage swing v_{MAX}, respectively.

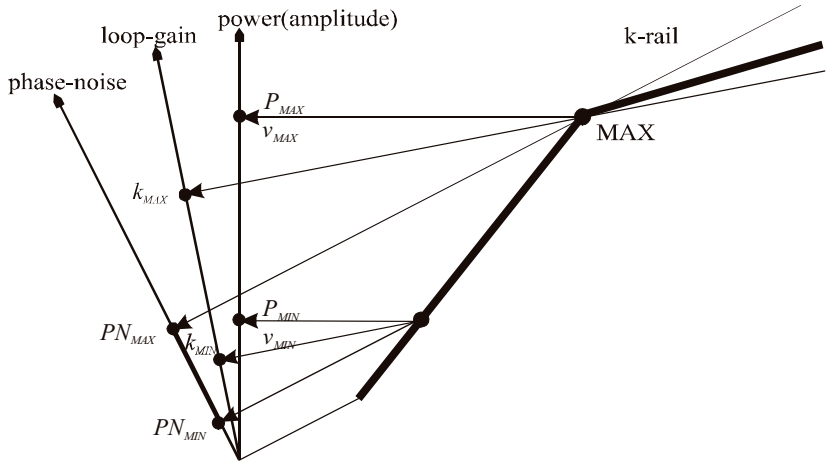

Figure 6.10: K-rail diagram for LC-VCOs.

The phase-noise tuning range shown in Fig. 6.10 between the points PN_{MIN} and PN_{MAX}, where PN_{MAX} ($1/\mathcal{L}_{MIN}$) and PN_{MIN} ($1/\mathcal{L}_{MAX}$) represent the maximum (i.e., best) and minimum phase noise, corresponds to the values k_{MAX} and k_{MIN}. In addition, some well known phenomena can also be recognized. For example, it is seen that an increase in power results in an improvement in the phase noise, but only up to a level determined by k_{MAX}. Increasing the loop gain beyond this value only wastes power, as the phase noise no longer improves.

Finally, the diagram helps one to grasp the basic concepts regarding behavior and functionality of VCOs without plunging into the "sea" of figures of merit, theories and expressions.

6.6.2 K-Rails Diagram

The K-rails diagram [23] is used for the performance comparison of different voltage-controlled oscillators. In this section, we will construct a K-rail diagram by comparing non-tapped and quasi-tapped VCOs.

The operating conditions that are used for the construction of the K-rails diagrams are the same power consumption condition ($k_{NT}=nk_{QT}$) and the same distance from the start-up condition, i.e., the same loop gain condition ($k_{NT}=k_{QT}$).

The phase-noise ratio for the same power consumption (Eq. (6.57)) shows that a non-tapped oscillator has better performance than a quasi-tapped oscillator.

This expression can be qualitatively mapped onto the K-rails diagram shown in Fig. 6.11. The arrows L_1, L_2 and L_3, perpendicular to the corresponding axes, represent lines of constant loop gain, phase noise and power consumption, respectively. Apart from the indicated loop gain, phase noise and power (amplitude) axes, this diagram has two k-rails, each referring to the oscillators design space (i.e., "design lines"). Here, the left rail corresponds to the non-tapped and the right rail to the quasi-tapped oscillator. For example, the design parameters of point A on the left-most rail (NT-VCO) are the phase-noise related parameter PN_{NT}, loop gain k_{NT}, and voltage swing v_{NT}.

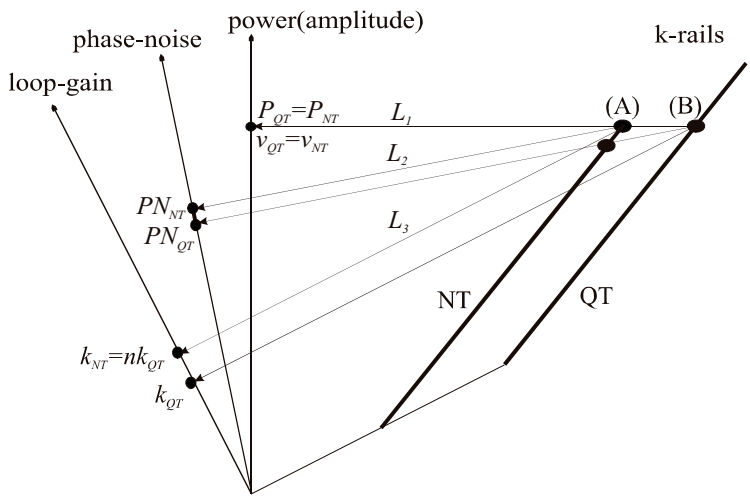

Figure 6.11: K-rails diagram for the same power consumption of NT- and QT-VCOs.

Following the diagram construction rules, it can be seen that for the same power consumption $P_{NT}=P_{QT}$, and accordingly $k_{NT}=nk_{QT}$ (points A and B), it holds $PN_{NT}>PN_{QT}$ (> means better). That is to say, the phase noise ($\mathcal{L}=1/PN$) of a non-tapped oscillator is better than the phase noise of a quasi-tapped VCO (as already indicated by Eq. (6.57)).

In a similar manner, the phase-noise ratio for the same excess negative conductance ($k_{NT}=k_{QT}$) that is given by Eq. (6.58) shows that a quasi-tapped

VCO has better performance than a non-tapped VCO. This operating condition is depicted by Fig. 6.12, where for the phase noise corresponding to the points A and B ($k_{NT}=k_{QT}=k$) holds $PN_{NT}<PN_{QT}$.

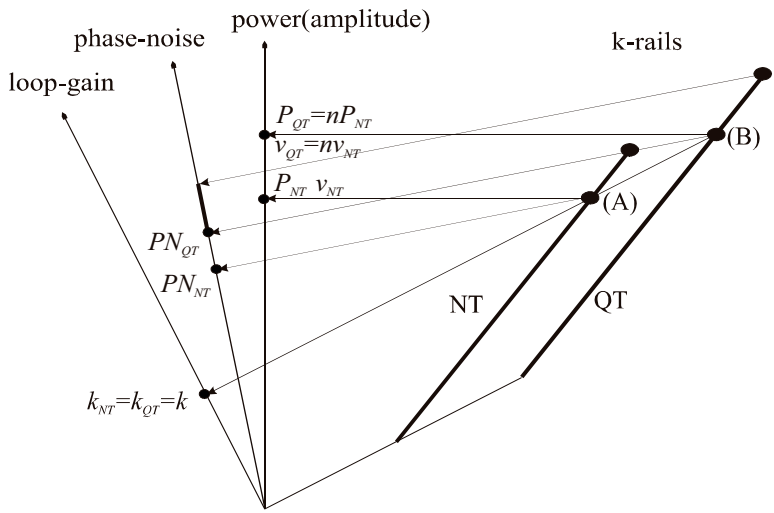

Figure 6.12: K-rails diagram for the same loop gain of NT- and QT-VCOs.

Finally, we can stress that the presented diagrams give a qualitative comparison between differently tapped VCOs. A number of parameters can simultaneously be compared, as it can also be seen to what extent the change in one parameter is reflected to other parameters.

6.6.3 K-Loop Diagram

The K-loop diagram [30] is used for a full performance characterization of adaptive oscillators. While in the case of the K-rails diagram it is assumed that the LC-tanks of the oscillators are fixed, phenomena related to the change in the resonating tank are described by K-loop diagrams.

The phenomenon of C-g_m tuning (Section 6.5.2) and the resulting sensitivity of the tail current I_{TAIL} to the tuning voltage U_T (see Eq. (6.74) and Fig. 6.1) are qualitatively described by means of the diagram that is shown in Fig. 6.13.

Compared to K-rail diagrams, one more axis is added. It refers to the LC-tank conductance and the oscillation frequency. In addition, two more rails are

added (k_2 and k_3), each corresponding to a different LC-tank, viz., a tank at a lower (f_L) and a tank at an upper oscillation frequency (f_U).

To explain the use of K-loop diagrams we will make one loop, for example, from point (0) to point (4) in the diagram, shown in Fig. 6.13.

Increasing the varactor capacitance results in a lower oscillation frequency f_L as well as a larger effective tank conductance $G_{TK,L}$, both related to the right-most rail k_2 in the diagram. The new operating point of the oscillator is found at the intersection of the new k-rail (k_2) and the power consumption level (P_0). As the tail current inserted is at the same level, i.e., I_{TAIL0}, the oscillator state is therefore changed from point (0) to point (1). It can be noticed that at point (1), the voltage swing across the resonator, the loop gain and the phase noise parameter are all decreased.

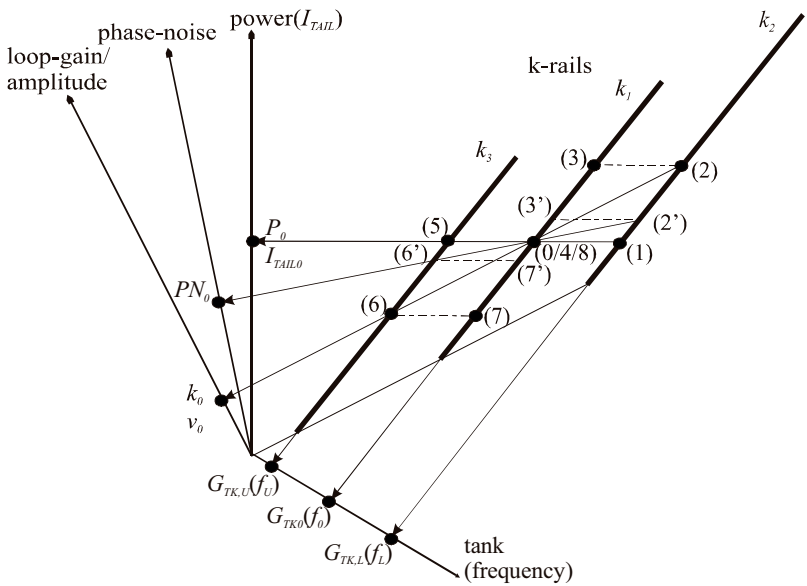

Figure 6.13: K-loop diagram for LC-VCOs.

To compensate for such deterioration in performance, the power level (tail current) must be increased for the amount indicated by Eq. (6.74). This corresponds to the next position in the diagram, point (2). At this operating point, the loop gain and the amplitude of the oscillation signal are restored to their previous levels (i.e., before the tuning action; v_0 and k_0). Moreover, the phase noise can even improve compared to the starting operating point PN_0.

On the other hand, the reduction of the varactor capacitance, and according increase of the oscillation frequency and reduction of the tank conductance, corresponds to point (3) on the middle k-rail, k_1. As the phase noise, the loop gain, the amplitude of the voltage swing, and the power consumption are at unnecessarily higher levels, the tail current can be reduced for an amount given by Eq. (6.74) so that all specifications are satisfied again. This brings us to point (4). As shown in the diagram, point (4) corresponds to starting point (0). In a similar manner, the left loop is constructed, consisting of points (4) to (8).

On a journey throughout the K-loop diagram, not only can all the previously addressed phenomena be recognized, but also all the trade-offs between power consumption, phase noise and loop gain can be qualitatively interpreted. Ending this journey, let us just name this particular phenomenon "frequency-transconductance tuning for a *constant loop gain"*. Note that the counterpart of the preceding concept in the circuitry is a simple amplitude control mechanism, as constant loop gain means constant amplitude of the signal across the LC-tank of the oscillator.

6.6.4 Construction of K-Loop Diagrams - an all-Round Example

An example is now presented addressing the concepts introduced in this chapter and showing usefulness of the K-loop diagram for both qualitative and quantitative representation of the adaptivity phenomena. As in the previous sections, we will refer to the bipolar oscillator (shown in Fig. 6.1) in the forthcoming analysis.

The values of the oscillator parameters are: f_0=900MHz, $2C_V$=2pF, Q_C=15, $L/2$=12.5nH, Q_L=4, $2C_A$=1pF, $2C_B$=1pF, V_{CC}=2V, U_{T0}=1V, φ=0.5V, a=2, and k=2, where Q_C and Q_L are the quality factors of the corresponding varactors and inductors.

To see what are the effects of both the varactor voltage tuning and the corresponding C-g_m tuning, we will use the diagram shown in Fig. 6.14 for the analysis. In addition, it will be shown how the loop gain, the tail current, the effective tank conductance and the phase noise values can be found at any point of the diagram.

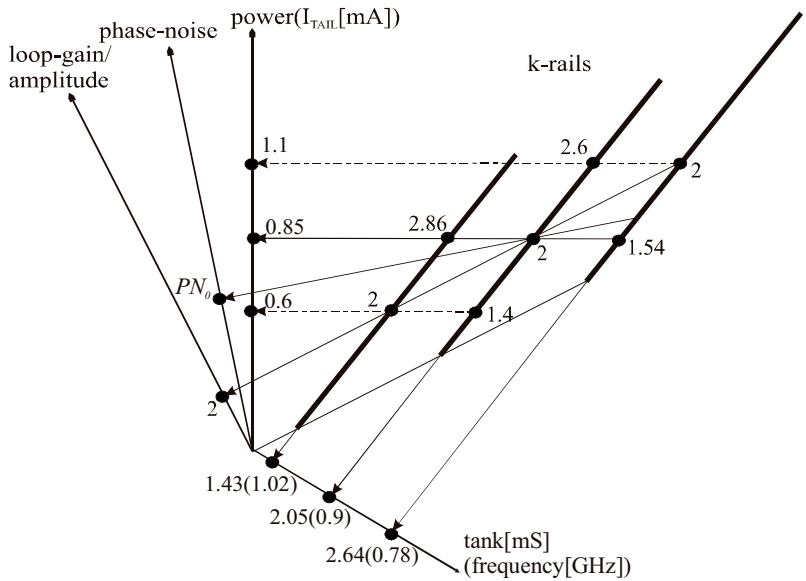

Figure 6.14: K-loop diagram for given parameters of the oscillator.

First, we will determine the values of the tank conductance for the lower, the central and the upper oscillation frequency. From Eq. (6.1), it is found that the tank conductance equals G_{TK}=2.05mS at the frequency f_0=900MHz, while from Eq. (6.2) the tail current is found to be I_{TAIL0}=0.85mA. For a maximum voltage tuning range of 1V, from Eq. (6.74) the maximum change in the tail current is expected to be $S_{U_T}^{I_{TAIL}}$=0.25mA/V. In order to sustain oscillations under the same condition (i.e., the loop gain of two), the tail current should be either increased or reduced by this amount as a response to frequency tuning.

Keeping the order of points the same as in Fig. 6.13, points (2) and (3) of the diagram correspond to a tail current of 1.1mA, while points (6) and (7) correspond to a current of 0.6mA. Knowing the loop gain at operating point (2) and referring to the tail current of 1.1mA as the safety start-up current for a new LC-tank, we can calculate the new tank conductance from Eq. (6.2). Corresponding to a lower resonant frequency f_L=780MHz, its value is $G_{TK,L}$=2.64mS. This holds for a tuning range of ±120MHz. The loop gain for point (3) is k=2.6, after the tuning system is linearized near the loop gain point k=2. The parameters of the left loop ((4) to (8)) are calculated following the same procedure.

Finally, the phase-noise ratio *PNR* and the phase-noise tuning range *PNTR* can be found and allocated to the points of the K-loop diagram. From Eqs. (6.57) and (6.58), the ratio *PNR* between points (0) and (2) is estimated to be around 1dB, while from Eq. (6.61), the *PNTR* between points (0) and (3) is calculated to be around 2dB.

6.7 Oscillator Design Problem

A schematic of a directly-coupled negative resistance LC voltage-controlled oscillator is shown in Fig. 6.15.

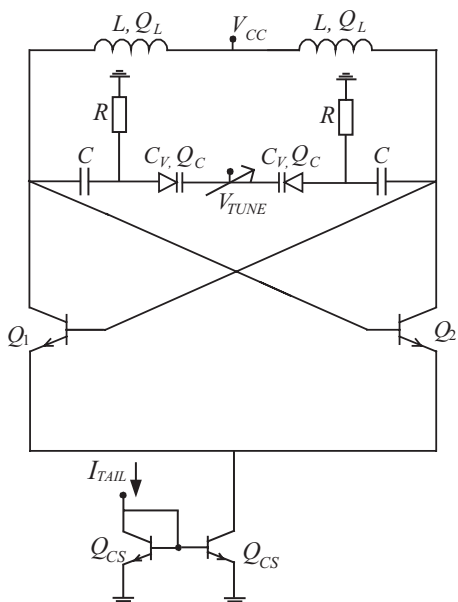

Figure 6.15: A directly-coupled LC voltage-controlled oscillator.

The oscillator consists of a resonating LC tank, a cross-coupled transconductance amplifier (Q_1 and Q_2). L stands for the tank inductance, Q_L for its quality factor, C_V for the varactor capacitance, Q_C for its quality factor, C for the additional tank capacitance with a quality factor $Q>>Q_C$, V_{CC} for the supply voltage, V_{TUNE} for the varactor tuning voltage, and I_{TAIL} for the bias tail current.

Determine the circuit parameters of this oscillator in order to meet the requirements of the Wireless Local Area Network (WLAN) standard [24]:

- central oscillation frequency of 2.44GHz,
- phase noise better than –110dBc/Hz at 1MHz offset from the central oscillation frequency,
- peak amplitude of a differential oscillation voltage signal across the LC-tank between $0.2V<v_S<0.4V$,
- maximum power consumption of 1mW from a 3V supply.

For a silicon technology chosen, inductors (L_{MAX}<5nH) with quality factors of 25 and varactors with quality factors of 35 are available in the 2.4GHz band.

For the oscillator design, provide the following:

(a) An expression for the LC-tank conductance (G_{TK}) at the oscillation frequency, assuming $R>>1/G_{TK}$.

(b) Expressions for the oscillation frequency f_0 and oscillation condition.

(c) An expression for the phase noise of the oscillator using circuit parameters. Model the LC-tank noise contribution by its loss conductance, G_{TK}, and the total active part noise contribution by AG_{TK}, A being the active part noise factor. Consider the bias circuitry as noiseless.

(d) Values of inductance L, varactor capacitance C_V, and tail current I_{TAIL}, for the oscillator requirements at the central oscillation frequency (assume $C=C_V$ at f_0). The noise factor of the transconductor is A=3.

(e) Values of minimum ($C_{V,MIN}$) and maximum ($C_{V,MAX}$) varactor capacitances for a frequency tuning between 2.4GHz and 2.48GHz.

Below are given the results only. The workout of the problem is left to the reader.

(a) LC-tank conductance:

$$G_{TK} = \omega_0 C_{TK} \frac{1}{Q_{TK}} \tag{6.75}$$

$$C_{TK} = \frac{1}{2} \frac{CC_V}{C + C_V} \tag{6.76}$$

$$\frac{1}{Q_{TK}} = \frac{1}{Q_L} + \frac{1}{mQ_C} \tag{6.77}$$

$$m = 1 + \frac{C_V}{C} \tag{6.78}$$

(b) Oscillation frequency and oscillation condition:

$$f_0 = \frac{1}{2\pi \times \sqrt{L_{TK} C_{TK}}} \tag{6.79}$$

$$L_{TK} = 2L \tag{6.80}$$

$$I_{TAIL} > 4V_T \sqrt{\frac{C_{TK}}{L_{TK}}} \left(\frac{1}{Q_L} + \frac{1}{mQ_C} \right) \tag{6.81}$$

(c) Phase-noise model:

$$\mathcal{L}(\Delta\omega) = \frac{\pi^2}{4} KT \left(\frac{\omega_0}{\Delta\omega} \right)^2 \left(\frac{1}{Q_L} + \frac{1}{mQ_C} \right)^3 \omega_0 \frac{C_{TK}}{I_{TAIL}^2} (1 + A) \tag{6.82}$$

(e) Minimum power-consumption circuit parameters:

$$L = \frac{2}{\omega_0^2 C_V} \tag{6.83}$$

$$\frac{I_{TAIL}}{C_V} = \frac{\pi}{8} \omega_0 \left(\frac{1}{Q_L} + \frac{1}{mQ_C} \right) v_S \tag{6.84}$$

L=5nH, C_V=1.7pF, f_0=2.44GHz, G_{TK}=0.53mS, I_{TAIL}=0.22mA, v_S=0.4V, $\mathcal{L}(1\text{MHz})$ =-113dBc/Hz.

(f) Varactor capacitance tuning requirements:

$$\frac{1}{C_{V,MAX}} = \frac{1}{C_V}\left[2\left(\frac{f_{0,MIN}}{f_0}\right)^2 - 1\right] \tag{6.85}$$

$$\frac{1}{C_{V,MIN}} = \frac{1}{C_V}\left[2\left(\frac{f_{0,MAX}}{f_0}\right)^2 - 1\right] \tag{6.86}$$

$C_{V,MAX}$=1.82pF, $C_{V,MIN}$=1.59pF.

6.8 Conclusions

Enhancing performance of wireless devices to cover multiple standards and provide more services offers more functionality to communication systems, but better performance only if systems can be adapted (i.e., respond actively to varying channel conditions). This necessitates a new design philosophy for analog receiver circuits. Therefore, a concept of designing for adaptivity has been introduced in this chapter, establishing a procedure for performance characterization of adaptive oscillators with qualitative and quantitative descriptions of the relationships and trade-offs between oscillator performance parameters.

The concept of phase-noise tuning explains how the designers can trade off RF performance of an oscillator for power consumption in an adaptive way. The extremes of the phase-noise tuning range and the power consumption reduction have been illustrated.

Furthermore, the concept of frequency-transconductance tuning has been presented. The analytical expressions derived have shown how this concept can be employed in order to achieve full control over the operation of the oscillator.

Finally, the performance characterization of oscillators using conceptual K-rail diagrams has been presented. It has been shown how K-rail diagrams can be used to interpret adaptivity phenomena and adaptivity figures of merit of oscillators.

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Chapter 7

DESIGN OF ADAPTIVE VOLTAGE-CONTROLLED OSCILLATORS AND ADAPTIVE RF FRONT-ENDS

Today's portable communication devices enable a growing variety of applications, ranging from text messaging, telephony and audio to full video. These devices must maintain connectivity while running multiple applications, they must track position, and be wearable rather than just portable. However, the energy supply for portables is fixed by the size and weight of the batteries in a handheld device. Consequently, the current consumption of circuitry in handhelds must be reduced in order to meet these increasing functional and concurrent operational requirements. Limited gains can be made through further improvements in circuit efficiency, radio architectures, and by sharing circuit blocks wherever possible. Another potential solution is circuit adaptivity. This requires scaling of parameters such as current consumption to the demands of the signal-processing task at hand.

Demands for new telecom services requiring higher capacities and higher data rates have motivated the development of broadband, third-generation wireless systems. The coexistence of second- and third-generation cellular systems requires multimode, multi-band, and multistandard mobile terminals. To prolong talk time, it is desirable to share and/or switch transceiver building blocks in these handsets, without degrading the performance compared to single-standard transceivers.

In multistandard terminals, power can be saved by using adaptive circuits that are able to trade off power consumption for performance on the fly [1]. Adaptive receiver circuits allow for reduced area, reduced power consumption, and most importantly, have the potential for lower cost in multifunctional terminals.

In this chapter, three design examples of adaptive circuits and systems for wireless communications are presented: a low-power 800MHz voltage-controlled oscillator, a multistandard/multi-mode second/third-generation (2G/3G) voltage-controlled oscillator, and a multi-mode image-reject downconverter.

7.1 Adaptive Low-Power Voltage-Controlled Oscillator

In portable devices, receiver circuits are exposed to worst-case conditions only for a short period during operation. Over-designing for the worst-case condition is therefore inefficient. On the other hand, circuit adaptation to varying channel conditions and application requirements ensures lower cost as the adaptivity allows for power savings, reduced silicon area, and longer battery life. Design of an 800MHz adaptive low-power voltage-controlled oscillator is presented in this section.

Operating from a 3V supply, the oscillator achieves -135.8dBc/Hz phase noise at 10MHz offset from the 800MHz oscillation frequency at a current consumption level of 5mA, and a phase noise of -128.6dBc/Hz at 10MHz offset and 1.5mA bias current. This oscillator achieves a phase-noise tuning range of around 7dB with a factor of around three change in power consumption. For a 0V-3V tuning voltage, a frequency tuning range of 120MHz is achieved (i.e., from 715MHz and 835MHz).

7.1.1 Design for Adaptivity of Voltage-Controlled Oscillators

The voltage-controlled oscillator [1,2], shown in Fig. 7.1, consists of a resonating LC tank, two capacitive voltage dividers and a cross-coupled transconductance amplifier. L stands for the tank inductance, C_V the varactor capacitance, C_A and C_B the quasi-tapping capacitances and R_D the tail-current source degenerative resistance. This oscillator topology is extensively discussed in Chapter 6.

Selection of design parameters for an adaptive oscillator is discussed next. The phase-noise adaptivity figure of merit (Eq. (6.59)) that accounts for a number of oscillator operation conditions and required specifications forms a base for design of adaptive oscillators. For given phase-noise tuning range (*PNTR*), the maximum loop gain (k_{MAX}) can be determined from Eq. (6.59) (the minimum loop gain is already known, e.g., k_{MIN}=2). On the other hand, if

the maximum and minimum loop gain values are know, the obtainable *PNTR* can be determined from Eq. (6.59) (i.e., the range of oscillator adaptation with respect to phase noise).

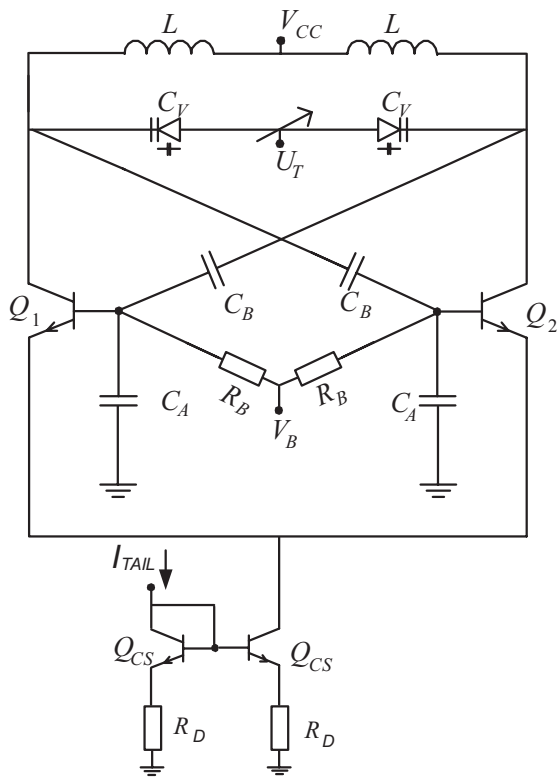

Figure 7.1: An adaptive LC-oscillator.

Furthermore, from the maximum phase-noise requirement and the frequency tuning range requirement, the LC-tank parameters can be determined, i.e., coil inductance and varactor capacitance. Once the resonator components are known, the equivalent tank conductance (G_{TK}) and the minimum power consumption can be determined from Eqs. (6.1) and (6.2), respectively.

Finally, from the maximum loop gain on the one hand and the minimum tail current on the other, the maximum power consumption (tail current) and

power consumption range can be estimated that provide an oscillator with the required phase-noise tuning range.

For k_{MIN}=2 (guaranteed start-up condition), k_{MAX}=6 (expected best phase noise for V_B=V_{CC}), a quasi-tapping ratio n=2, and a parameter c=$r_B g_{ms\text{-}up}$ of 0.65, a phase-noise tuning range *PNTR* of around 6.3dB is estimated from calculations.

7.1.2 Circuit Parameters of the Adaptive Voltage-Controlled Oscillator

For a capacitive divider ratio of n=2, the feedback capacitances C_A=1pF and C_{JI}+C_B=1pF have been chosen, C_{JI} being the base-emitter junction capacitance of devices Q_1 and Q_2 in Fig 7.1.

The reverse biased base-collector junctions of available transistors have been used for variable capacitors (varactors). The quality factor of the varactors is estimated at 15 from simulations (at around 800MHz).

Optimized for low-power operation, a relatively large inductance value of 12nH is chosen, which was laid out in 1um thick top (second) metal layer. The low quality factor of the inductor (Q=2) in 800MHz band is the result of the 6Ωcm substrate resistivity, operating frequency and relatively thin metal windings close to the substrate. The 6.25-turn inductor has an outer diameter d_{OUT}=360um, metal width w=18.5um, and metal spacing s=1um.

The equivalent lumped-element model of the on-chip spiral inductor is shown in Fig. 7.2.

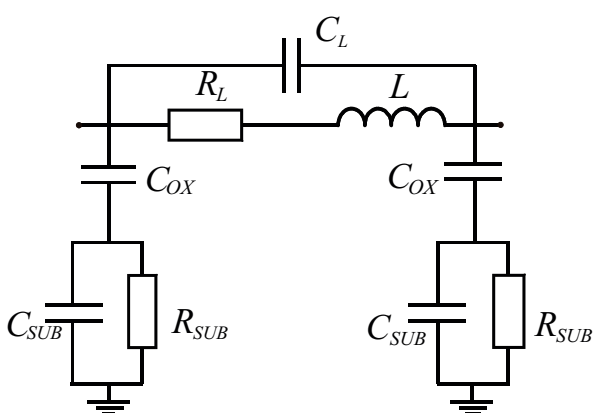

Figure 7.2: Lumped-element model of spiral inductor on silicon.

The model consists of an ideal inductance L, a series resistance R_L (representing the losses in the coil) and an inter-winding capacitance C_L. The oxide capacitance between the spiral and the silicon substrate is modeled by C_{OX}. The substrate resistance and capacitance R_{SUB} and C_{SUB} are added as well, representing the RF signal flow through the silicon substrate.

The model parameters of the inductor are estimated with the phase-noise-inductance (PNL) calculator [3]. The results are shown in Table 7.1. It is appropriate to mention ASITIC [4], an inductor simulator, used to verify the PNL-resulted physical inductor model.

Table 7.1: Model parameters of the employed integrated inductor.

Parameter	Value
L	12nH
R_L	18Ω
C_L	80fF
C_{OX}	0.8pF
C_{SUB}	40fF
R_{SUB}	150Ω

A two-stage common collector buffer has been used as an interfacing stage between the VCO and measurement equipment. Its current consumption is 2mA.

A good match is obtained between the results predicted by calculations and simulations on the one hand and the measurement results on the other, validating the design procedure.

7.1.3 Measurement Results for the Adaptive Voltage-Controlled Oscillator

The chip micrograph of the adaptive oscillator is shown in Fig. 7.3. It occupies an area of 1mm^2, including bondpads. Wire-bonded into a 20-lead package, it is placed in a commercial test fixture.

For a 3V tuning voltage, a frequency tuning range of 120MHz is achieved, between 715MHz and 835MHz, as shown in Fig. 7.4.

Using a technology with a peak transit frequency f_T=8GHz, the VCO achieves a phase noise of -135.8dBc/Hz at 10MHz offset from the 800MHz

oscillation frequency at a current consumption of 5mA. A phase noise of -128.6dBc/Hz at 10MHz offset is measured at a current of 1.5mA. The plots of the maximal and the minimal phase noise measured are shown in Fig. 7.5.

The phase-noise tuning range of around 7dB is achieved for a 3.3 times change in power consumption. A phase-noise tuning range of 6.8dB is calculated for the ratio k_{MAX}/k_{MIN} of 3.3 using the model of Eq. (6.59).

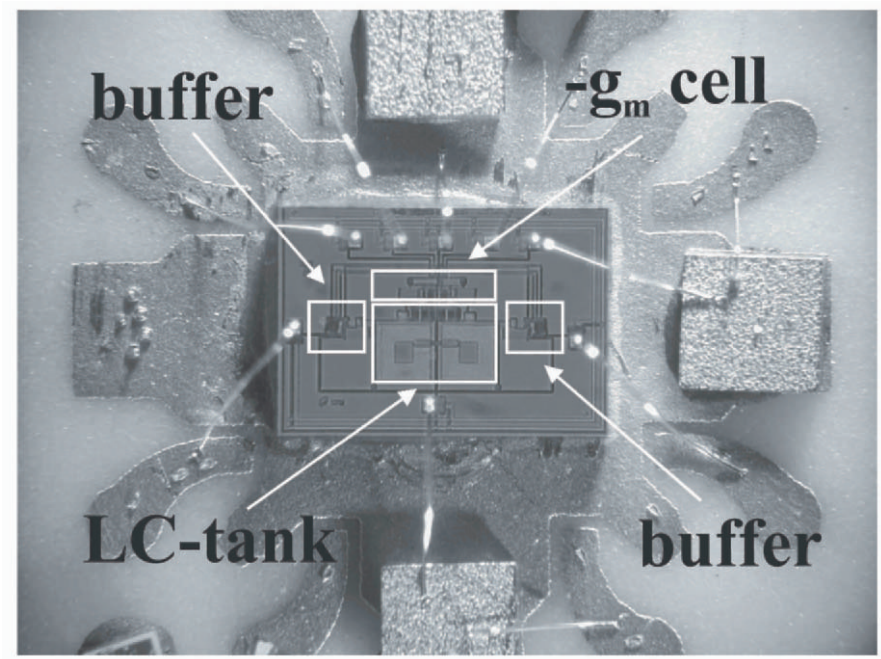

Figure 7.3: The 800MHz oscillator chip micrograph.

The frequency-transconductance tuning phenomenon (Section 6.5) can also be recognized in the results obtained for the oscillator under consideration. Fig. 7.6 depicts the C-g_m tuning phenomenon.

In this case, the oscillator is tuned to the resonant frequency f=800MHz at a tail-current I_{TAIL}=2.5mA. The measured output signal power is -19dBm, and it corresponds to a loop gain value of around three. By tuning the resonant frequency to 740MHz, the output power of the oscillation signal changes to -26dBm, and the VCO's loop gain k approaches one. Any further reduction of the oscillation frequency at the same power consumption results in disappearance of oscillations, as the loop gain k is less than one. This is shown

in Fig. 7.6 at left (-70dBm marker). The corresponding points in the K-loop diagram (Fig. 6.13) are point 1 (-70dBm) and point 5 (-19dBm).

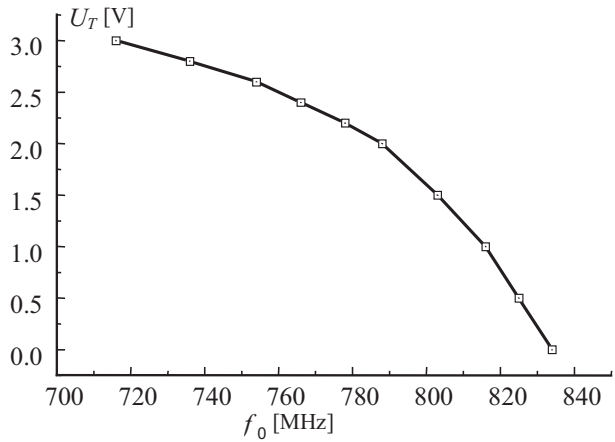

Figure 7.4: Oscillation frequency vs. tuning voltage for the adaptive VCO.

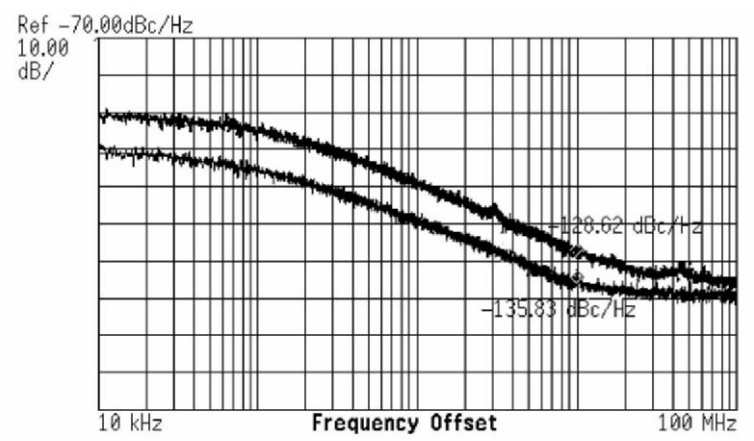

Figure 7.5: Maximum and minimum phase noise at 10MHz offset from the 800MHz oscillation frequency at 5mA and 1.5mA tail currents, respectively.

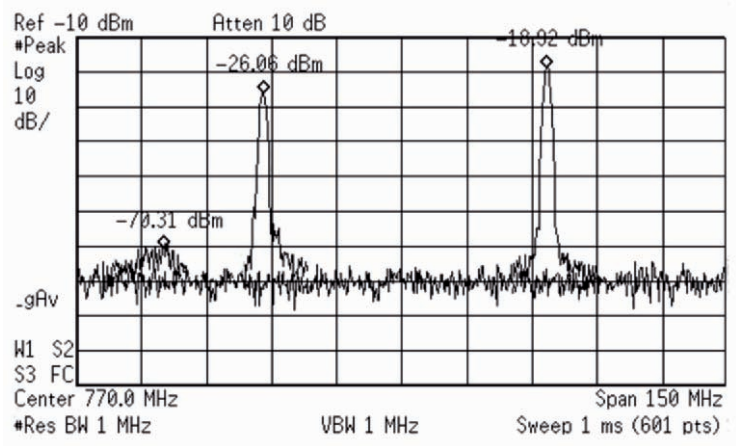

Figure 7.6: Frequency-transconductance tuning from 800MHz to 715MHz oscillation frequency at 2.5mA tail current.

Finally, let us stress that in this single-standard application, the adaptivity is utilized as a power saving mechanism by trading performance (7dB of phase noise) for power consumption (factor of 3.3 saving).

7.2 A Multistandard Adaptive Voltage-Controlled Oscillator

Multistandard modules (MSMs) can be implemented in different ways:

- MSMs can be implemented as standalone fixed circuits that are designed for the worst-case condition of the most demanding standard [5]. Even though operating conditions might improve or a less demanding standard might be active, these circuits always operate at the highest power consumption levels. This design approach thus requires more power.

- MSMs can be implemented as multiple circuits, i.e., one per standard [6]. Even though simple to implement, this approach requires more silicon area. Moreover, when multiple standards operate simultaneously, power consumption increases.

- MSMs can be implemented as standalone, adaptive circuits, by sharing circuit functions across multiple standards, when they don't

operate simultaneously. This allows for reduced area and power consumption and, most importantly, has the potential for reduced cost.

An adaptive, multistandard/multi-band voltage-controlled oscillator that satisfies phase-noise requirements of both second- and third-generation wireless standards (DCS1800/WCDMA/WLAN–Bluetooth-DECT) is described in this section [1]. A factor of around 12 reduction in power consumption has been realized, with a phase-noise tuning range of 20dB by adapting the VCO bias to the desired application. The VCO achieves -123dBc/Hz, -110dBc/Hz and -103dBc/Hz phase noise at 1MHz offset in a 2.1GHz band at supply currents of 6mA, 1.2mA and 0.5mA, respectively.

The design procedure for the multistandard adaptive VCO, i.e., the design for a certain phase-noise tuning range, is outlined next. Parameters selection for the multistandard oscillator and measurement results are discussed afterwards.

7.2.1 Designing for Adaptivity of Multistandard Voltage-Controlled Oscillators

The receiver phase-noise requirements (dBc/Hz at 1MHz offset) for five different standards (i.e., DCS1800/WCDMA/WLAN–Bluetooth-DECT) are listed in Table 7.2 [7-11]. We will refer to the DCS1800 standard as a phase-noise demanding (PN-D) standard, to the WCDMA, WLAN and Bluetooth standards as phase-noise moderate (PN-M) standards, and to the DECT standard as a phase-noise relaxed (PN-R) standard.

Table 7.2: Multistandard/multi-band VCO requirements.

MSVCO	DCS1800	WCDMA	WLAN	Bluetooth	DECT
PN@1MHz [dBc/Hz]	-123	-110	-110	-110	-100

The bipolar VCO [1] shown in Fig. 7.7 is used to implement the multistandard adaptive oscillator. Compared to the oscillator of Fig. 7.1, the resonant-inductive degenerated (RID) tail-current source in Fig. 7.7 is implemented with degeneration inductor L_{RID}. Degeneration of the current source is necessary to minimize the phase noise contributed by the bias circuit

(Section 6.3.6; [12]). The oscillation signal is delivered to the measurement equipment (50Ω impedance) using an on-chip open-collector buffer and an external transformer balun, *TR*. Buffering the output from the bases of the transconductor transistors rather than from the LC-tank, the buffer can share the base bias voltage, thereby eliminating output coupling capacitors. Gain of the buffer is set by the emitter-degeneration resistance R_E.

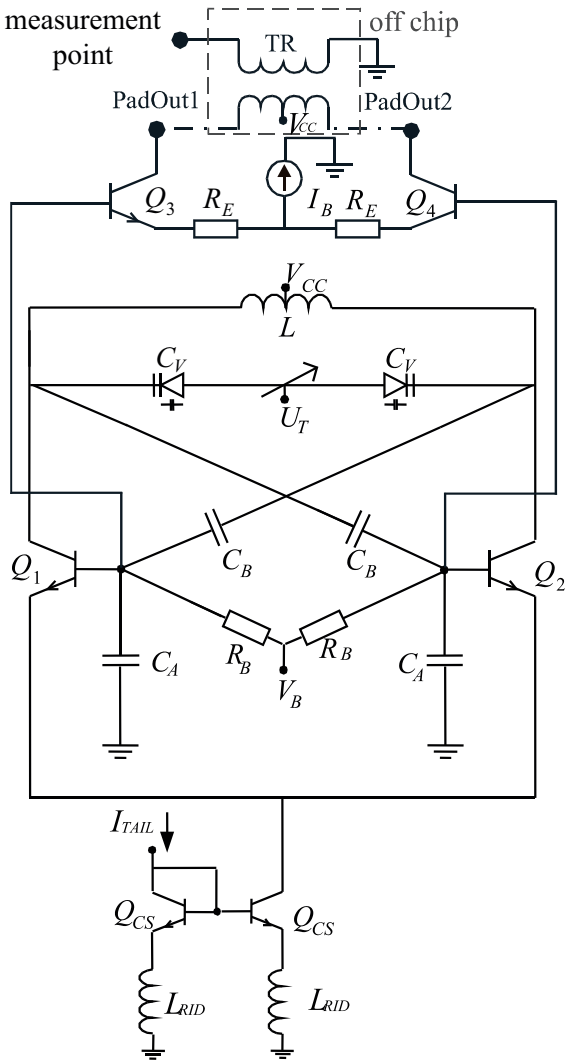

Figure 7.7: A resonant-inductive degenerated oscillator with an open-collector buffer.

Given the phase-noise requirements listed in Table 7.2, the phase-noise range between the demanding (PN-D) and moderate (PN-M) modes is *PNTR*=123-110-20log(2.4GHz/1.8GHz)=11dB. Taking into account the relaxed DECT mode (PN-R), the *PNTR* increases to 123-100-20log(2.4/1.8) =21dB. Therefore, a *PNTR* of 21dB is targeted.

After the effects of the noise from the biasing tail-current source are eliminating by means of RID (Eq. (6.27)), the minimum and the maximum loop gain and tail current can be estimated from Eq. (6.59). Using this intuitive model (see Section 6.3.5), a *PNTR* of 16.4dB is estimated between the loop gain k_{MIN}=2 and k_{MAX}=20. Taking into account device and noise bandwidth limitations, a *PNTR* of around 18dB is expected. However, as the resonant-inductive degeneration is constructed for the best phase-noise (thus around k_{MAX}), the reduced effect of the RID at k_{MIN} results expectedly in a larger *PNTR*, which may be sufficient to accommodate multiple standards.

Once the maximum loop gain is known, the oscillator bias point can be determined. The choice of the base-bias voltage V_B is a compromise between a large output voltage swing and saturation of transconductor devices Q_1 and Q_2 (see Fig. 7.7). For maximum loop gain and lowest phase noise, a voltage swing across the bases of the transconductor devices of $v_{S,B,MAX}$=1.2V is estimated from Eq. (6.9). Further, to avoid the saturation of the transistors in the active part of the oscillator, $v_{S,B}$ should satisfy Eq. (6.60), for the convenience given by Eq. (7.1) as well.

$$v_{S,B,MAX} \le 2\frac{V_{CC} - V_B + V_{BE} - V_{CE,SAT}}{n+1} \tag{7.1}$$

The worst-case condition is derived assuming the largest base and the lowest collector potential, and therefore insures proper operation of the transistors in the active part at all times. V_{CC}=3V is the supply voltage, V_{BE} is the base-emitter voltage, and $V_{CE,SAT}$ is the collector-emitter saturation voltage. For a capacitive divider ratio n of 1.4, a base potential V_B of 2.1V is finally obtained from Eq. (7.1).

7.2.2 Circuit Parameters of the Multistandard Adaptive Voltage-Controlled Oscillator

Tank inductor L=3nH is chosen as a compromise between low power consumption and high quality factor in the 2.1GHz band. The inductor is fabricated using 4um thick aluminum top metal in a 50GHz SiGe technology.

The 3-turn inductor has outer diameter d_{OUT}=320um, metal width w=20um and metal spacing s=5um. The differentially-shielded symmetric inductor uses a ladder metal filling scheme as shown in Fig. 7.8 [13]. This improves the peak Q-factor by 40% (Q_L=25 around 2.1GHz), but has only a minor effect on the inductor self-resonant frequency. It also satisfies the aggressive metal fill restrictions in modern VLSI backend technologies without compromising RF performance.

The quality-factor of the varactor can also limit the overall tank Q-factor in an integrated oscillator. The quality factor of the collector-base varactor is estimated at Q_C=40 from simulation. The varactor consists of two base-collector diodes with 32 fingers, each 4um wide and 20um long.

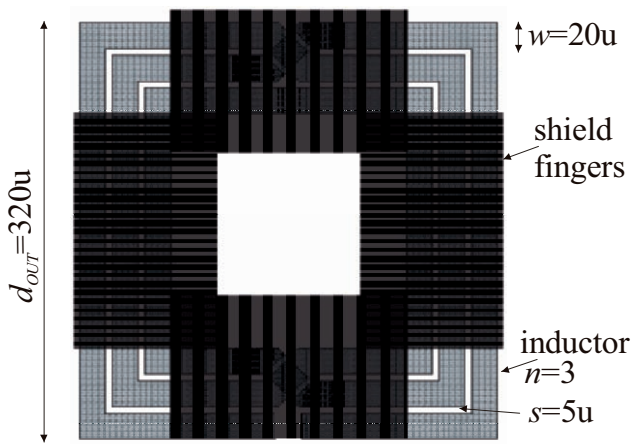

Figure 7.8: Shielded inductor layout (bottom view).

The metal-insulator-metal capacitances C_A=150fF (C_{IT}=90fF) and C_B=600fF are chosen for a capacitive-divider ratio of 1.4. For effective suppression of the tail-current source noise, L_{RID} is set to 3.4nH using the resonant-tuning design method outlined in Section 6.3.6. The degeneration inductor is realized in 0.85um thick second metal layer, as quality factor for this inductor is not of great concern. The inductor outer diameter is d_{OUT}=140um, metal width w=6um, metal spacing s=1um and it has seven turns.

Finally, the open-collector output buffer is designed with a linearization resistor R_E of 750Ω and a bias current I_B of 1.1mA.

7.2.3 Measurement Results for the Multistandard Adaptive Voltage-Controlled Oscillator

The chip photomicrograph of the multistandard VCO is shown in Fig. 7.9. It occupies an area of 700x970um^2, including bondpads. Wire-bonded in a 20 lead RF package, the chip is tested in a metal fixture with filtering on all bias and supply lines, as shown in Fig. 7.10. On the test printed-circuit board (PCB), three-stage low-pass LC filters remove low-frequency noise originating from the power supply and bias interconnections. Heavy filtering of the supply and bias lines is needed to remove spurs from the VCO output caused by pick-up from the supply and tuning lines. This unwanted interference would otherwise modulate the VCO in both phase and frequency making accurate phase-noise measurements impossible without filtering.

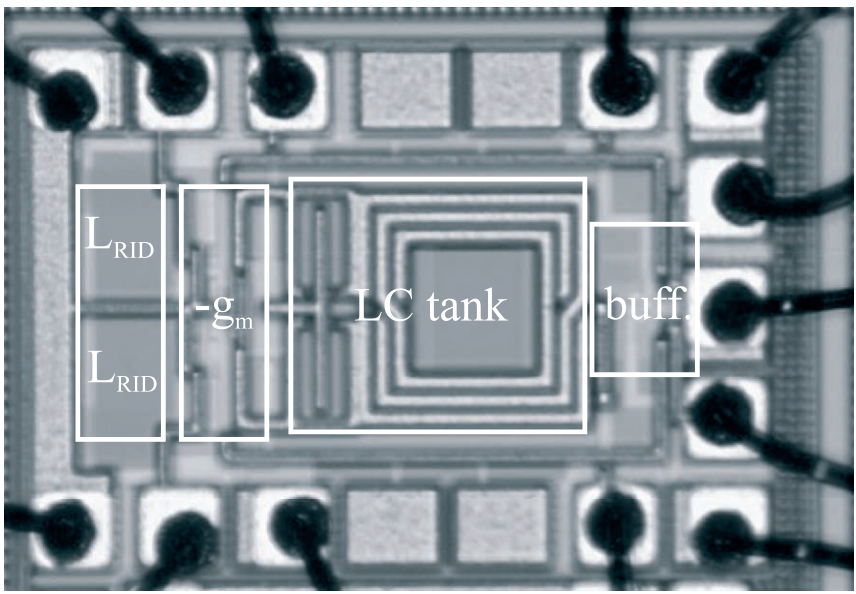

Figure 7.9: The photomicrograph of the multistandard VCO.

For a 3V supply, a frequency tuning range of 600MHz (i.e., output from 1.8GHz to 2.4GHz) is measured, as shown in Fig. 7.11. In order to relax the requirement of a large frequency tuning range from a variable capacitor, switched capacitor banks can be used [14]. They allow for switching between

frequency bands (standards), whereas varactors perform fine frequency tuning within a band. For example, the complete 2.4GHz band can be covered using this method.

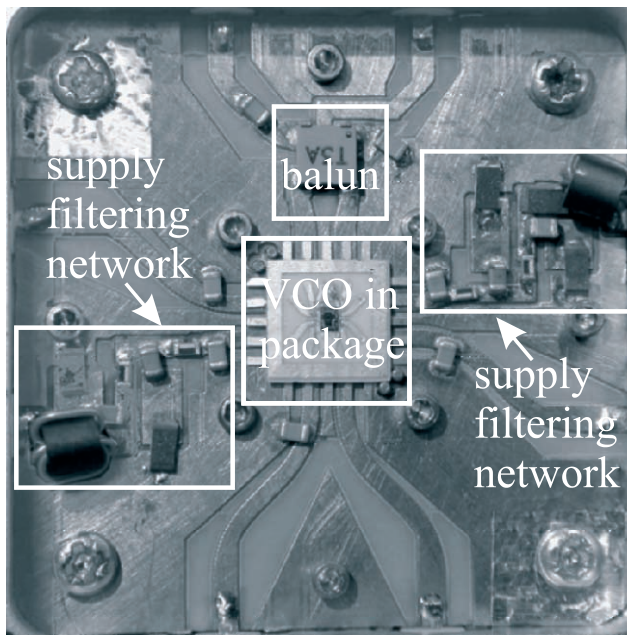

Figure 7.10: Packaged VCO IC on a PCB in a test fixture.

Plots of the measured phase noise at 1MHz offset in the 2.1GHz mid-frequency band is shown in Fig. 7.12. Due to low gain in the output buffer, an output signal in order of -20dBm (maximum) has been measured in a 50Ω system. This results in a noise floor for the phase-noise measurement of -130dBc/Hz, as seen in Fig. 7.12.

The operating conditions accompanying the measurements shown in Fig. 7.12 are listed in Table 7.3, with the loop-gain values estimated from the measured output power of the oscillation signal. As can be seen from this table, by adapting the bias tail current between 0.5mA/0.9mA and 6mA, a phase-noise tuning range of 20dB/15dB has been achieved. This satisfies the requirements of five different wireless standards, as desired. Note that by following the measured phase-noise slope in the range 100KHz-1MHz, a

phase noise better than -133dBc/Hz at a 3MHz offset is expected, fulfilling the stringent DCS1800 receiver requirement at this offset as well.

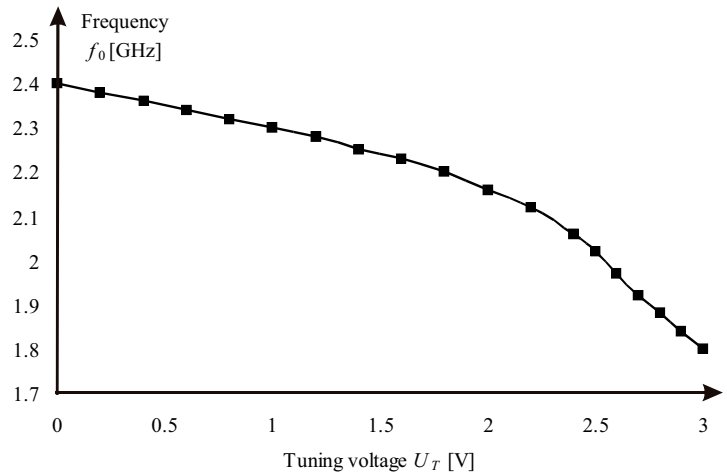

Figure 7.11: f_0-tuning curve for a 3V tuning voltage.

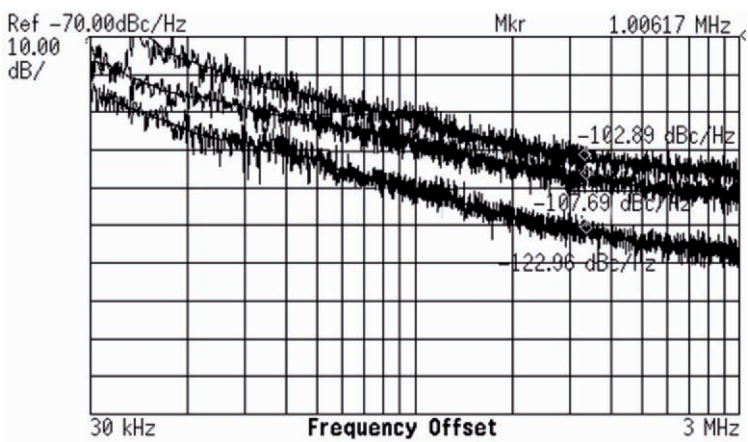

Figure 7.12: Phase noise at 1MHz offset in the 2.1GHz band.

The power-consumption figure of merit,

$$FOM1 = \mathcal{L}(\Delta f_{OFFSET} / f_0)^2 V_{CC} I_{TAIL} = 178\,, \tag{7.2}$$

and the tuning-range figure of merit,

$$FOM2 = FOM1(f_0 / \Delta f_{TUNE})^2 = 167\,, \tag{7.3}$$

of the oscillator under consideration have been realized. $\mathcal{L}$ stands for phase noise, Δf_{OFFSET} offset frequency, and Δf_{TUNE} tuning range. The adaptive VCO shows a good compromise between phase-noise and frequency-tuning performance. Referring to Leeson's phase-noise formula [15], Eq. (7.4),

$$\mathcal{L} = F \frac{KT}{2P_{SIGNAL}} \frac{1}{Q_{TANK}^2} \left(\frac{f_0}{\Delta f_{OFFSET}}\right)^2, \tag{7.4}$$

*FOM*2 appears to be a useful VCO figure of merit. It accounts for the frequency dependency of the phase noise as well as the power consumption and the tuning range of the oscillator, the latter related to the LC-tank *Q*-factor.

Table 7.3: Oscillator Performance in the 2.1GHz band.

PhaseNoise@1MHz	I_{TAIL}
-123dBc/Hz	6mA
-108dBc/Hz	0.9mA
-103dBc/Hz	0.5mA

The procedure of designing for adaptivity can be applied to any standard. The standards chosen in this exploratory design serve a proof of concept of designing for adaptivity and validate the feasibility of the design procedure outlined.

7.3 Multistandard Adaptive RF Front-Ends

Transceivers for multi-mode and multistandard telephony are mostly implemented by replicating the receiver for each operating band or standard

[6]. This allows applications such as GSM and WCDMA to operate concurrently (i.e., one can receive or make a call with either system at any time). Although high integration levels are possible in RF IC technologies, the increase in hardware required to implement this type of multistandard radio increases the total current consumption, thereby reducing the overall talk time. In such situations, the ability to share circuit functions between different standards in an adaptive multistandard receiver offers the advantages of reduced power consumption, less chip area, longer talk time, and, most importantly, has the potential for lower cost.

In this section, the results of an exploratory circuit design for a multi-mode adaptive image-reject downconverter (as a part of an RF receiver front-end) are described in the context of $2^{nd}/3^{rd}$ generation standards. The multi-mode adaptive (MMA) image-reject (IR) quadrature downconverter (QD) (oscillator and mixers) allows for adaptation between different modes of operation by trading RF performance for current consumption, which ranges from around 10mA for the relaxed mode (e.g., DECT) to around 20mA for the highest performance mode of operation (e.g., DCS1800). The quadrature downconverter (single-complex mixer-oscillator) has *IIP*3 of +5.5dBm, single-side band (SSB) *NF* of 13.9dB (50Ω) and conversion gain (voltage and/or power) of 1.4dB, while drawing 10mA from a 3V supply. The adaptive VCO achieves -123dBc/Hz and -103dBc/Hz phase noise at 1MHz offset in a 2.1GHz band for bias current levels of 6mA and 0.5mA, respectively.

The following section describes the selection of performance for multistandard adaptive RF front-end circuits. The design of the quadrature downconverter circuits used in the experimental implementation is then described. Finally, the measurement results are presented demonstrating that a 2:1 saving in power consumption is possible when adaptivity is employed.

7.3.1 System Considerations for Multistandard Adaptive RF Front-Ends

Concurrent operation of different wireless standards using a common receiver poses demands on performance (e.g., band selection, image-rejection and noise/power match prior to low-noise amplification) that are difficult to meet using a single RF path [16]. Therefore, multistandard receivers typically use duplicate circuit blocks, or even multiple RF front-ends (i.e., one for each standard).

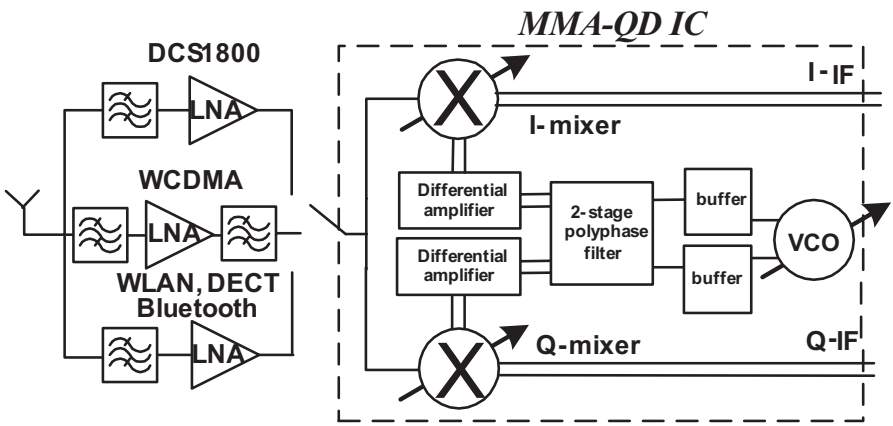

Figure 7.13: A multistandard receiver concept.

The multistandard receiver, shown in Fig. 7.13, is a compromise between these two approaches. Impedance matching, packaging and prefiltering requirements are relaxed and simplified by using multiple low-noise amplifiers. A single quadrature or image-reject downconverter can then be used to interface the RF and baseband sections of the receiver. An RF switch is used to select the standard of interest. If the VCO and mixer performance is adequate to cover the range of signals anticipated for each application, the downconverter enables a multistandard receiver realization with a single circuit block (the MMA-QD IC in Fig. 7.13).

Analog and digital baseband signal processing functions could be used to monitor quality of service (e.g., error rate of the detected bit sequences) and adjust the receiver parameters (e.g., tune a single bias current or multiple currents) in real-time to meet the requirements of a given standard.

The multi-mode adaptive downconverter may operate in zero-IF mode for all standards considered except the (200kHz) narrow-band DCS1800 standard, where low-IF operation would be favored. The MMA-QD test circuit consists of an adaptive voltage-controlled oscillator, oscillator buffers, a two-stage poly-phase filter to generate in-phase (I) and quadrature-phase (Q) local oscillator signals, mixer buffer amplifiers and dual balanced adaptive mixers, as illustrated in Fig. 7.13.

Using mixer-oscillator models (Section 3.3), a single-channel representation of the adaptive receiver (Fig. 7.13) is shown in Fig. 7.14, consisting of an LNA, a single-complex mixer-oscillator (SC-MO) and (quadrature) baseband circuitry. Referring to Fig. 7.14, we will discuss the procedure for the selection of the specifications for to the multistandard/multi-mode receiver blocks.

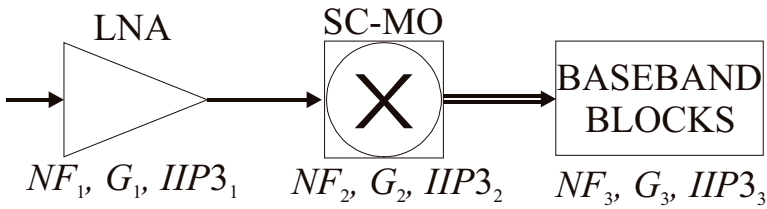

Figure 7.14: A simplified receiver model.

7.3.1.1 System Requirements for Multistandard Receivers

We consider the application of the design for adaptivity to multi-mode RF front-end circuits in the framework of the requirements of the standards listed in Table 7.5 [7-11, 17-20]. Situated between 1.8GHz-2.4GHz, these standards describe a scenario where second- and third-generation standards may co-operate in a single device. The standards considered are chosen to illustrate the feasibility of the application of the adaptivity design concept to multi-mode receivers. The procedure of designing for adaptivity presented in this section can be applied to any standard.

In the remainder of the section, we will refer to multiple modes of operation of the adaptive receiver shown in Fig. 7.13: with respect to noise-figure and linearity, the receiver operating modes are classified as *demanding*, *moderate* and *relaxed*, as given in Table 7.6.

In the context of the noise-figure and linearity requirements of the standards listed in Table 7.5, the demanding (D) mode of operation may be related to the DCS1800 and W-CDMA standards, the moderate (M) mode to the IEEE 802.11b WLAN standard, and the relaxed (R) mode to the Bluetooth and DECT standards.

Table 7.5: Requirements for different standards prior to an LNA.

MSAFE	**DCS1800**	**WCDMA**	**WLAN**	**Bluetooth**	**DECT**
f_0 [GHz]	1.8	2.1	2.4	2.4	2.4
NF [dB]	9 (D/M)	6 (D)	10 (M)	23 (R)	18 (R)
*IIP*3[dBm]	-9 (D)	-9 (D)	-12 (M)	-16 (R)	-20 (R)
PN@1MHz	-123 (D)	-110 (M)	-110 (M)	-110 (M)	-100 (R)

Table 7.6: Performance requirements for different modes (desired specs).

desired specification / mode	**D (demanding)**	**M (moderate)**	**R (relaxed)**
NF_D [dB]	6	10	18
$IIP3_D$ [dBm]	-9	-12	-16

Specifications for the multi-mode receiver blocks will be determined with the aid of Eqs. (4.3-4.7), (4.11-4.13), (4.15-4.18), and the procedure outlined in Chapter 4. Accordingly, the noise and linearity equilibrium points are determined first. Using Eqs. (4.5) and (4.15), and the inputs of Table 7.6, the equilibrium parameters are calculated as given by Table 7.7 (a three-block system of Fig. 7.14 is considered; n=3).

Table 7.7: Receiver equilibrium performance.

specification/mode	**demanding**	**moderate**	**relaxed**
NF'_E/NF_E [dB]	-0.2/2.9	4.5/5.8	13/13.2
$IIP3_E$ [dBm]	-4	-7	-11

Required specifications for receiver blocks in different modes of operation will be determined in the following sections with the aid of the equilibrium design requirements given in Table 7.7.

Design procedure for an adaptive multi-mode/multistandard circuit is different from design for a single standard. Figures of merit referring to a number of operating conditions and specifications are required for multi-mode designs, i.e., the adaptivity figures of merit. For oscillators, the phase-noise tuning range (Section 6.4) is used to specify the difference between the maximum and minimum achievable phase noise. Useful adaptivity figures of merit for mixers and amplifiers are the ranges of noise figure and the intercept point that are realized when a particular parameter, e.g., bias current, is adjusted (see Chapter 5).

Referring to Table 7.6 and Section 7.2.1 (Table 7.2), the phase-noise tuning range (*PNTR*), the noise-figure tuning range (*NFTR*), and the third-order input-intercept point tuning range (*IIP*3*TR*) are given in Table 7.8 for the multi-mode receiver.

Table 7.8: Tuning ranges of the desired performance parameters for the multi-mode receiver.

PNTR	*NFTR*	*IIP*3TR
21 dB	10 dB	7 dB

7.3.2 A Multi-Mode Adaptive Quadrature Signal Generator

The VCO shown in Fig. 7.7 (Section 7.2 and [1]) is used to implement the adaptive oscillator (without open-collector buffer shown in Fig 7.7). As the procedure for the selection of parameters of this adaptive VCO has already been discussed in detail in Section 7.2.1, in this section we will focus on the circuitry proceeding the VCO: two common-collector buffers, a polyphase filter (PPF) and two differential amplifiers, as shown in Fig. 7.15.

The common-collector buffers (Q_{CC}) are added as an interface between the polyphase filter and the oscillator (from bases of Q_1, Q_2 in Fig. 7.7). They consist of 0.5x1.7um^2 transistors and consume 1mA each.

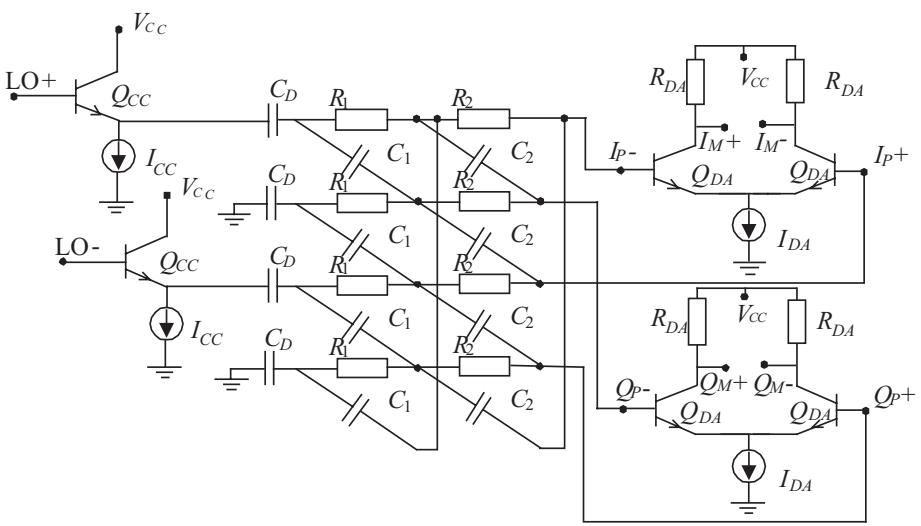

Figure 7.15: Buffers, a polyphase filter, and differential amplifiers.

The quadrature signals used to drive the mixers are derived from a two-stage polyphase filter. The first and second stage *R-C* filter sections provide rejection at 1.75 and 2.15GHz, respectively. This allows for more image-rejection in the 1.8GHz band where low-IF operation is presumed. Image-rejection requirements are relaxed around 2.4GHz, as the zero-IF operation is assumed in this band.

The attenuation of the passive polyphase filter necessitates a differential buffer amplifier for the oscillation signal before driving the mixer quad (Fig. 7.15). The buffer provides 160mV oscillation signal swing across while consuming 1.1mA of bias current.

7.3.3 A Multi-Mode Adaptive Quadrature Downconverter

In order to determine the required specifications for the MMA quadrature downconverter, we will apply the following procedure (see Chapter 4):

(a) determine the deviation (*A*) from the linearity and noise equilibrium performance for an LNA using Eqs. (4.11) and (4.16).

(b) determine the deviation (*B*) from the noise and linearity equilibrium performance for the quadrature downconverter (single-complex mixer-oscillator, SC-MO) using Eq. (4.7) and the deviation *A*.

(c) determine the linearity and noise performance for the quadrature downconverter using Eqs. (4.12) and (4.17) and the deviations *A* and *B*.

Without loss of generality, we will assume that the noise and linearity performance of the (quadrature) baseband circuitry is at equilibrium, i.e., C_{NF}=C_{IIP3}=0. Typical LNA performance is assumed (see Table 4.1): NF_1=2dB (NF'_1=-2.3dB), $IIP3_1$=1dBm and voltage gain (from source) VG_1=13dB (for example, for 50Ω source and load impedances).

In accordance with the design procedure proposed (steps (a-c)), deviations from the equilibrium of the LNA noise and linearity performance in different modes of operation are calculated from Table 7.7 (step (a)). The results are shown in Table 7.9.

Table 7.9: *NF* and *IIP*3 deviations from the LNA equilibrium point in different modes of operation.

deviation/mode	demanding	moderate	relaxed
$A_{NF'}$ [dB]	-2.1	-6.8	-15.3
A_{IIP3} [dB]	-5	-8	-12

Table 7.10 is generated from Table 7.9 (step (b)). It shows the difference between the desired and equilibrium performance for the quadrature downconverter.

Table 7.10: *NF* and *IIP*3 deviations from the equilibrium points of the quadrature downconverter in different modes of operation.

deviation/mode	demanding	moderate	relaxed
$B_{NF'}$ [dB]	1.4	2.5	2.95
B_{IIP3} [dB]	2.26	2.65	2.87

Finally, from the inputs of Tables 7.8, 7.9 and 7.10, the required noise and linearity performance for the quadrature downconverter (Fig. 7.14) are determined as given by Table 7.11 (step (c)).

Table 7.11: Required performance for the quadrature downconverter.

specification/mode	demanding	moderate	relaxed
NF'_2/NF_2[dB]	14.2/14.4	20/20	29/29
$IIP3_2$ [dBm]	6.74	3.35	-0.87

Now, the *NFTR* and *IIP*3*TR* of the quadrature downconverter can be determined from Table 7.11. When the *NF* and *IIP*3 of the downconverter are adapted between 14dB and 29dB, and 6.74dBm and -0.87dBm, respectively, the quadrature downconverter satisfies the requirements of different operating modes: $NFTR_2$ is 14.6dB, and $IIP3TR_2$ is 7.6dB

Assuming a voltage gain VG_2 of 0dB for the quadrature downconverter (from signal source; see Section 2.1), the typical performance for the baseband block (in the demanding mode) are obtained from Eqs. (4.13) and (4.18): NF_3'/NF_3 of 12.8dB/13dB and $IIP3_3$ of 7dBm (C_{NF}=C_{IIP3}=0dB) [21].

The results obtained confirm that the proposed specification-selection scheme imposes realistic (realizable) requirements on the receiver circuits, covering the requirements of different modes of operation.

Before closing the discussion on the selection of the specifications, we will shortly pinpoint the effects of second-order intermodulation (IM2) distortion on the linearity of the system. As IM2 products fall close to DC, they interfere with the desired signal in zero-IF receivers (together with IM3 products).

However, the distribution of *IIP*2 to the receiver building blocks is somewhat different from the *IIP*3 distribution. Namely, the IM3 products lying in the desired signal band pass from an LNA to a mixer, whereas the IM2 products from an LNA could be filtered by, for example, a resonating LNA load or AC-coupling between the LNA and mixer. Therefore, the *IIP*2 specifications of the mixer (or SC-MO in Fig. 7.14) determine this type of distortion for a complete receiver. Typically, a receiver *IIP*2 in excess of 45dBm would suffice for the standards under consideration (i.e., a SC-MO *IIP*2 of 58dBm for the assumed LNA gain) [22].

7.3.3.1 Mixer Circuit Parameters

The schematic of the double-balanced mixer that is used to implement the quadrature downconverter is shown in Fig. 7.16 [23].

The mixer consists of a class-AB input stage ($Q_{M1\text{-}M4}$) for improved linearity, cascoded by the switching quad $Q_{M5\text{-}M8}$. The single-ended input is converted into a differential current via common-base stage Q_{M1} and current mirror Q_{M2}, Q_{M3}. Distortion is further suppressed and the RF input impedance match improved by resistors R_{M1}-R_{M4}. Transistor Q_{M4} improves isolation in the input stage and attenuates local oscillator leakage to the RF input.

The transistors and resistors are sized to optimize conversion gain, noise figure, and linearity. For the mixer input stage, transistors $Q_{M1\text{-}M4}$ have a length/width ratio of 40um/0.5um and resistors $R_{M1\text{-}M4}$ are 21Ω. For the switching quad, transistors $Q_{M5\text{-}M8}$ have a length/width ratio of 8um/0.5um. The mixer performance parameters can be adaptively adjusted by changing the mixer bias current, which is set by the voltage applied to the bases of Q_{M1} and Q_{M4}.

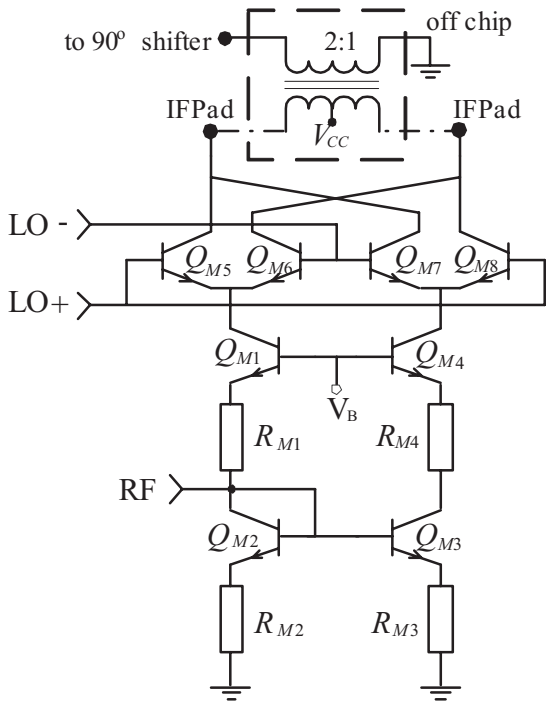

Figure 7.16: Mixer schematic.

Simulations show that a factor of two reduction in power consumption can be achieved between the moderate and demanding modes of operation for the mixer.

7.3.4 Experimental Results for the Multi-Mode Adaptive Image-Reject Downconverter

The 0.65x1.0mm^2 MMA-IR testchip (excluding bondpads), shown in Fig. 7.17, is wirebonded into a 32-pin quad package for testing [24]. A custom printed-circuit board (see Fig. 7.18) with bias and supply line filtering was designed for testing.

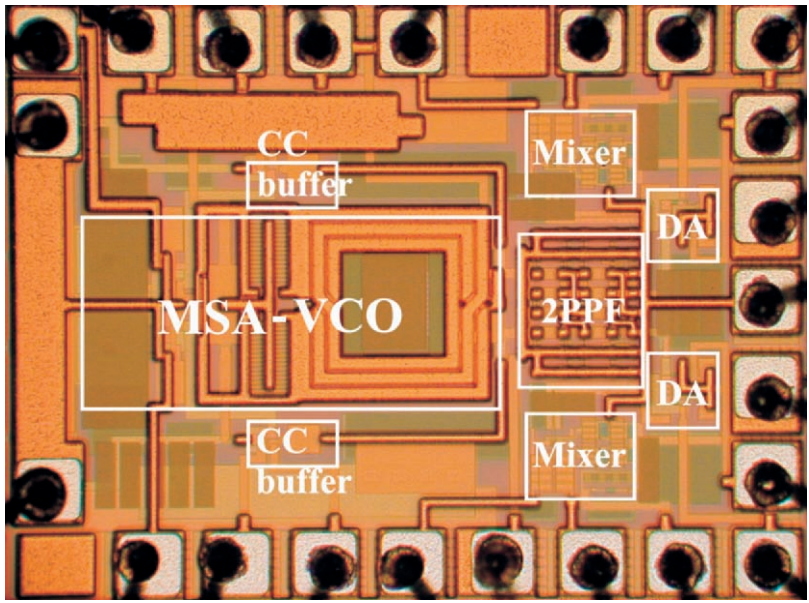

Figure 7.17: MMA-IR IC photomicrograph.

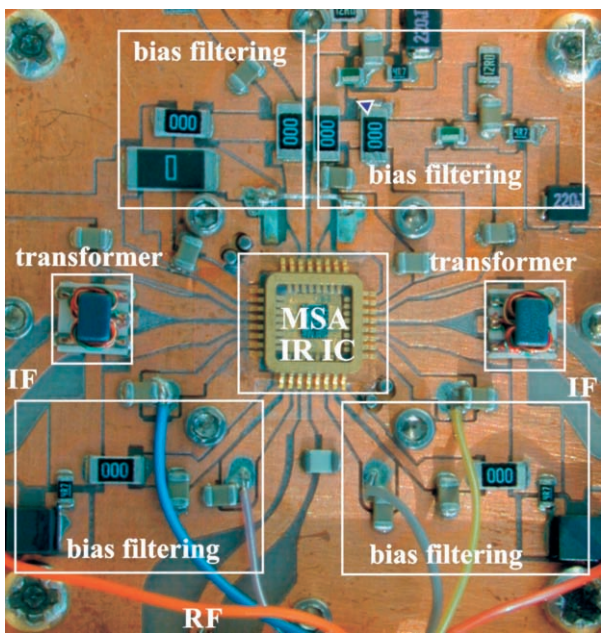

Figure 7.18: Packaged IC on PCB test fixture.

The differential quadrature IF signals (*I* and *Q*) are converted to single-ended form via external transformers with a 2:1 turns ratio, giving an effective mixer load of 200Ω. A 50Ω quadrature hybrid (70MHz IF) is then used for final IF signal combining.

The VCO performance was characterized using a separate test circuit [1]. Operating from a 3V supply, the adaptive VCO achieves a tuning range of 600MHz, ranging from 1.8GHz to 2.4GHz. A plot of the phase noise measured in the 2.1GHz band is shown in Fig. 7.18. The operating conditions are summarized in Table 7.12.

Table 7.12: Measured multi-mode VCO performance in a 2.1GHz band.

PhaseNoise@1MHz	-123dBc/Hz	-103dBc/Hz
I_{TAIL} [mA]	6 (D)	0.5 (R)

By adapting the bias tail current between 0.5mA and 6mA, a phase-noise tuning range of 20dB is achieved, which satisfies the requirements of different operating modes (i.e., standards). In addition, the VCO allows a factor of 12 reduction in power consumption when tuned from the demanding mode (e.g., DCS1800) to the relaxed mode (e.g., DECT).

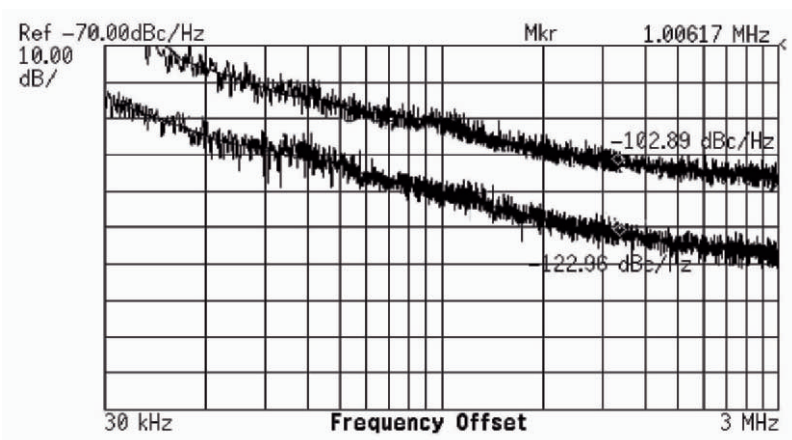

Figure 7.19: Phase noise at 1MHz offset in a 2.1 GHz band in different modes of operation.

After de-embedding the measurement results of the test set-up, shown in Fig. 7.20 (see circuit schematics for the notation), the MMA-IR downconverter performance parameters have been determined for the demanding mode of operation.

The measured SSB noise figure of the quadrature downconverter is 13.9dB in the demanding mode of operation, while drawing 10mA of bias current.

The linearity is characterized by an $IIP3_2$ of 5.5dBm. IIP3 can be traded off for NF, a larger oscillator voltage swing reduces mixer noise figure, but can degrade its linearity, whereas a lower gain of the LNA improves receiver linearity but degrades its noise figure.

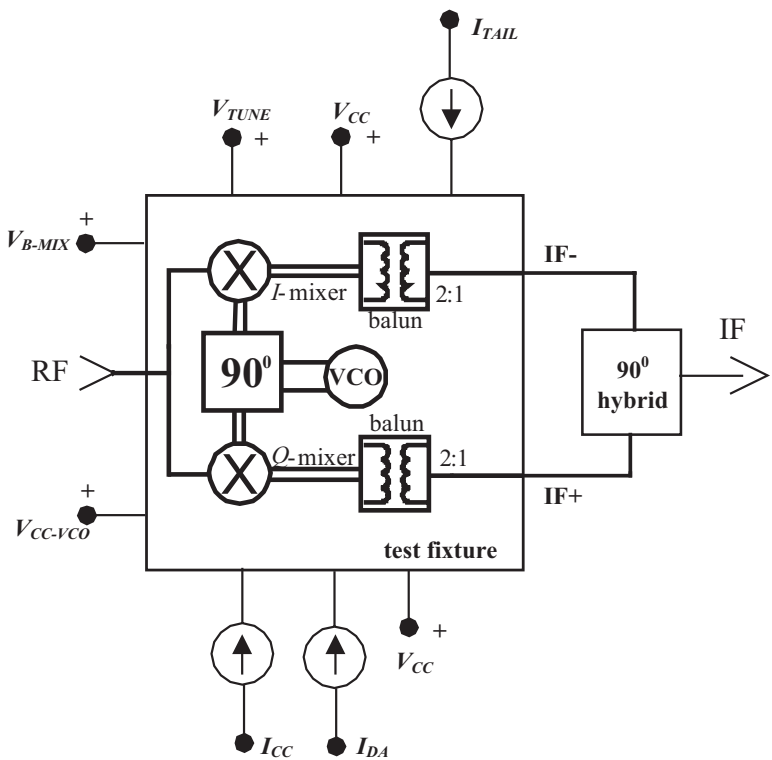

Figure 7.20: A block diagram of the test setup.

The measured $IIP2_2$, important for zero-IF operation, is 51dBm. An improvement of around 5dB can be expected after low-frequency baseband filtering [19,20]. Moreover, increasing the amplitude of the applied quadrature

VCO signals (at the cost of increased power consumption of the VCO and/or differential amplifiers) improves the second-order intermodulation distortion [25].

On-package capacitors on the output signal lines (10pF at each IF output) filter high-frequency output signals, and for the 70MHz IF used in testing, they attenuate the desired signal. Therefore, at the IF of the standards considered (MHz order), the total gain of the image-reject quadrature downconverter is estimated to be around 3dB better and equals 1.4dB. An even larger gain can be achieved if larger mixer load impedance is used.

The measured image-rejection of 20dB is satisfactory for the zero-IF mode of operation. For the low-IF operation, a better image-rejection would be required. It can be improved if the quadrature combining is implemented on-chip at baseband (or in a digital back-end), or if a three-stage polyphase filter is implemented for oscillator quadrature signal generation.

Isolation between the oscillator port of the quadrature downconverter and the input (RF) port is 45dB.

The quadrature downconverter consumes 10mA in the demanding mode.

Control of the circuits' bias currents could be realized by additional baseband circuitry. The hypothetical multi-mode receiver has the potential to meet the system specifications in the demanding mode as summarized in Table 7.13 (see Section 7.3.3).

Table 7.13: Hypothetical receiver performance in the demanding mode.

Performance	**LNA**	**IR-QD**	**Baseband**
VG [dB]	13	1.4	-
NF [dB]	2	13.9	13
*IIP*3 [dBm]	1	5.5	11

The total power consumption of the MMA-IR downconverter testchip (comprising the VCO, two mixers and buffers) is varied from mode to mode. Due to relaxed requirements in the R-mode, a considerable power consumption reduction can be realized with sufficient functionality. By trading power consumption for performance in an adaptive way, this multi-mode adaptive image-reject downconverter offers more than a factor of two reduction in power/current consumption between demanding and relaxed modes of operation, from around 60mW to 30mW.

7.3.5 Back-Annotation of Specifications to Receiver Circuits

In this section we will determine the performance parameters for an LNA and baseband circuitry according to the requirements of the 2.1GHz-WCDMA standard [8], given the specifications of the quadrature downconverter in the demanding mode (see Section 7.3). We will refer to a three-block receiver model shown in Fig. 7.14 and apply the selection procedure outlined in Chapter 4.

The noise and linearity requirements for 2.1GHz-WCDMA standard are taken from Table 7.5 as: NF_D=6dB=10logF_D (NF'_D=10log(F_D-1)=4.8dB), and $IIP3_D$=–9dBm. The measured performance of the quadrature downconverter is NF'_2=13.7dB, $IIP3_2$=5.5dBm, and G_2=1.4dB.

We will first calculate the equilibrium noise and linearity points of the receiver (a). Then, we will select two sets of specifications (b): the *NF'* and *IIP*3 for the circuits at the noise equilibrium (i.e., A_{NF}=B_{NF}=C_{NF}=0dB), and the *NF'* and *IIP*3 for the circuits at the linearity equilibrium (i.e., A_{IIP3}=B_{IIP3}=C_{IIP3}=0dB). A final choice of performance is then made by trading off between the two equilibrium specifications obtained (c).

(a) With the aid of Eqs. (4.5) and (4.15), the equilibrium design point of the receiver is calculated as NF'_E = 0dB (NF_E=3dB) and $IIP3_E$=–4.2dBm.

(b) For all the receiver circuits at the noise equilibrium, gain of the LNA is determined from Eq. (4.17) as G_1=13.7dB (F_2, F_E and B_{NF} are known). For the LNA at the linearity equilibrium, A_{IIP3}=0dB, B_{IIP3}=4dB is obtained from Eqs. (4.12), whereas Eq. (4.13) is not satisfied even for C_{IIP3}=-∞. This suggests that the quadrature downconverter has poor linearity performance to satisfy both the noise and linearity equilibriums of the LNA. Its positive linearity deviation from the equilibrium of 4dB implies that the downconverter linearity is more relaxed than allowed. We would come to the same conclusion by referring to Fig. 4.2: for A_{IIP3}=0dB and C_{IIP3}=-∞, B_{IIP3} has to be 3dB, or in other words, a design point A_{IIP3}=0dB and B_{IIP3}=4dB is outside of the design space (the shaded area of Fig. 4.2).

For the noise equilibrium, the noise and linearity specifications of receiver circuits are summarized in Table 7.14, with the aid of Eqs. (4.11-4.13) and (4.16-4.18). Note that the baseband *IIP*3 is not specified as even a theoretical intercept point of +∞dBm would not be satisfactory in this case.

Table 7.14: Performance of receiver circuits for the noise equilibrium and G_1=13.7dB.

block/specification	***NF'* [dB]**	***NF* [dB]**	***IIP*3 [dBm]**
LNA	0	3	-4.2
downconverter	13.7	13.9	5.5
baseband circuitry	15.1	15.2	…

Similarly, for all the receiver circuits at the linearity equilibrium, gain of the LNA is determined from Eq. (4.12) as G_1=9.7dB. For the LNA at the noise equilibrium, A_{NF}=0dB, B_{NF}=4dB is obtained from Eq. (4.17), whereas Eq. (4.18) is not satisfied even for C_{NF}=-∞. Thus, the quadrature downconverter has poor noise performance to satisfy both the noise and linearity equilibriums of the LNA.

For the linearity equilibrium, the noise and linearity specifications of the receiver circuits are summarized in Table 7.15, with the aid of Eqs. (4.11-4.13) and (4.16-4.18).

Table 7.15: Performance of receiver circuits for the linearity equilibrium and G_1=9.7dB.

block/specification	***NF'* [dB]**	***NF* [dB]**	***IIP*3 [dBm]**
LNA	0	3	-4.2
downconverter	13.7	13.9	5.5
baseband circuitry	…	…	6.9

(c) As an LNA gain of G_1=13.7dB is too large to satisfy the linearity specification of a WCDMA receiver (we look for realizable baseband circuitry with $IIP3_3$<+∞), and a gain of G_1= 9.7dB is too low to satisfy its noise requirements (we look for a realizable baseband circuitry with NF'_3>-∞, thus NF_3>0dB), we opt for a gain of G_1=11.7dB, as a compromise between the two equilibrium points. Having failed to satisfy the system requirements for the LNA at the noise and linearity equilibriums, the gain chosen requires an LNA with better noise and linearity performance.

In this situation, the noise and linearity specifications for the LNA, downconverter and baseband circuitry are given in Table 7.16.

Table 7.16: Performance of receiver circuits for an LNA gain of G_1=11.7dB.

block/specification	***NF'/NF* [dB]**	***IIP*3 [dBm]**	A_{NF}, B_{NF} , C_{NF} [dB]
LNA	-3.8/1.5	-0.4	A_{IIP3}=A_{NF}=-3.8
downconverter	13.7/13.9	5.5	B_{IIP3}=B_{NF}=2
baseband circuitry	15.1/15.2	6.9	C_{IIP3}=C_{NF}=0

Given the specifications of the downconverter designed, the typical performance requirements are obtained for the LNA and baseband circuitry [21]. This confirms that the proposed specification-selection procedure imposes realistic and realizable requirements on the receiver circuits, even for the demanding WCDMA standard.

7.4 Conclusions

In singlestandard applications, adaptivity can be utilized as a power saving mechanism, thereby enhancing the overall receiver performance. In multistandard applications, sharing functional blocks between different standards using adaptive multi-band/multistandard circuits offers reduced power consumption and chip area, and may reduce overall cost.

A proof-of-concept 800MHz adaptive voltage-controlled oscillator design has been described in this chapter, allowing for a phase-noise tuning range of 7dB and more than a factor three saving in power consumption.

A $2^{nd}/3^{rd}$ generation multi-mode multistandard adaptive VCO design has also been presented. It satisfies the demanding and relaxed phase-noise requirements of different standards at 18mW and 1.5mW power consumption, respectively.

The exploratory multi-mode adaptive image-reject downconverter test circuit designed satisfies the requirements of the demanding $2^{nd}/3^{rd}$ generation standards in the 1.8GHz-2.4GHz band at current consumption of around 20mA.

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Appendix A

REAL-TO-COMPLEX-TO-REAL SPECTRUM-SIGNAL TRANSFORMATION

An application of the introduced SC-MO models is found in the Weaver architecture [1] shown in Fig. A.1a. Using two SC-MO models, this topology can be presented by Fig. A.1b. Here, both conversions take place, i.e., a real-to-complex and a complex-to-real conversion with the corresponding SC-MO models.

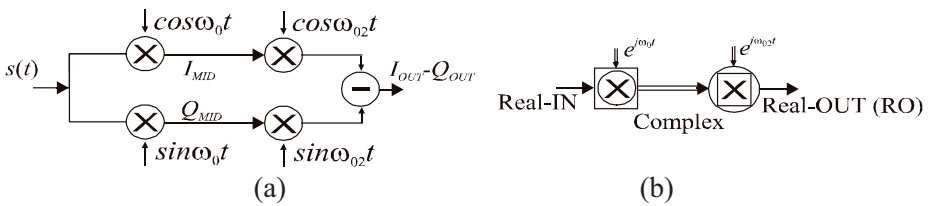

Figure A.1: (a) The Weaver architecture, (b) mixer-oscillator model.

Applying the SC-MO SS presentation models, the input real signal is downconverted first to a complex signal and then back to a real signal, as shown in Fig. A.2. The final SS form is a complex presentation of the real output signal. As expected, the desired signal component can be successfully detected from the downconverted signal (*A-jB*).

The validity of the SC-MO models will be examined by performing the conversion using DR-MO models according to the scheme that is shown in Fig. A.1a.

First, the real input signal $s(t)$ (Fig. 3.9) is converted by the LO signal (Fig. 3.10) into two real signals (I_{MID} and Q_{MID}) as shown in Figs. 3.11 and 3.12 as well as Figs. A.3a and A.3b (SS presentation).

The SS form of I and Q signals (I_{OUT} and Q_{OUT}) after the second down-conversion with the DR-MOs, but before the summation, is shown in Fig. A.4.

Finally, combining the signals I_{OUT} and Q_{OUT} (their contents) from Fig. A.4, the finally downconverted signal has the SS form as given by Fig. A.5.

As the obtained result (the signal content is $(A\text{-}jB)/2$ in Fig. A.5) is the same as the result shown in Fig. A.2 (the signal content is $(A\text{-}jB)/2$), the validity of the introduced SC-MO models is due.

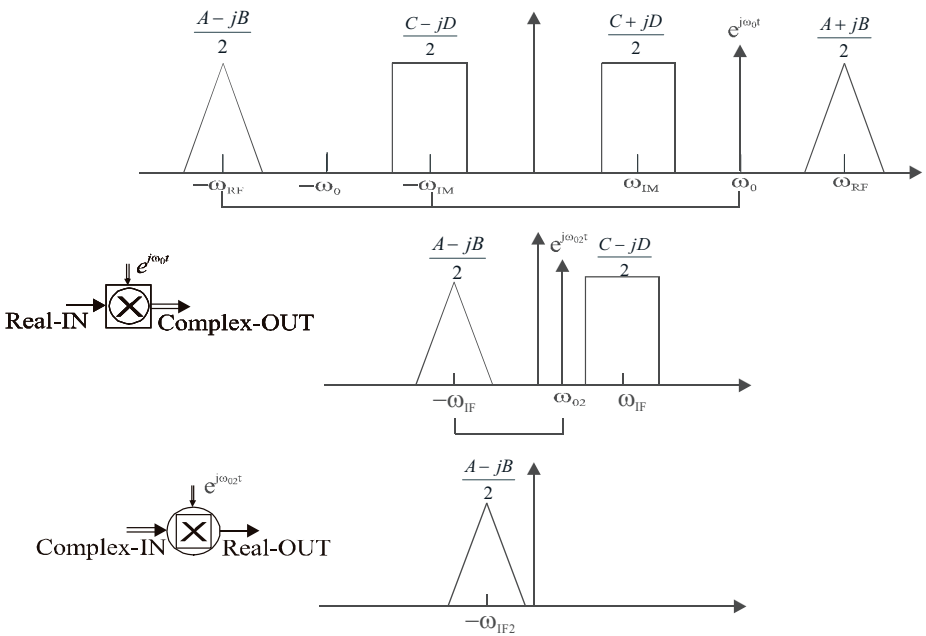

Figure A.2: SS transformation for the Weaver architecture.

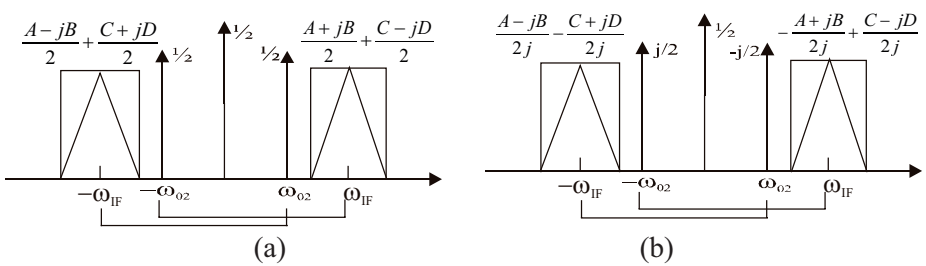

Figure A.3: Spectrum-signal form after the first downconversion (Fig. 3.27)
a) I_{MID} path, b) Q_{MID} path.

Finally, the content of the output real signal shown in Fig. A.5 is

$$\mathrm{RO} = \frac{A - jB}{4} e^{-j\omega_{IF2}t} + \frac{A + jB}{4} e^{j\omega_{IF2}t}, \tag{A.1}$$

$$\mathrm{RO} = \frac{A}{2}\cos\omega_{IF2}t - \frac{B}{2}\sin\omega_{IF2}t, \tag{A.2}$$

where ω_{IF2} is the final intermediate angular frequency. As can be seen from Eq. (A.2), only the desired signal is obtained while the image signal is rejected, as expected from the Weaver architecture.

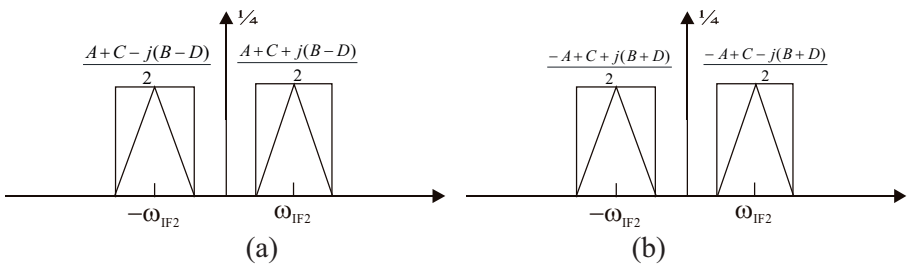

Figure A.4: Spectrum-signal form after the second downconversion a) I_{OUT} path, b) Q_{OUT} path.

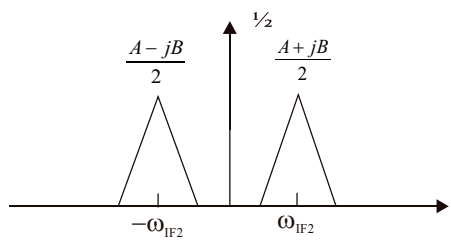

Figure A.5: I_{OUT} -Q_{OUT}= I_{OUT} +*j*(*j* Q_{OUT}).

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Appendix B

TRANSFORMER-FEEDBACK DEGENERATION OF LOW-NOISE AMPLIFIERS

A concept of transformer-feedback degeneration (TFD) is described, offering the possibility for low-noise amplifiers to achieve matching of both the real and the imaginary part of the input impedance in an orthogonal way [1]. The schematic (model) of a transformer-feedback degenerated low-noise amplifier is shown in Fig. B.1 (without a complete bias scheme).

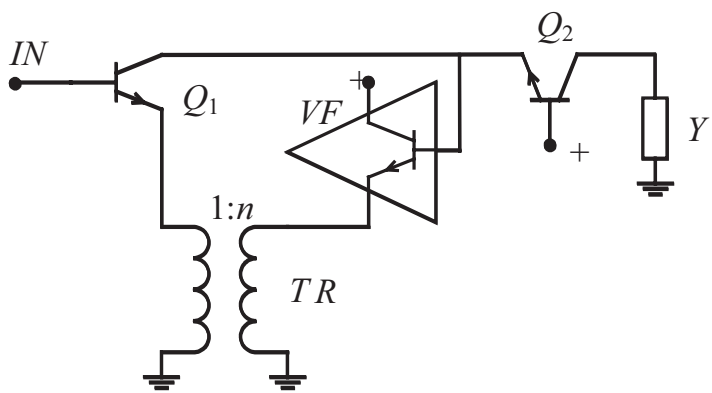

Figure B.1: A Model of a transformer-feedback degenerated LNA.

This amplifier topology is a traditional cascode configuration, with the addition of the feedback around the input transistor, which is realized by means of a voltage-follower (VF) (e.g., a single transistor in a common-collector configuration) and a transformer TR (orientation of the transformer is not shown; either negative of positive coupling is realized).

Controlling the amount of feedback, the TFD-LNA achieves orthogonal match of input impedance to source impedance. What is more, the power

match is rather independent of the transistor transit frequency (f_T), accordingly allowing for the matching even at very high f_Ts [2].

In the remainder of this appendix, we will derive input-impedance and power-matching models for a TFD-LNA.

B.1 Input-Impedance Model of Transformer-Feedback Degenerated Low-Noise Amplifiers

The input circuit of the TFD-LNA is shown in Fig. 5.3, where for the TFD topology, Y_E stands for the equivalent admittance seen at the emitter of transistor Q_1.

The equivalent circuit of the transformer-feedback degenerated LNA that is used for the calculation of the feedback function f, with a simplified transformer model [3,4], is shown in Fig. B.2: L_1 and L_2 are the transformer primary and secondary inductors, n is the transformer turn ratio, and k the coupling factor between the transformer inductors.

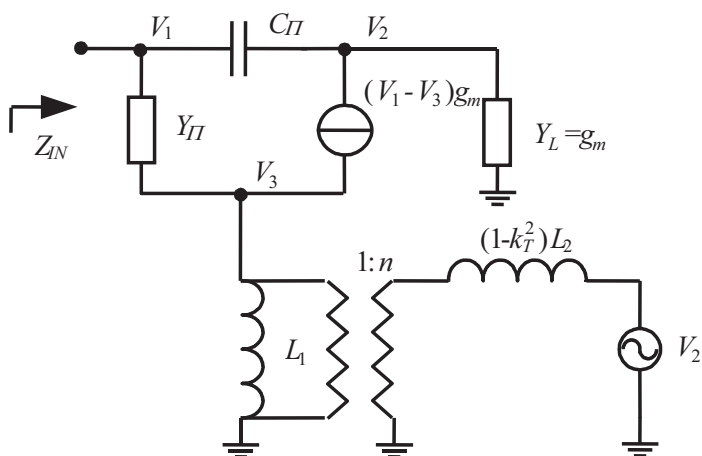

Figure B.2: Detailed schematic of a TFD-LNA.

As the primary and the secondary inductors of the transformer *TR* are by definition related as $L_2/L_1 = n^2/k^2$, it is straightforward to calculate the voltage

transfer function from node V_1 to node V_3, and subsequently derive the function $f(Y_1, Y_2)$ as

$$f(Y_1, Y_2) = \frac{Y_1 + n^2 Y_2}{Y_{IT} + Y_1 + n^2 Y_2 + g_m(1 \pm nY_2 / Y_L)}, \tag{B.1}$$

with $Y_1=1/(sL_1)$ and $Y_2=1/(s(1-k^2)L_2)$.

Depending on the orientation of the transformer, the feedback can be either negative or positive, which is the origin of a ± sign in Eq. (B.1). Note that the properties of the function $f(Y_1, Y_2)$ depend on the transformer parameters.

With the aid of Eqs. (6.1) and (B.1), the input impedance $Z_{IN}=1/Y_{IN}$ (with the condition $C_\mu=0$) becomes

$$Z_{IN}\Big|_{C_\mu=0} = R + j\left[\frac{\omega}{\omega_T}R \pm \frac{\omega_T}{\omega}\frac{k^2}{n}\frac{1}{g_m} - \frac{\omega_T}{\omega}\frac{1}{g_m}\right]. \tag{B.2}$$

$R=\omega_T(1-k^2)L_1$ stands for the real part of the input impedance, with $\omega_T=2\pi f_T$ and $\omega=2\pi f$ being the angular transit and input signal frequencies.

A circuit equivalent of Eq. (B.2) is shown in Fig. B.3: Fig B.3a for a positive feedback, and Fig. B.3b for a negative feedback.

Fig. B.3 shows that the effect of the transformer feedback is the additional reactance at the input of the TFD-LNA, i.e., a capacitance in case of negative feedback and an inductance in case of positive feedback.

We will calculate loop gain of the TFD-LNA to examine its stability (this topology employs a positive feedback for an additional feedback inductance (X_{FD} in Fig. B.3a). In order to evaluate the loop gain of the TFD-LNA, shown in Fig. B.1, we will refer to the detailed schematic of Fig. B.2, with a difference of a source resistance R_S added at the input and the voltage-controlled current source $g_m V_{BE}$ replaced with an uncontrolled current source I.

The loop gain can be determined from the transfer function between the current source I and the base emitter voltage V_{BE}. For the "critical" positive feedback, the loop gain (modulus squared) is calculated as

$$|LG|^2 = \left|\frac{g_m V_{BE}}{I}\right|^2 \cong \frac{k^2/n + (g_m R\omega/\omega_T)^2}{1 + (g_m R\omega/\omega_T)^2}. \tag{B.3}$$

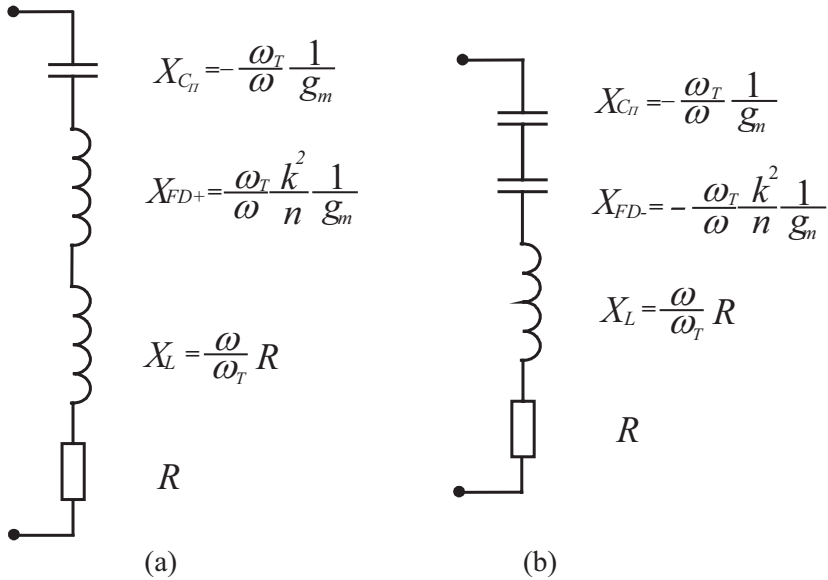

Figure B.3: Input impedance for $C_\mu = 0$
(a) positive feedback model, (b) negative feedback model.

As for safe operation of the amplifier its loop gain should be below one, this condition reduces to

$$k^2 / n < 1, \tag{B.4}$$

which indicates that for stabile amplifier operation, the transformer turn ratio should be larger than the square of the coupling coefficient k.

B.2 Power-Matching Condition for Transformer-Feedback Degenerated Low-Noise Amplifiers

With the aid of the input-impedance model for a slightly positive feedback (Fig. B.3a), the equivalent input circuit of the amplifier can be shown as depicted by Fig. B.4, where R_S is the impedance of the source (e.g., antenna).

The condition for the match of the real part of the input impedance to the source impedance is derived from Eq. (B.2) as

$$\omega_T(1-k^2)L_1 = R_S\,. \tag{B.5}$$

The impedance match is possible even at high f_Ts for a moderate value of primary inductance L_1 (with a larger coupling coefficient k).

On the other hand, setting the imaginary part of the input impedance to zero is facilitated, simply because the feedback-resulting inductance L_{FD} (Fig. B.3a and Eq. (B.6)) enables the cancellation of the transistor reactive part, i.e., the capacitance C_{Π}.

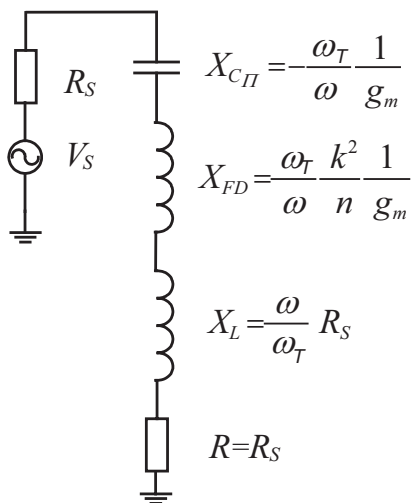

Figure B.4: Antenna and input-impedance models of a TFD-LNA.

$$L_{FD} = \frac{\omega_T}{\omega}\frac{k_T^2}{n}\frac{1}{g_m} \tag{B.6}$$

The matching condition is derived from Eq. (B.2), by setting the imaginary part to zero,

$$\frac{k^2}{n} = g_m\left[\frac{1}{g_m} - (\frac{\omega}{\omega_T})^2 R_S\right]. \tag{B.7}$$

This condition implies that the stability criterion (Eq. (B.4)) is not violated. What is more, a small input bond-wire inductance, relaxes the loop-gain constraint to the extent that inherent stability is achieved.

For example, for a 50Ω input impedance match, using technology with f_T=100GHz, an inductance of 0.075nH is required for an ID-LNA, whereas in the case of a TFD-LNA with a transformer coupling coefficient k=0.9, a primary inductance of 0.39nH suffices.

B.2.1 Transformer Power-Matching Model

Another property of the proposed topology is the orthogonal match of real and imaginary parts of input impedance to source impedance. As given by Eq. (B.5), by choosing a certain value for the coupling factor k and the primary inductance of the transformer L_1, the real part of the input impedance equals source resistance. On the other hand, by choosing the right value for the transformer turn ratio n, according to Eq. (B.7), the imaginary part is set to zero (for the power match to real source impedance).

The matching conditions (Eqs. (B.5) and (B.7)) can be translated into a transformer-parametric model that is shown in Fig. B.5, where model parameters E and D are expressed as

$$E = \frac{R_S}{\omega_T}, \tag{B.8}$$

and

$$D = 1 - g_m R_S \left(\frac{\omega}{\omega_T}\right)^2. \tag{B.9}$$

This transformer model is suitable for simulation (design) purposes, where the real part of the input impedance is controlled by the parameter E, and the imaginary part depends on the parameter D.

A favorable property of the transformer-feedback degeneration is that once the values for E and D are properly chosen, amplifier matching becomes independent of the coupling coefficient k. Namely, from the model shown in Fig. B.5, the choice of k determines only the primary and secondary inductance values. Only if k=0, i.e., there is no coupling, the transformer-feedback degeneration reduces to the inductive degeneration.

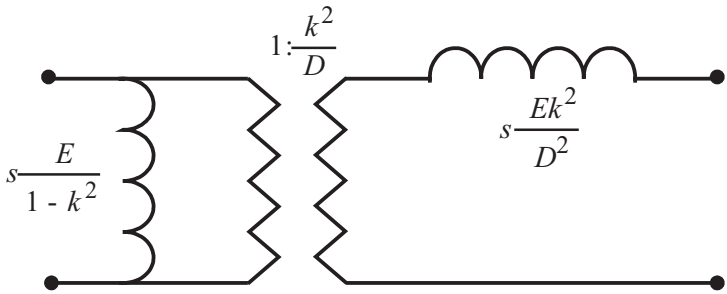

Figure B.5: Transformer power-matching model ($s=j\omega$).

Example B.1:

The operating conditions for the TFD-LNA are: a transition frequency f_T=24GHz, a frequency of operation f=2.4GHz and a collector current I_C=7mA.

With the aid of Eqs. (B.5) and (B.7), the corresponding 50Ω matching parameters are given by Table B.1.

Table B.1: Parameters of the power-matched TFD-LNA.

LNA \ parameter	***k***	***E*** [*e*-9]	***D***	L_1 [nH]	L_2 [nH]	***n***
TFD1	0.9	0.33	0.86	1.74	1.9	0.95
TFD2	0.7	0.33	0.86	0.66	0.47	0.6
TFD3	0.5	0.33	0.86	0.44	0.16	0.3

The results show that in the case of the transformer degeneration, power matching is possible not only for one, but for a number of different transformer parameters values. In addition, the parameters E and D of the transformer power-matching model (Fig. B.5) are indeed constant and the final choice of a primary and a secondary inductance of a transformer depends only on the factor k.

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