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Electrical Insulation Weaknesses in Wide Bandgap Devices

Mona Ghassemi

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Abstract

The power electronics research community is balancing on the edge of a game-changing technological innovation: as traditionally silicon (Si) based power semiconductors approach their material limitations, next-generation wide bandgap (WBG) power semiconductors are poised to overtake them. Promising WBG materials are silicon carbide (SiC), gallium nitride (GaN), diamond (C), gallium oxide (Ga_2O_3) and aluminum nitride (AlN). They can operate at higher voltages, temperatures, and switching frequencies with greater efficiencies compared to existing Si, in power electronics. These characteristics can reduce energy consumption, which is critical for national economic, health, and security interests. However, increased voltage blocking capability and trend toward more compact packaging technology for high-power density WBG devices can enhance the local electric field that may become large enough to raise partial discharges (PDs) within the module. High activity of PDs damages the insulating silicone gel, lead to electrical insulation failure and reduce the reliability of the module. Among WBG devices, electrical insulation weaknesses in WBG-based Insulated Gate Bipolar Transistor (IGBT) have been more investigated. The chapter deals with (a) current standards for evaluation of the insulation systems of power electronics modules, (b) simulation and modeling of the electric field stress inside modules, (c) diagnostic tests on modules, and (d) PD control methods in modules.

**Keywords:** wide bandgap devices, partial discharge, electric field stress

1. Introduction

The growing integration of distributed generation resources, envisagement of direct current (DC) microgrids and high-voltage direct current (HVDC) networks, the continued electrification and grid-level power flow controls call for advanced power electronics with improved

efficiency, reliability and power density [1]. Undergoing dynamic evolution in power electronics is mainly due to the development of power semiconductor devices seeking simultaneous operation at a higher voltage, power, and switching frequency. Having higher blocking voltage capability, higher temperature tolerance, and higher switching frequency than Si technology, wide-bandgap (WBG) semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) are expected to be a response to the mentioned challenge [2]. Si has a bandgap of 1.1 eV, whereas the bandgap of SiC and GaN is, respectively, 3.3 and 3.4 eV. The bandgap is the energy required to transfer an electron from the valence to the conduction band. Insulators, semiconductors, and conductors have large, small and very small bandgaps, respectively. While the highest commercial Si IGBT breakdown voltage capability is 6.5 kV, a record high blocking voltage of 15 kV was reported for the SiC IGBT produced in [3] and higher voltage capability up to 20–30 kV is expected shortly [4].

The metalized ceramic substrate shown in **Figure 1a** is well-known and established insulation technology for blocking voltages up to 3.3 kV, but it exhibits some weaknesses due to partial discharges (PDs) in silicone gel at higher voltages. In a sufficient electric stress condition localized gaseous breakdowns known as PDs can occur within an insulation system. Various measuring techniques and sensors have been developed for PD detection to perform an accurate condition monitoring and assessment of the insulation status of power equipment [5, 6]. We will discuss this topic in Section 4. The blocking voltage places across substrate solid insulating material, which is aluminum nitride (AlN) or alumina (Al_2O_3) ceramics where HV electrode is IGBT or diode and the ground electrode is copper or aluminum silicon carbide (AlSiC) base plate connected to the heat sink. However, both sides of the insulating ceramic are metalized by copper to evacuate better and transfer the heat generated by IGBTs or diodes to the base plate [7]. IGBTs, diodes and base plate are soldered onto the metalized ceramic substrate [7]. In this regard, solid dielectric substrates should also have appropriate thermal properties such as resistance to high temperatures and good thermal conductivity in addition to their desirable electrical insulation and mechanical properties. This is the case for AlN and Al_2O_3 with a thermal conductivity of typically, respectively, 180 and 27 W/mK [8]. Note that, however, the thermal resistance of the AlN substrates assembled with IGBTs is around a factor of only three less than Al_2O_3 substrates [8] (not 180/27 = 6.7 times for AlN and Al_2O_3 materials itself). Attaching the copper metallization to the ceramic substrate can be done by direct
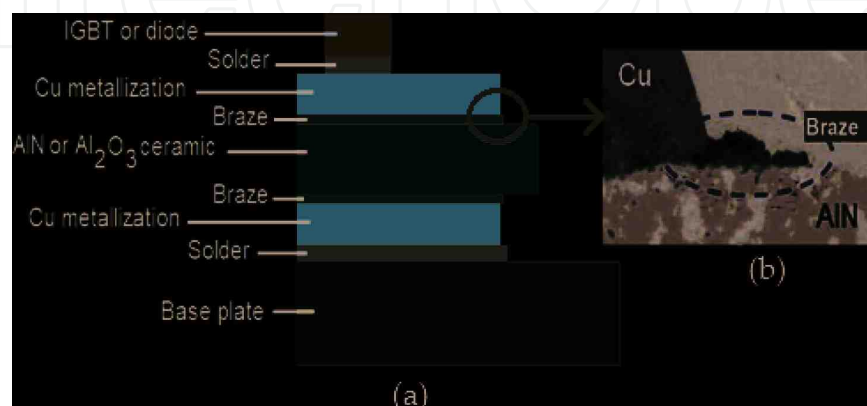
Figure 1. (a) A schematic of an IGBT substrate with active metal brazing (AMB) of the metallization and (b) protrusions with extremely sharp edges of some braze below the metallization.
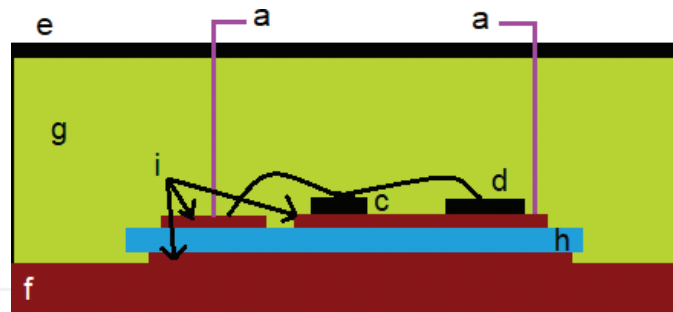
Figure 2. A schematic of an IGBT module with DBC, (a) connection to bus bars, (b) bond wire, (c) diode, (d) IGBT, (e) plastic case, (f) baseplate, (g) silicone gel, (h) AlN ceramic, and (i) copper metallization.

bonded copper (DBC) or active metal brazing (AMB). **Figure 1a** shows active metal brazing method [7]. No braze layers are needed for DBC as shown in **Figure 2**. Then a soft dielectric such as silicone gel is used to encapsulate the whole module to prevent electrical discharges in air as well as to protect semiconductors, substrates, and connections against humidity, dirt, and vibration. As a commercial example, "SYLGARD™ 527 Silicone Dielectric Gel" manufactured by the Dow Chemical Company has a dielectric constant of 2.85 and dielectric strength of 17 kV/mm [9].

Silicone gel also prevents thermal induced movements of bond wires attached to the semiconductor. The final encapsulation is achieved using polymer housing. The schematic layout of an IGBT with AMB is similar to that shown in **Figure 2** where brazes are also added to the structure.

As a consequence of higher blocking voltage, new packaging solutions to provide electrical insulation between the grounded heat sink and the HV terminals of the module are required. Due to the high electric fields, especially at the edges of the copper metallization, PDs can be initiated from these regions. The situation gets worse at protrusions shown in **Figure 1b** with extremely sharp edges of some braze below the metallization. High activity of PDs damages the insulating silicone gel and leads to electrical insulation failure and reduces the reliability of the module. Moreover, high-frequency PD pulses can lead to disturbance of the power electronics and cause severe shortcomings in high-power applications. The PD issue is one of the most crucial challenges to the development of HV high power density WBG power semiconductor devices. A description of current standards on PD tests on power electronics modules and relevant technical gaps is presented in Section 2. Section 3 deals with simulation and modeling of electric field stress inside power electronics modules. The various PD detection techniques employed for modules and correlation between measurements and electric field calculation is discussed in Section 4, and finally, PD control methods to relieve high field regions is explained in Section 5.

2. International standards on PD tests on power electronics devices

IEC 61287-1: "Railway applications-power converters installed on board rolling stock-part 1: characteristics and test methods" is the current standard commonly used for IGBT working at 1.5 kV or more [10]. The test voltage is a 50 Hz or 60 Hz alternating current (AC) root mean

square (RMS) voltage equal to $1.5\,U_m/\sqrt{2}$ or higher where U_m is the maximum blocking voltage of the module in (V). For a 6.5 kV IGBT, it is $1.5 \times 6.5/\sqrt{2} \approx 6.9$kV. The voltage is ramped up to $1.5\,U_m/\sqrt{2}$ in 10 s and is maintained for $t_1 = 1$ min as shown in **Figure 3**. The rate of the ramp as shown in **Figure 3** is $(1.5\,U_m/\sqrt{2})/10$kV/s. During this time t_1, some PDs may be observed. After t_1, the voltage is decreased to $1.1\,U_m/\sqrt{2}$ in 10 s. For a 6.5 kV IGBT, it is $1.1 \times 6.5/\sqrt{2} \approx 5.1$kV. The voltage $1.1\,U_m/\sqrt{2}$ is applied for $t_2 = 30$ s. During the last 5 s of t_2, the peak magnitude of partial discharge in pC is measured. A typical value to pass the test for a component and a subassembly is, respectively, 10 and 50 pC.

However, IGBT modules are subjected to pulse width modulator (PWM) stress-type instead of power frequency AC voltages. To elucidate this stress-type, consider a single-phase full-bridge inverter as shown in **Figure 4a**. An inverter changes a DC input voltage to a symmetrical ac output voltage of desired magnitude and frequency. When switches (which can be IGBTs) Q_1 and Q_2 are turned on at the same time, the input voltage U_s appears across the load. In this situation, the voltage on Q_3 and Q_4 which are off will be U_s. If switches Q_3 and Q_4 are turned on simultaneously, the voltage across the load is $-U_s$. In this situation, the voltage on Q_1 and Q_2 which are off will be $-U_s$. **Figure 4b** shows the waveform for the output voltage. Thus a unipolar square wave voltage with a magnitude of U_s for $(0 - T_0/2)$ and almost zero for $(T_0/2 - T_0)$ places on Q_3 and Q_4 and a unipolar square wave voltage with an amagnitude of nearly zero for $(0 - T_0/2)$ and $-U_s$ for $(T_0/2 - T_0)$ places on Q_1 and Q_2.

In many industrial applications, it is often required to control the output voltage of inverters (1) to cope with the variations of dc input voltage, (2) for voltage regulation of inverters, and (3) for the constant volts/frequency control requirement [11]. The most efficient method of controlling the gain is to incorporate pulse-width-modulation (PWM) control with the inverters. In this regard, the commonly used techniques are:

1. Single-pulse-width modulation

2. Multiple-pulse-width modulation

3. Sinusoidal-pulse-width modulation

4. Modified sinusoidal pulse-width modulation

5. Phase-displacement control

Here we describe only sinusoidal-pulse-width modulation (SPWM) technique which is widely used. For other methods see [11]. In SPWM, the width of each gating signal can be varied in proportion to the amplitude of a sine wave. As shown in **Figure 5**, the gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency, f_c, and peak, A_c. In this case, Q_3 and Q_4 should withstand u_{ab} which is a fast-rising and fall square waveform known as PWM-stress in $(0 - \pi)$ and Q_1 and Q_2 should withstand u_{ab} in $(\pi - 2\pi)$.

It has been known that repetitive voltage impulses generated as PWM-stress can lead to insulation premature failure of stator winding due to partial discharges in inverter-fed motors [12, 13]. About IGBTs the studies in [14, 15] show that PD behavior under 50 Hz or 60 Hz AC sinusoidal voltage is different from that for fast rise bipolar high-frequency square wave voltages. In this regard, for example for the test sample in [14] while partial discharge inception voltage (PDIV) under 50 Hz sinusoidal test voltage is 13 kV, for a bipolar square voltage with
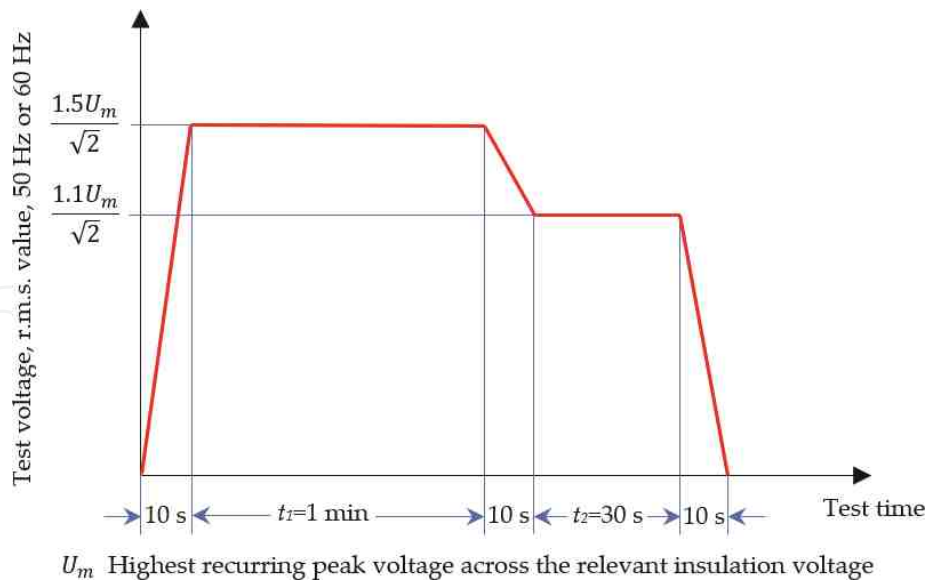
Figure 3. IEC 61287-1: "Railway applications-power converters installed on board rolling stock-part 1: characteristics and test methods" for partial discharge test.

rising time of about 400 μs, fast rise positive unipolar square and fast rise negative unipolar square both with rise time of about 100 ns it is 12, 9 and 7 kV, respectively. Moreover, the rate of increase in the PD magnitude concerning voltage is higher for steeper voltage rise [14].

Therefore new standards are needed to take into account actual voltages for power electronic modules. It was shown in [16] that although IGBTs could pass 50 Hz sinusoidal test under IEC 61287-1, insulation failure occurs when applying PWM input voltage with 50 Hz modulating frequency with 1 kHz carrier frequency and a rise time of 10 μs that is the stress condition more similar to the real operating conditions.

According to IEC 61287-1, the collector, emitter, and gate of a power electronics module should be connected, and PDs are measured when an alternating voltage is applied between the interconnected terminal and the metal base plate. The drawback is that it tests only the insulation
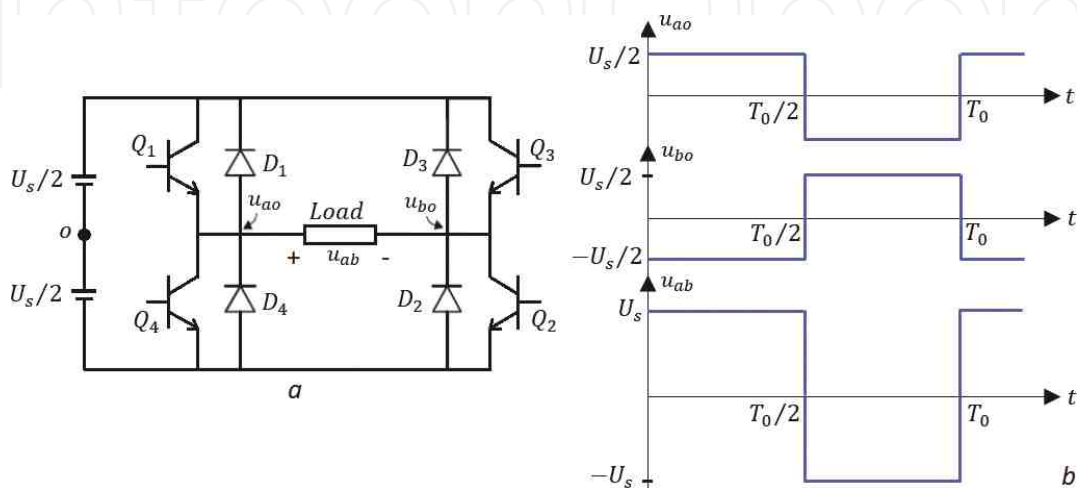
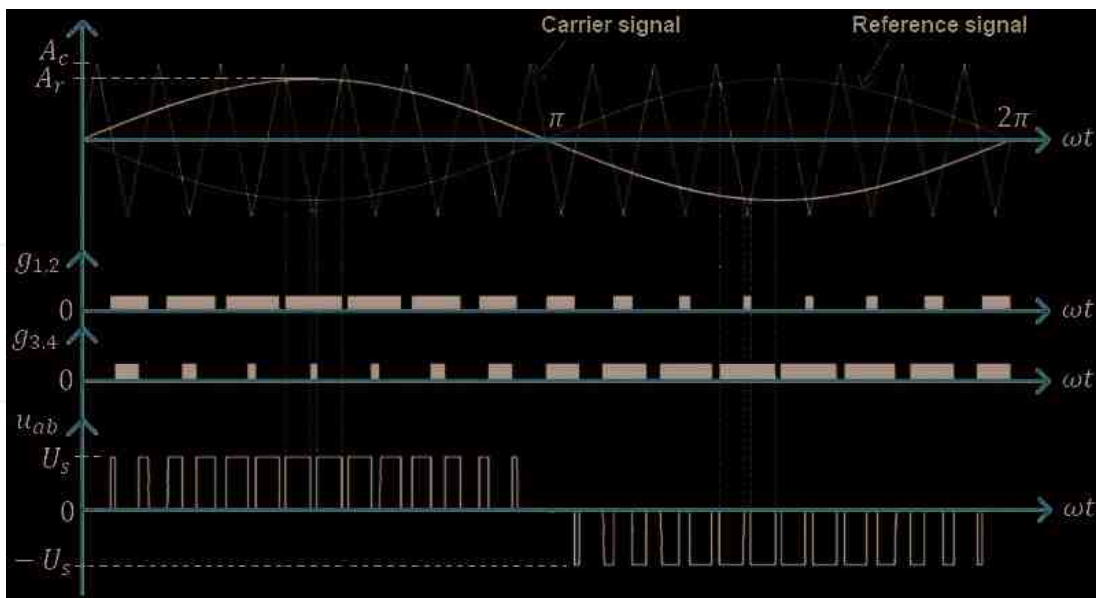**Figure 4.** Single-phase full-bridge inverter.

Figure 5. Sinusoidal pulse-width modulation.

of the substrate and the bulk of the gel is not tested. To address this issue, the test voltage is proposed as an AC voltage superimposed on a direct current (DC) one directly applied to the component turned off using a negative gate polarization [17–19]. The inverse DC offset of magnitude higher than the AC peak value as shown for an example in **Figure 6a** used as the test voltage avoids diode conduction [18]. The discharge inception voltage (U_{DIV}) is then defined as the peak value of the applied voltage ($U_{DC} + U_{AC}$) [17]. **Figure 6b** shows an experimental set-up generating such test voltage [17].

This method leads to detect PD for voltages lower than the one necessary to trig them during IEC 61287-1 test [17–19]. Although neither the test proposed in [17–19] nor IEC 61287-1 test can represent thoroughly the stresses endured by the power modules in inverters, the testing method proposed in [17–19] can provide more useful information on PDs during normal operation by stressing all the components involved in the packaging.
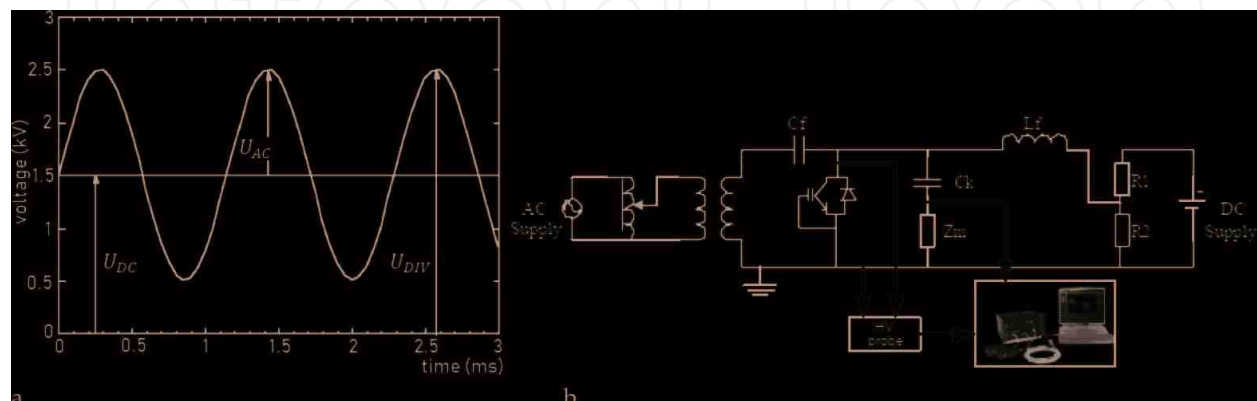

Figure 6. (a) New test voltage waveform and (b) set-up generating new test voltage for PD detection of an IGBT [18], License No. 4383271241884.

3. Simulation and modeling of electric stress inside the module

Since a combination of material defects in gel and the high electric stress due to sharp edges leads to partial discharge, PDs do not occur all along the sharp edges. However, identifying the critical spots with the maximum electric field magnitude due to only sharp edges can be useful to develop geometrical strategies to reduce the electric field magnitude peaks due to the effect of one contributing factor.

Note that the maximum electric field magnitude at perfectly sharp edges is theoretically infinite. Thus, the smaller mesh size, the higher electric stress and mathematically there is no convergence point. Assuming a rounded edge converges to a finite maximum electric field intensity with increasing resolution of the mesh grid. However, the value depends on the assumed edge radius. The smaller assumed edge radius, the higher amount of maximum electric field magnitude. To overcome this difficulty, it was shown in [20, 21] that when the distance to sharp edges becomes larger than 20 μm for the assumed geometry and dimensions, the differences between the electric field magnitudes for different meshing sizes are less than 1%. To be on the safe side, measuring points were considered at a distance of 50 μm to sharp edges in [20, 21]. In [22], both strategies containing rounded edges and considering measuring points at a distance of 20 μm from edges were benefited.

Assuming the measuring points defined above, the influence of following geometrical options are studied in [20, 22] on reducing the electric field stress values.

1. The thickness of the metallization layer,

2. The thickness of the substrate,

3. The shape of the edge,

4. Metal/conductive layer offset.

Among four parameters above, the thickness of the substrate and metal/conductive layer offset have a strong influence on the electric field magnitude. By varying the thickness of the ceramic, the electric field stress does not follow the equation of a plate capacitor: a doubling of the thickness (1–2 mm) reduces the electric field stress only by about 30% and not by 50%. However, an increased substrate thickness decreases cooling efficiency of the semiconductors, and this technique may not meet the miniaturization needs of power electronics as well.

Defining an offset of the two metallization layers as $r_{off} = r_u - r_l$ for r_u (the distance from the AlN ceramic edge to the edge of the upper Cu metallization) and r_l (the distance from the AlN ceramic edge to the edge of the lower Cu metallization) shown in **Figure 7a**. **Figure 8** shows the electric field stress values at measuring point located on L1 for different values of r_{off} for a d = 630 μm ceramic layer [22]. For that (**Figure 7a**), a finite-element method (FEM) model was developed in the *Electrostatics* (*es*) module of COMSOL Multiphysics solving Poisson's equation.

$$\nabla^2 U = -\frac{\rho_v}{\epsilon_0 \epsilon_r} \tag{1}$$

$$E = -\nabla U \tag{2}$$

where ρ_v is volume charge density which is $\rho_v = 0$ in the model considered in [22], ϵ_r is relative permittivity which for AlN and gel were considered, respectively, 8.9 and 2.7 in [22], E is electric field intensity, and u is electric potential.

As shown in **Figure 7b**, an extremely custom fine meshing with a maximum element size of 0.001 mm was used for Area 1 shown in **Figure 7a** to obtain precise results for electric field
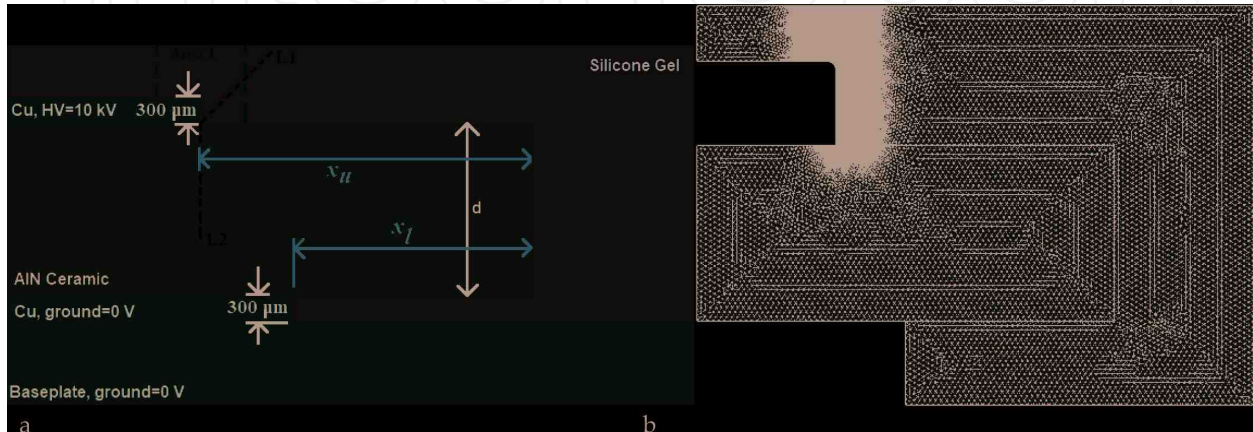
Figure 7. (a) The geometries considered for simulations in COMSOL Multiphysics and (b) meshing strategy.

intensity along L1 [22]. Such meshing strategy, using several levels of extremely custom fine meshing for the study area having sharp edges and a normal meshing for other areas to increase the computational efficiency was used in [23–29] as well. From **Figure 8**, it can be seen that with decreasing offset the electric field magnitude reduces. In other words, an increase in the length of the upper metal layer relieves the worst high field region. It is due to the influence of the grounded based plate, since the more extended top metal layer, the less nonuniform electric field. Changing r_{off} from 0.35 to −0.5 mm reduces the electric field intensity up to 57% that presents the method as an efficient electric field control technique [22].
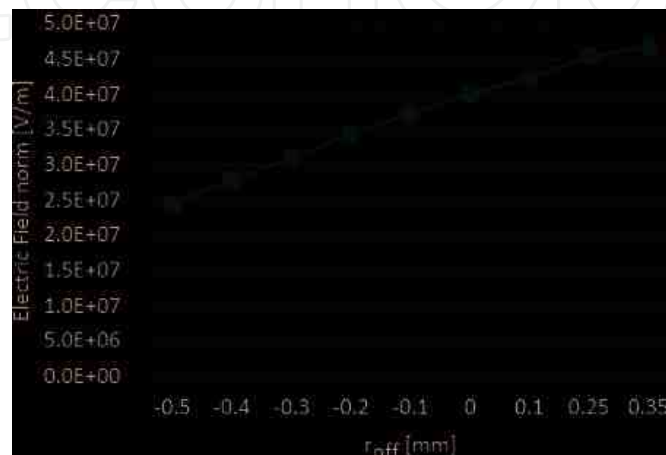
Figure 8. Influence of r off on electric field intensity.

4. Partial discharge measurements

Research carried out on PD detection, and localization inside an IGBT can mainly be divided into electrical and optical PD measurements. For electrical PD measurement, measured phase-resolved partial discharge (PRPD) patterns were analyzed to identify the type and location of PD. As shown in **Figure 9** [30, 31], it was observed that the PD of a metalized ceramic in an isolating liquid occurs at the maximum voltage at 90° and 270° and the amount of PD does not rise sharply with increasing voltage.

However, as shown in **Figure 10** [21, 30, 31] for the same metalized ceramic embedded in silicone gel, PD was found at a phase between zero and the maximum voltage, between 0–90° and 180–270°. Since the number and magnitude of the PDs strongly increase with rising voltage, it was argued that the origin of this discharge phenomenon is due to discharges at the interface between the silicone gel and the substrate and not due to locally restricted cavities in the gel.

In [21] the calculated electric field intensity and the measured PDIV were correlated. Combining the calculated electric field intensity in four measuring points ML1-ML4 shown in **Figure 11a**, the PDIV was plotted as shown in **Figure 11b** as a function of the geometric mean of E values at ML1-ML4. A fitted equation as "PDIV (kV) = 20.4–0.25E (kV/mm)" was also reported for **Figure 11b** [21].

However, through an artificial spherical void embedded in silicone gel, it was shown in [32] that voids inside the silicone gel significantly accelerate the aging of the materials even at a normal operating electric stress. It was also found that an extremely non-uniform electric field resulted by a needle-sphere electrode with no artificial void inside the material can also lead to rapid aging at a normal operating electric stress [32]. Thus, it was concluded that the electrical treeing in front of the needle tip produces gas-filled voids inside the silicone and these week points besides conductive channels of trees lead to shortening the lifetime of the insulation [32].

In [33, 34] an optical PD localization setup benefitting from compact charge-coupled device (CCD) camera modules was used to record the small light intensities emitted by electroluminescence effects as well as the light caused by PD. It should be noted that before partial discharge inception, insulating polymers subjected to high electrical fields usually display electroluminescence as a result of the radiative relaxation of excited molecular states within the gel excited by high electrical field [34]. The measurement of electroluminescence allows the critical regions of high electric fields to be identified in the translucent silicone gel insulation
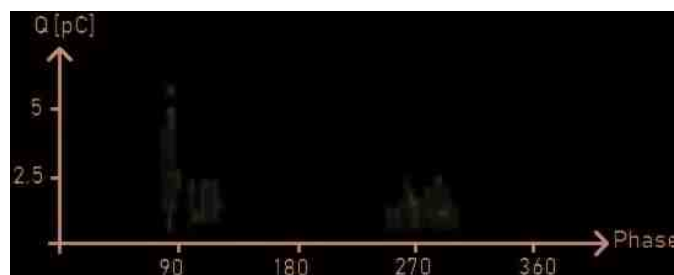
Figure 9. PD spectroscopy of AlN substrates in an insulating liquid [31], License No. 4383271013906.
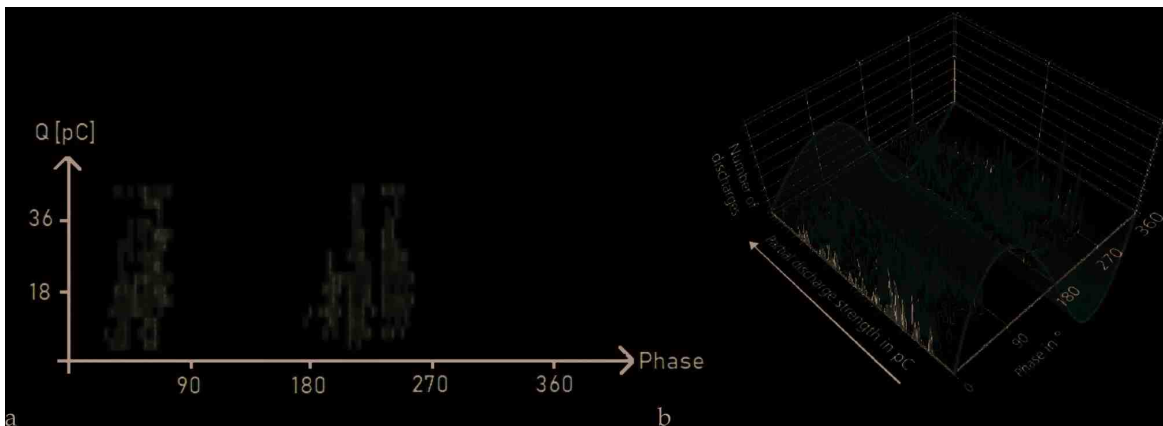
Figure 10. PD spectroscopy of AlN substrates in silicone gel (a) from [31], License No. 4383271013906, (b) from [21], License No. 4383270757365.

even before electrical aging begins. Increasing the voltage, PD starts at distinct locations. Bright shining spots in the image as seen in **Figure 12** show the higher possibility for PD inception.

In [35] the results concerning both electrical and optical detection of PDs occurring in the silicone gel were presented. That work showed that optical measurements could be used to study PDs in transparent gels, with any voltage shape and with very high sensitivity (<1 pC). In recent years, micro silicon photomultipliers (SiPM) were also examined and compared to conventional photomultiplier tubes (PMT) for optical PD detection [36].

In [37, 38], besides PRPD measurements, other diagnostic and quality control test methods to discriminate the dielectric condition between new and aged IGBT samples and reveal the influence of moisture on dielectric state of IGBT modules were used. They are time-dependent dielectric response measurements such as insulation resistance and polarization index, and frequency-dependent dielectric response measurements such as loss factor and frequency response analysis (FRA). Humidity as a result of the condensation caused by the difference in the interior and exterior temperatures may impact on the dielectric integrity of IGBT modules.
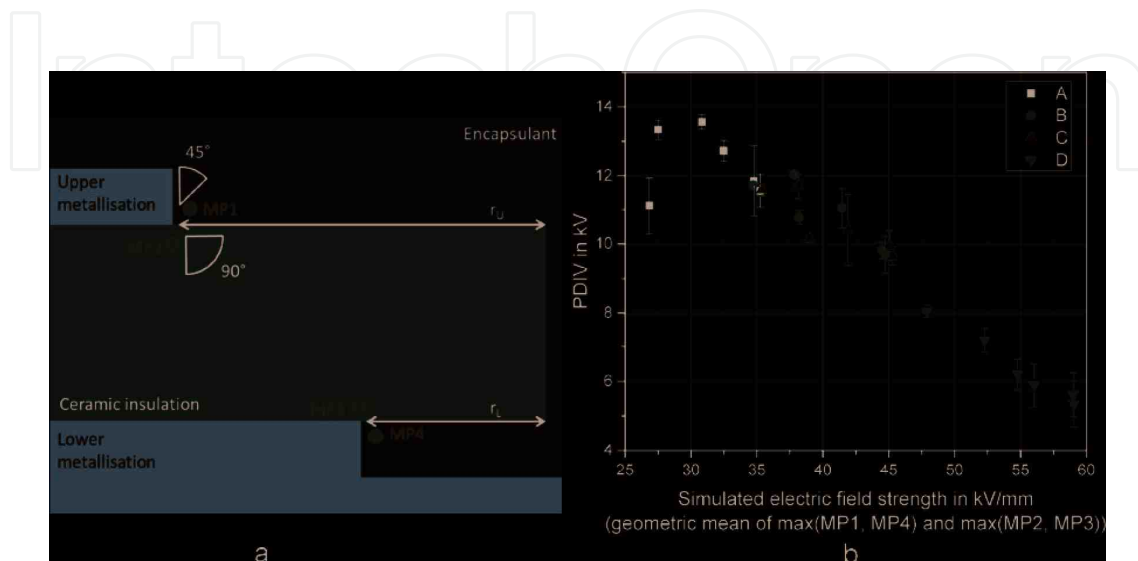
Figure 11. PDIV as a function of the geometric mean of MP1-4 [21], License No. 4383270757365.
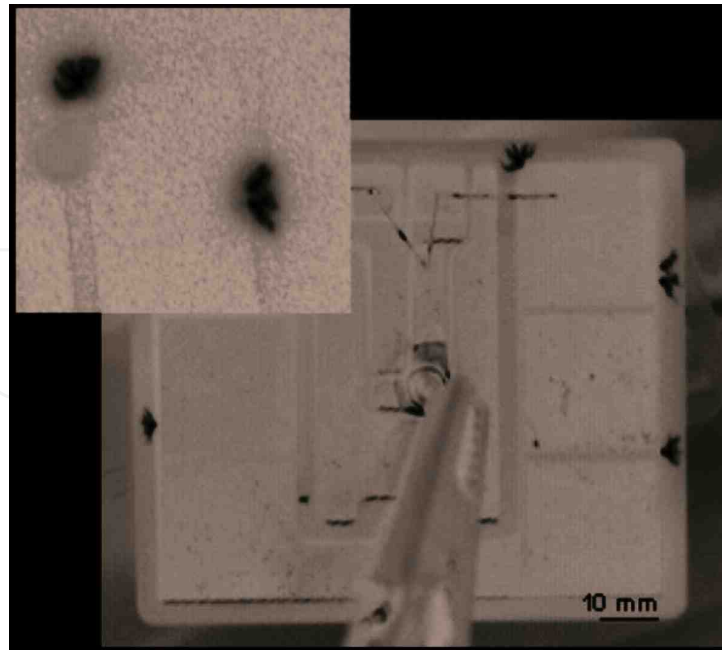
Figure 12. Optical localization of PD for an AIN substrate embedded in silicone gel. The discharges are located at the outer edges of the copper metallization [34], License No. 4383270494717.

Converters are often located in cubicles under atmospheric pressure, and the most widely used material for encapsulation of power electronic circuits is silicone gel [8, 15–22, 30–38, 42–45, 48, 51–54]. However, for variable-frequency drive (VFD) fed motors used in the subsea factory for oil and gas production at depths more than 3000 m, the development of pressure tolerant power electronics is envisaged where an incompressible insulating material is needed for power electronic modules. Thus, liquid embedded power electronics are investigated. In [14, 39] PDs in liquid embedded power electronics under three different waveforms as sinusoidal (50 Hz) voltage, a slow rise bipolar square voltage with a rise time of 400 μs, and a fast unipolar positive and negative rise square voltage with a rise time of 100 ns were investigated. Both electrical and optical techniques were used to study PD behavior of IGBT insulation. Regarding a good correlation found in [14, 39] between the measured electrical and optical PDs, optical PDs can also be considered for the characterization of PD phenomena. Another significant result obtained in [14, 39] is that the fast rise square voltage has the lowest PDIV while the sinusoidal voltage has the highest one. Moreover, it was reported in [14, 39] that the number and magnitude of PDs decrease when the pressure of the liquid in the test cell increases. In other words, pressure can collapse the propagation of the streamers, and that is the great merit of liquid embedded power electronics used for the subsea application.

Various liquid dielectrics such as Nytro 10XN, Midel 7131 and Galden HT230 were examined in [40, 41] for pressure tolerant liquid embedded power electronics modules for deep, and ultra-deepwater. The test object used in [40] is a printed circuit board (PCB) card shown in **Figure 13a** with a dimension of $50 \times 24 \times 1$ mm^3 and a schematic shown in **Figure 13b**. The thickness of copper metallization at both sides is 420 μm. The trench located at the upper metallization layer has a width of 2 mm. The left end of the board was connected to a high voltage source and the other end of the board and the base plate (the lower metallization layer) was connected to ground. Sharp edges were rounded to ensure the set-up is PD free.
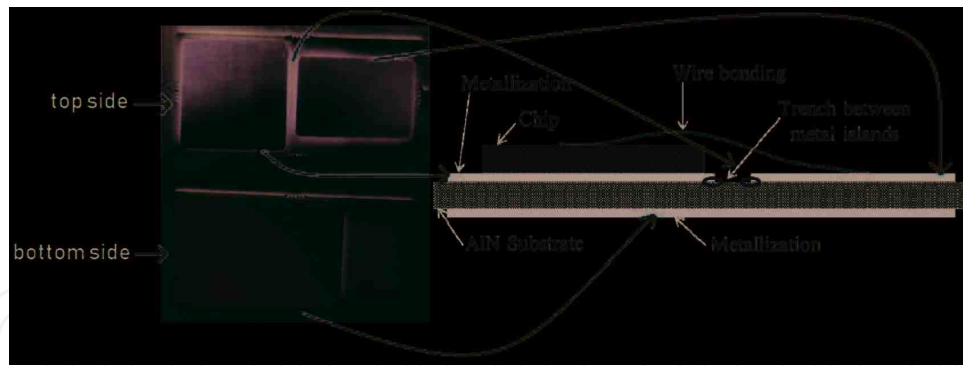
Figure 13. (a) PCB card test object and (b) the schematic of PCB card [40], License No. 4383270012789.

Table 1 shows the $U_{1\%}$, $U_{50\%}$, and $U_{63\%}$ breakdown probability. For $U_{63\%}$, the cumulative Weibull function was considered given by

$$f(v) = 1 - e^{[-v/\alpha]^{\beta}} \tag{3}$$

where v is voltage, $f(v)$ is the probability of failure, α is the characteristic breakdown voltage and β is the range of failure voltages within the distribution. The higher the β, the lower the scatter is. Besides sinusoidal voltage (38.5 Hz), tests were carried out under a fast-rising positive square wave voltage. From **Table 1** it can be seen that Galden has a superior breakdown characteristic.

The influence of temperature on PD characteristics in silicone gel was experimentally investigated in [42]. It was found that with increasing the temperature, the PDIV and the overall shape of PD patterns remain unchanged, but both discharge amplitudes and number increase as shown in **Figure 14** for PRPD patterns in the same sample at a fixed applied voltage at 20 and 100°C [42].

Figure 15 shows the influence of temperature on the variation of the average PD current (I_{av}), which is the sum of all recorded discharges per unit time, versus voltage in the same experiments [42]. It can be seen that with increasing the temperature, the PDIV remains unchanged. However, due to the increase of PD amplitudes and number the increase of I_{av} is faster at high temperature [42].

Voltage type	Samples	$U_{1\%}$ (kV)	$U_{50\%}$ (kV)	α (kV)	β
Sinusoidal voltage	Nytro	20.01	40.89	43.89	5.92
	Midel	25.94	39.76	41.26	9.92
	Galden	27.56	41.98	43.54	10.06
Positive square voltage	Nytro	19.19	22.5	22.86	26.29
	Midel	15.28	22.98	23.75	10.43
	Galden	20.80	32.17	33.41	9.7

Table 1. $U_{1\%}$, $U_{50\%}$, and $U_{63\%}$ breakdown probability for PCB card test object [40].
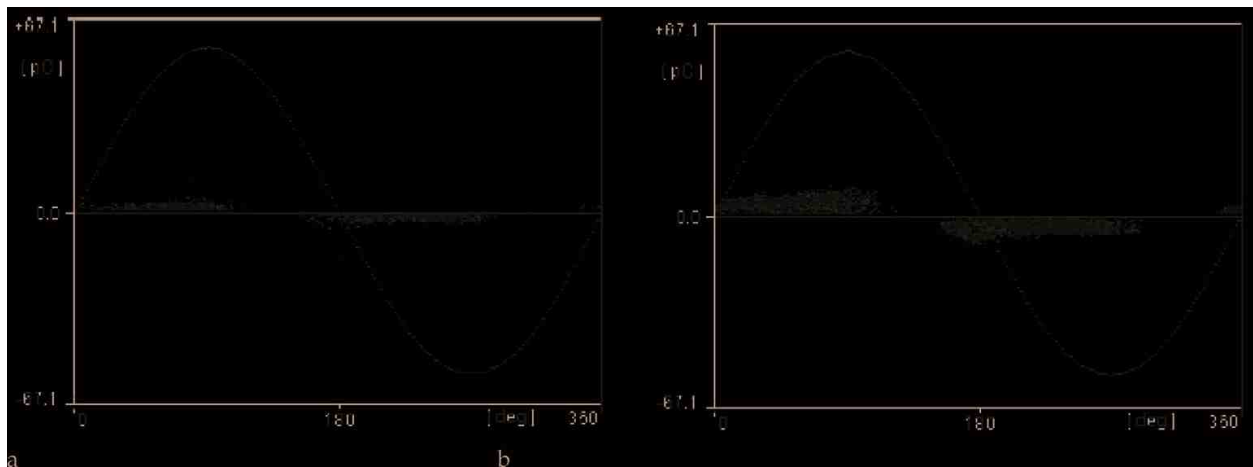
Figure 14. PRPD patterns at two temperatures (a: 20°C, b: 100°C) with a point-plane sample embedded in silicone gel (ac 50 Hz, the tip radius of curvature for the point of r_0 = 1.4 µm, gap distance of d = 4 mm, V = 8 kV) [42], License No. 4383261112180.
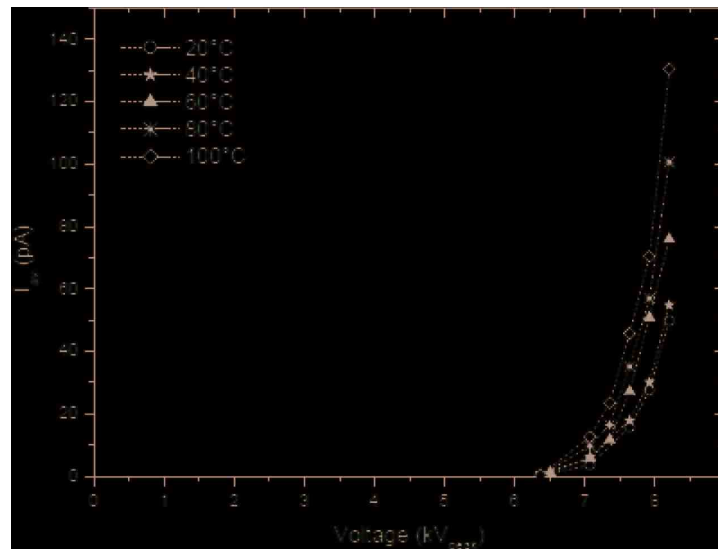
Figure 15. Influence of temperature on average PD current versus voltage (ac 50 Hz, r_0 = 1.4 µm, d = 4 mm) [42], License No. 4383261112180.

5. Partial discharge control

5.1. Linear resistive electric field control

Applying functional materials on the highly stressed region can reduce the electric field. Two types of stress relieving composite dielectrics are as follows. (1) The conductivity of the material varies with the electric field, field-dependent conductivity (FDC) [43, 48], (2) the permittivity of the material changes with the electric field, field dependent permittivity (FDP) [50].

In FDC stress relieving control, also called resistive field control, a conductive layer is applied at the metallization edge. The field distribution is modified by flowing the conduction current

through the layer. Materials used for resistive field control can be linear or nonlinear. The conductivity of linear resistive field control materials is not field dependent. Therefore, the conductivity of the layer made of linear materials must be carefully selected. For too low conductivity, the layer has no role in electric stress control [48]. On the other hand, if the conductivity of the layer is too high and for the case of a non-bridging layer, the layer behaves as a prolongation of the metallization and the high field problem is merely transferred to the end of the layer [48]. For the case of a layer bridging HV and ground potential, the layer leads to massive leakage current [48].

In [43], a 300-nm high impedance layer having an electrical conductivity of 105 Ω cm made of semiconducting amorphous silicon, a-Si: H, was applied by plasma-enhanced chemical vapor deposition (PECVD) process to the edge of the substrate connecting the top copper metallization with the bottom. The mentioned conductivity was adjusted to homogenize the electric field by having the magnitude of the conduction current higher than the capacitive current. By electric field simulations, the same value of the electric conductivity of the layer was reported in [44, 45]. Two sample modules with and without a-Si:H coating built under manufacturing conditions were tested in [43]. While the partial discharge increases sharply at low voltages of 3–4 kV without an a-Si:H coating, it does not exceed 10 pC up to a voltage of 10 kV with an a-Si:H coating layer satisfying the partial discharge requirements based on IEC 61287-1. Note that the linear resistive field control depends on the frequency and its advantage reduces with increasing frequency.

The intrinsic semi-conductive nature of the particles and their connectivity lead to non-linear behavior of nonlinear resistive electric field control composites. In this regard, the particle to particle contact is possible if the filler concentration is above a prescribed limit. The electrical field magnitude must also be high enough to allow conduction through the semi-conductive particles and barriers between particles.

A theory-based evaluation of the behavior of field grading materials with strongly field-dependent conductivities is presented in [46] with a survey of ZnO microvaristors in various applications in [47]. ZnO microvaristor layer was studied to relieve high field regions in an IGBT [48]. An advantage of nonlinear materials compared to linear materials is that losses are not permanent. They occur only when the electrical field magnitude passes a threshold known as switching filed where the material switches to a conductive behavior.

An electrostatic FEM model developed in ACE TripleC was used for electric field calculations in [48]. **Figure 16a** shows electric field distribution for without a coating layer on the protrusion considered in the model. In this case, the maximum electric stress, E_{max}, obtained 2.6×108 V/m at the gel adjacent to the protrusion [48]. To relieve this high field stress region, a layer for coating the metallization edges was considered in three cases with polyimide layer ($\varepsilon_r = 3.5$), a high permittivity ($\varepsilon_r = 40$) layer of a polymer/ceramic composite and ZnO microvaristor layer described above. A comprehensive study of the general structure of polymers, their properties and applications can be found in [49]. For polyimide layer, E_{max} in the layer (adjacent to the protrusion) and gel will be 2.3×108 and 0.18×108 V/m, respectively [48]. In this regard, although polymer/ceramic composite with $\varepsilon_r = 40$ can reduce the maximum electric field in the layer adjacent to the protrusion to 0.3×108 V/m, the electric field in the gel reaches higher values (0.2×108 V/m) than with polyimide coating. Employing a ZnO microvaristor layer, E_{max} in both the layer (0.066×108 V/m as shown in **Figure 16b**) and gel (0.06×108 V/m) dramatically decreases.

Figure 16. The influence of nonlinear FDC coating layer on reducing the electric field in the module [48], License No. 4383260855923.

5.2. FDP stress relieving control

As mentioned in Section 5.1 although a high permittivity coating layer relieves high electric field stress adjacent to the copper metallization, it leads to higher electric field stress in the gel and in particular the weak interface between the layer and the gel encapsulation. This means a high permittivity material as a coating layer may not be efficient. Thus in [50] employing it as a filler was examined. The filler studied in [50] was a ferroelectric filler, barium titanate, in the base silicone gel to form an FDP stress relieving dielectric material having a $\epsilon_r(E)$ as $\epsilon_r(E) = 6.4 + 1.3E$. By enhancing polarization mechanisms, the ferroelectric filler particles can reduce high electrical stresses. However, it should be noted that this electric field control method works only under ac fields and at the temperatures higher than Curie temperature which is 130°C for pure barium titanate [51] this advantage will disappear [50].

It is shown in [50] that applying a high permittivity non-dependent field filler can reduce electric stress by around 10% while with a dependent-field one a reduction of 29% can be achieved.

5.3. The quality and type of substrates

Despite all publications, which have concluded that PDs occur in the silicone gel or at the interface between the substrate and the gel, a different conclusion about the origin of PDs was reported in [52]. To explore the actual origin of PDs, six insulating liquids including Silicon oil #1 (Sil20), Silicon oil #1 (Sil350), Transformer oil (Toil), Synthetic capacitor liquid (Scl), Synthetic transformer liquid (Stl) and Ester liquid (Est), which have different PD properties were used instead of gel, and three substrate materials including AlN, Al_2O_3, and glass/epoxy composite were also examined.

A rather large variation in PDIV was observed for six mentioned liquids used in a point-plane electrode geometry under 50 Hz AC voltage at room temperature (20°C). However, a substrate test geometry similar to an IGBT shows almost no changes in PDIV for the mentioned different liquids. Moreover, for the IGBT test geometry, PDs appear in both polarities and provides somewhat symmetrical patterns with good stability. However, asymmetrical PRPD

patterns for the point-plane electrode geometry were obtained. Using the gel in the mentioned experiments produces no change. Thus, it was concluded that PDs recorded with the substrate indeed do not occur within the liquid or the gel. The only remaining possibility is that PDs originate from the porous nature of the AlN or Al_2O_3 substrates. This is a hypothesis opposed to the ideas commonly accepted. The experiments carried out with another sintered porous material, and with a non-porous material (epoxy resin) confirm this hypothesis where with epoxy, no stable PD regime can be achieved.

In the almost same direction, it was experimentally shown in [53, 54] that surface discharges initiated at the triple junction and propagated at the gel-AlN substrate interface creates cavities composed of tree-like structure and spherical sub-cavities leading to the degradation of AlN substrate [53] as well as give rise to the growth of cavities in the gel [54]. Regarding the first issue, other substrates such as Al_2O_3 and glass were compared with AlN. The cavities usually start from the triple junction with high voltage and being pushed away from the high voltage conductor through a conductive channel on the power module substrate. Focusing on the conductive channel, it was found that during repetitive surface discharges, desorption of nitrogen from AlN substrate results in the formation of Al and this leads to a decrease in the resistance of cavity path that was measured around 5 kΩ/100 μm for AlN compared to above 1 MΩ/100 μm for glass and Al_2O_3. Thus, it was justified that the high electric field at the tip of surface conductive paths is the reason for elongation the cavity stopping length for AlN to more than twice than that on other substrates. To address the second issue, the dynamic potential distribution of surface discharges in gel was measured by a two-dimensional sensing technique with a Pockels crystal [54].

Another survey of the topics discussed in this book chapter can be found in [55] where other papers, as well as other aspects of the documents reviewed in this book chapter, are evaluated. These two publications, [55] and this book chapter, cover together almost all electrical insulation issues in power electronics modules.

6. Conclusion

The book chapter reviews some technical issues raised for electrical insulation weaknesses in high power IGBTs. FEM modeling of electric stress inside modules, which have perfectly sharp edges, is a challenge where using rounded edges or assuming measuring points at a distance from edges are used to address this issue. Although PRPD patterns can be used to identify the origin and location of PDs, the hypotheses proposed based on the measured patterns have not reached an agreement. Further investigation is also needed to determine permissible levels for time and frequency dependent diagnostic methods for modules. The optical technique is a promising technique to localize PDs in a power electronics module. Using linear and non-linear resistive electric field control as a coating layer or using field dependent permittivity materials as a filler in the silicone gel can be used to control PD in modules. However, these mitigation solutions are not mature and need further research.

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