69-1996

TODD, David Arlen, 1937-

AN INVESTIGATION OF CHARGE TRANSPORT MECHANISMS IN EVAPORATED OXIDE FILMS ON ETCHED SILICON SURFACES.

The University of Oklahoma, Ph.D., 1968
Engineering electrical

University Microfilms, Inc., Ann Arbor, Michigan

THE UNIVERSITY OF OKLAHOMA

GRADUATE COLLEGE

AN INVESTIGATION OF CHARGE TRANSPORT MECHANISMS IN EVAPORATED OXIDE FILMS ON ETCHED SILICON SURFACES

A DISSERTATION

SUBMITTED TO THE GRADUATE FACULTY

in partial fulfillment of the requirements for the

degree of

DOCTOR OF PHILOSOPHY

BY

DAVID ARLEN TODD

Norman, Oklahoma

1968

AN INVESTIGATION OF CHARGE TRANSPORT MECHANISMS IN EVAPORATED OXIDE FILMS ON ETCHED SILICON SURFACES

APPROVED BY

DISSERTATION COMMITTEE

ACKNOWLEDGMENT

The author wishes to express his appreciation to Dr. Leon Zelby for his advice, assistance, and helpful direction throughout this investigation. Also, thanks are due Dr. William Kuriger and other members of the faculty of the School of Electrical Engineering, University of Oklahoma, for many helpful discussions and assistance.

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CHAPTER I

INTRODUCTION

In recent years the study of the surface properties of semiconductors has been spurred by the need for more detailed knowledge of the surface effects on semiconductor device operation. This is particularly true where the semiconductor surface exhibits its influence through thin oxide layers, as in oxide-protected integrated circuit structures and in metal-oxide-semiconductor (MOS) devices such as the MOS field effect transistor.

The electrical current which flows through an oxide layer to the surface of a semiconductor, and subsequently, into the bulk of the semiconductor, is controlled by the properties of the oxide layer, the surface properties of the semiconductor, and the bulk properties of the semiconductor. A number of authors (1, 2, 3, 4) have investigated current flow through oxide films normally used to protect semiconductor surfaces. They studied effects of the properties of the oxide using a metal-oxide-metal structure and both thermally grown and vacuum-evaporated oxide films ranging in thickness from a few angstroms to several microns. Also, many studies of the influence of oxide films thermally grown on various semiconductor surfaces have been made (5, 6). The surface of the semiconductor and its effect on current transport through what are called surface states has been extensively reported (7, 8, 9). The surface studies have been concerned with ways of characterizing the surface properties of a semiconductor and the effects of various surface treatments, ambient atmosphere conditions, defects

and impurities on the surface, etc., on the electrical nature of the semiconductor surface. Surface states on semiconductor surfaces have been categorized into two forms: "fast" states due to the abrupt termination of the crystalline lattice at the surface, and "slow" states due to impurities, defects, or oxide layers found on surfaces prepared by chemical etching and subsequent drying in room atmosphere conditions.

Gray (10) has used a metal-oxide-semiconductor structure in which a thin oxide (silicon dioxide) layer was formed by slow thermal oxidation of a cleaved silicon surface. Measurements of volt-ampere characteristics and ac capacitance and conductance were found to yield data concerning the density and energy levels of fast states on silicon surfaces. However, this study was not concerned with slow states, which, on etched surfaces may be of greater importance.

The present investigation was undertaken in an attempt to determine the primary mechanisms of charge transport through a MOS structure composed of an evaporated metal electrode, a thin evaporated layer of silicon monoxide, and a silicon sample whose surface was prepared by what might be considered "normal" processing, i.e., mechanical lapping and polishing followed by acid etching and drying in room atmosphere conditions. The oxide film was vacuum evaporated onto the surface of the silicon in order to cause the least disturbance of the silicon surface slow states. Semiconductor surfaces prepared as described above are generally referred to as "real" or technical surfaces as opposed to those cleaved in vacuum, which are described as "clean" surfaces.

It has been found that, both for thermally grown and vacuum evaporated oxides on silicon, an n-type surface layer is formed at the oxide-silicon interface layer. When p-type silicon is used as the bulk material, the effect of an oxide layer is to form a depletion layer (part of the acceptor atoms are compensated by induced negative charges in the surface) which extends into the silicon bulk. In some cases the p-type bulk is inverted at the surface to n-type material forming what is called an inversion layer. P-type silicon was chosen for the semiconductor material in order that the depletion

layer could be studied to give information concerning the surface states.

The possible mechanisms of charge transport through such MOS structures have been investigated (3, 7, 9, 10) and a summary of the basic mechanisms is given here. These mechanisms include tunneling from metal to semiconductor through thin oxide films, emission of electrons over the energy barrier represented by the oxide (Schottky emission) and variously described current flow mechanisms all depending on charge transport via electron traps in the oxide or on the semiconductor surface. The salient features of these mechanisms are discussed in Chapter II with emphasis on current flow via trapping processes. Chapter III describes the sample preparation and the experimental procedures for obtaining the volt-ampere characteristics and other important data. The results of the experimental program are presented in Chapter IV with the interpretation and discussion of the results presented in Chapter V.

The experimental evidence indicates that charge transport through evaporated silicon monoxide films on technical silicon surfaces is primarily controlled by electron trapping in the oxide layer and at the silicon surface. Even for extremely thin oxide layers (< 100 Å) where tunneling current would be expected, the current mechanism is still trap dominated. Differential capacitance measurements as functions of bias voltage and time also indicate that long time constants associated with the discharging of electron trap sites play a primary role in current flow through the MOS structure.

CHAPTER II

THEORETICAL DEVELOPMENT

Charge transport through thin insulating films between two metals or between a metal and a semiconductor is generally considered to be due to one or more of the following:

1. Schottky emission or Richardson emission -- field or thermal emission of electrons over a potential barrier
2. Tunneling of electrons through a thin potential barrier
3. Field and/or thermal ionization of electron trap levels caused by impurities or defects
4. Breakdown phenomena including Zener breakdown and avalanche multiplication.

EMISSION over a POTENTIAL BARRIER

An insulating film situated between two conductors or semiconductors represents a potential barrier which electrons must surmount or penetrate in some fashion in order to establish a current flow through the structure. Schottky emission describes the process whereby electrons are emitted from a metal electrode into the conduction band of an insulating film over the image force interfacial barrier under the attendant lowering of the electric field. The Schottky emission equation modified from the original development for emission into vacuum to emission into an insulating film is (3)

$$I = A\lambda T^2 \exp\left(\delta V^{\frac{1}{2}} - \varphi/kT\right) \qquad (1)$$

where I = electron current

A = cross-sectional area

λ = Richardson constant

T = temperature

V = voltage applied across film

φ = interfacial barrier height

k = Boltzmann's constant

and $\delta = (q/\epsilon\epsilon_o a)^{\frac{1}{2}} (q/kT)$ (2)

where q = electron charge

$(\epsilon\epsilon_o)$ = dielectric constant of insulator

a = insulator thickness

In the elementary theory, λ, the Richardson constant equals 120 A cm^{-2} $^oK^{-2}$ but divergences from this value by a factor of 10 have been observed. Experimentally, the slope of the plot of the natural logarithm of I versus the square root of the applied voltage yields values for δ which can be compared to calculations based on dielectric constant and thickness measurements. The zero voltage current intercept

$$I_o = A\lambda T^2 \exp(-\varphi/kT) \quad (3)$$

yields values for the interfacial barrier height. For example, using an assumed value of 120 for λ and their measured data for aluminum-evaporated silicon monoxide sandwiches, Hartman, et. al., (3) determined an interfacial barrier height of 0.7 electron volts (ev) corresponding roughly to one-half of the measured photoresponse threshold energy (1.77 ev).

TUNNEL EMISSION

A number of authors (1, 2, 10, 11) have considered electron tunneling as a current flow mechanism through thin oxide films between conductors or semiconductors. Simmons (1, 2) has considered in detail tunneling of electrons through insulating layers of thickness less than 100 Å separating metals. Because the particular structure under investigation in this report utilizes a film of approximately 50 Å thickness, we will consider tunneling phenomena in some detail.

When the potential barrier to electron motion is set up by an insulating film of less than about 100 angstroms thickness the probability of an electron tunneling through the barrier is finite if

there are empty energy states on the far side of the barrier to receive the electron. Consider the simple one-dimensional problem illustrating a rectangular potential barrier to the flow of electrons from material 1 to material 2 shown in Figure 1.

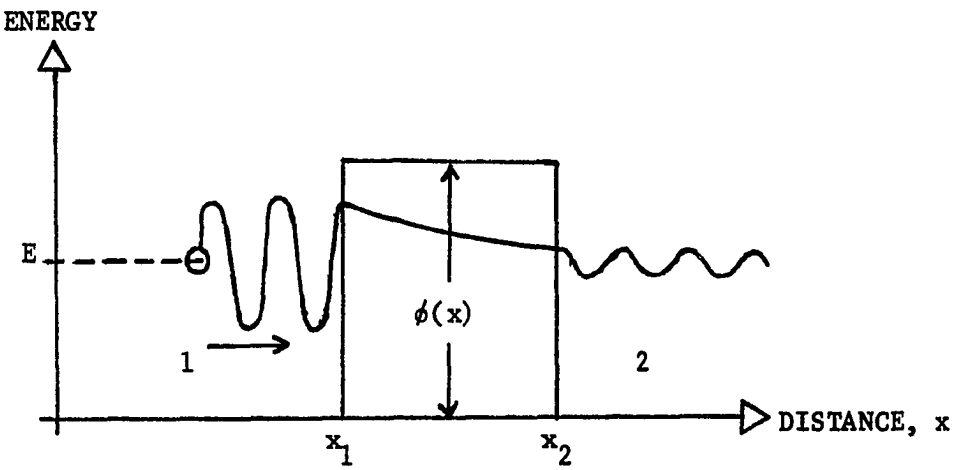


Figure 1. Tunneling Through Insulating Films

The one-dimensional Schrodinger wave equation may be used to describe the wave functions of an electron in this system:

$$-\frac{h^2}{2m}\frac{\partial^2\psi}{\partial x^2} + \phi(x)\psi = E\psi \tag{4}$$

where h = Planck's constant

m = mass of electron

ψ = wave function of electron

$\phi(x)$ = potential barrier

E = energy of incident electron

For the rectangular barrier shown, equation (4) may be solved:

$$\psi = \psi_o \exp i\left(\frac{2mE}{h^2}\right)^{\frac{1}{2}} x \quad \text{for} \quad \begin{matrix} x < x_1 \\ x > x_2 \end{matrix}$$

$$\psi = \psi_o \exp\left[-\left(\frac{2m(\varphi - E)}{h^2}\right)^{\frac{1}{2}}\right] x \quad \text{for } x_1 < x < x_2 \tag{5}$$

where the solutions must be matched at the boundaries. Since the expectation value of finding an electron at x is $|\psi(x)|^2$, the probability that an electron incident on the barrier from the left will pass through the barrier is

$$P(E) = \frac{|\psi(x_2)|^2}{|\psi(x_1)|^2} = \exp\left\{-2\left[\frac{2m(\varphi - E)}{h^2}\right]^{\frac{1}{2}}(x_2 - x_1)\right\} \tag{6}$$

Real potential barriers are almost never the simple rectangular shape shown in Figure 1. However, if the potential barrier is relatively smooth, the WKB approximation may be used to simplify the expressions. The tunneling probability is then

$$P(E) \approx \exp\left\{-\int_a^b \left[\frac{2m}{h}\left(\varphi(x) - E\right)\right]^{\frac{1}{2}} dx\right\} \tag{7}$$

where a and b are the values of x where $\varphi(x) = E$, the so-called classical turning points.

Tunneling may enter into the problem of conduction through thin insulating films in a number of different ways. Some of these are depicted in Figure 2, which illustrates the following:

(a) tunneling from metal directly through insulator into the conduction band of a second metal or semiconductor

(b) (1) tunneling from metal to impurity sites (traps) within the insulator and

(2) tunneling from filled traps in the insulator into the conduction band of the metal or semiconductor

(c) tunneling from metal into conduction band of insulator

(d) (1) tunneling from metal into insulator conduction band and/or

(2) band-to-band tunneling (Zener process) in the insulator

(e) tunneling from metal to surface states located at the insulator-semiconductor interface with energy levels within the band gap of the semiconductor.

Tunnel current densities are calculated by integrating the product of density of states function with the occupation function,

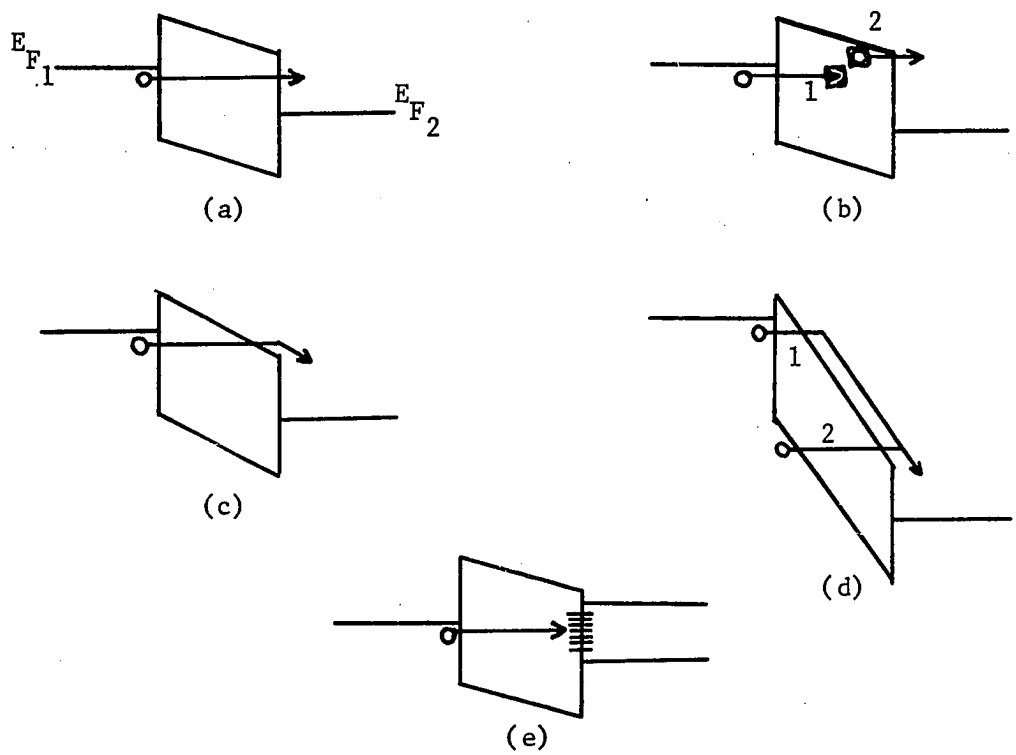


Figure 2. Tunneling Processes Through Insulators

velocity of electrons, and tunneling probability over the range of wave vectors of the electrons available for tunneling,

$$j_x = q \int N(E) f(E) V_x P(E_x) \, d\bar{k} \tag{8}$$

There have been many attempts to calculate equation (8) for specific situations considering such phenomena as image force effects on barrier shape, dielectric constant of the insulator, and effective mass of electrons in the insulator. In most cases only approximate solutions are obtained where many simplifying assumptions have been employed, such as assuming a parabolic barrier or neglecting possible dielectric constant variations.

Before presenting some of the resultant expressions for tunneling current, a discussion of some of the processes which may modify the tunnel current and which seldom have been accounted for analytically will be given. First, carriers injected into the conduction band or

into a trap level of a semiconductor continue to flow toward the positive electrode whether the injection process is tunneling, Schottky emission, or some o her process. These carriers give rise to a space charge near the semiconductor surface which, in turn, may upset the field distribution in the insulator. This disturbance may alter the shape of the potential barrier and affect the carrier injection process. This effect leads to a space-charge limited current.

Also, with large fields across an insulator, as would be the case for small applied voltages and very narrow films, the energy lost by an electron traversing the insulator through ionized impurity and acoustical phonon scattering may be so small that thermal equilibrium cannot be maintained. The electrons in this situation may attain higher average velocities (become so-called "hot" electrons) and new kinds of interactions take place, notably optical phonon scattering, impact ionization, and hole-electron pair production. For these hot electrons, the effects of scattering by ionized impurities and trap sites is considerably reduced.

However, of perhaps greatest importance in relating theoretical calculations of tunneling current to measured data on real insulator systems is the fact that virtually all of the tunneling models assume a nearly perfect crystalline insulator structure. The real situation is considerably different with only small sections of the insulator having local order. This is particularly true for evaporated insulators where no special provisions are made to promote single crystal growth. The effects of crystal defects and impurities in insulator structures are, generally, 1) each imperfection introduces one or more localized energy states in the forbidden band and 2) localized imperfections scatter free charge carriers thereby reducing carrier mobilities. In the case of insulators, imperfections generally introduce donor or acceptor states lying deep in the forbidden band. A large number of these states may be empty in equilibrium and may act to trap excess carriers. Further, trap sites which are full will cause increased scattering of charge carriers. One influence of trap sites on tunneling currents has been discussed by Zaininger in reference (9). The primary effect of charge trapped at trap sites in an insulator is to introduce a space charge which reduces the electric field near the negative electrode thus

effectively causing the tunneling barrier to increase in thickness. Thus, large trapping densities may be expected to effectively stop tunneling currents by this process.

With the preceding ideas in mind, we may consider the simple case of tunneling through thin insulator films between two metals as shown in Figure 3.

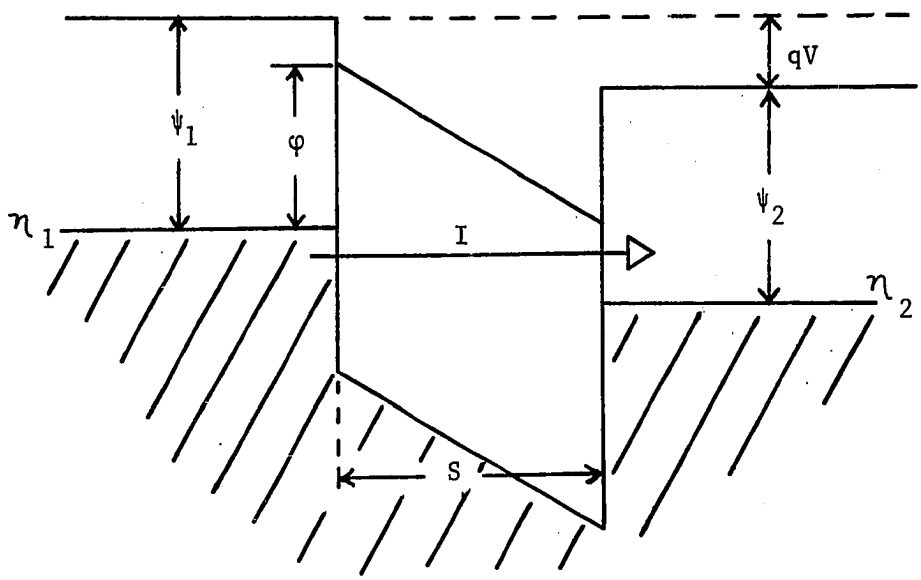


Figure 3. Tunneling in a Metal-Insulator-Metal Structure

In Figure 3 the identification of symbols is:

ψ_1, ψ_2 = work functions of the metal electrodes

η_1, η_2 = Fermi energy level in the metals

ϕ = metal-insulator potential barrier

V = applied voltage

S = thickness of insulator

The volt-ampere relations for tunneling current through the structure of Figure 3 have been calculated in reference (1) as:

(a) for low voltages, $V \approx 0$

$I = K_1 V$ (ohmic behavior)

$$\text{where } K_1 = A\,\frac{3(2m\varphi)^{\frac{1}{2}}}{2s}\,(q/h)^2\,\exp\left[\frac{-4\pi s}{h}(2m\varphi)^{\frac{1}{2}}\right] \tag{9}$$

(b) for $0 < V < \frac{\varphi}{q}$

$$I = K_2\left[(\varphi - \tfrac{qV}{2})\,\exp K_3\,(\varphi - \tfrac{qV}{2})^{\frac{1}{2}} - (\varphi + \tfrac{qV}{2})\,\exp K_3\,(\varphi + \tfrac{qV}{2})^{\frac{1}{2}}\right] \tag{10}$$

$$\text{where } K_2 = \frac{Aq}{2\pi h s^2}\;;\quad K_3 = \frac{-4\pi s}{h}(2m)^{\frac{1}{2}}$$

(c) for $\frac{\varphi}{q} < V < \frac{\varphi + \eta}{q}$

$$I = K_4 V^2\left\{\exp\,(-K_5 V^{-1}) - (1 + \tfrac{2qV}{\varphi})\,\exp\left[-K_5 V^{-1}(1 + \tfrac{2qV}{\varphi})^{\frac{1}{2}}\right]\right\} \tag{11}$$

$$\text{where } K_4 = \frac{A2q^3}{8\pi h\varphi}\;;\quad K_5 = \frac{-4\pi s}{q}\,m^{\frac{1}{2}}\varphi^{3/2}$$

(d) for $V > \frac{\varphi + \eta}{q}$

$$I = K_6 V^2\,\exp\,(-K_7 V^{-1}) \tag{12}$$

$$\text{where } K_6 = \frac{2.2Aq^3}{8\pi h\varphi s^2}\;;\quad K_7 = \frac{8\pi s}{2.96hq}\,(2m)^{\frac{1}{2}}\,\varphi^{3/2}$$

In equations (9) through (12) m = rest mass of electron, q = electron charge, A = cross-sectional area, and φ = barrier height in electron-volts. Note that, although equations (10) through (12) have very complex forms, the ohmic behavior at low voltages shown by equation (9) is consistent with the low voltage tunnel current originally calculated by Esaki (12) for the tunnel diode. At higher voltages the tunnel current is controlled by the availability of empty states into which electrons may tunnel and, in the tunnel diode, the decrease of available states at higher bias values causes the tunneling current to decrease.

The equations shown above for the metal-insulator-metal structure must be considerably modified when one metal is replaced by a semiconductor. When tunneling into a semiconductor is considered, the tunneling current will be primarily determined by the density and energy level of empty states into which the electrons from the metal may tunnel.

Dahlke (11) has considered the tunneling mechanism through thin silicon dioxide films grown in various ambients on p-type silicon surfaces. The silicon used was heavily doped ($N_A = 10^{19} cm^{-3}$) and conductance measurements indicated currents flowing as shown in Figure 4.

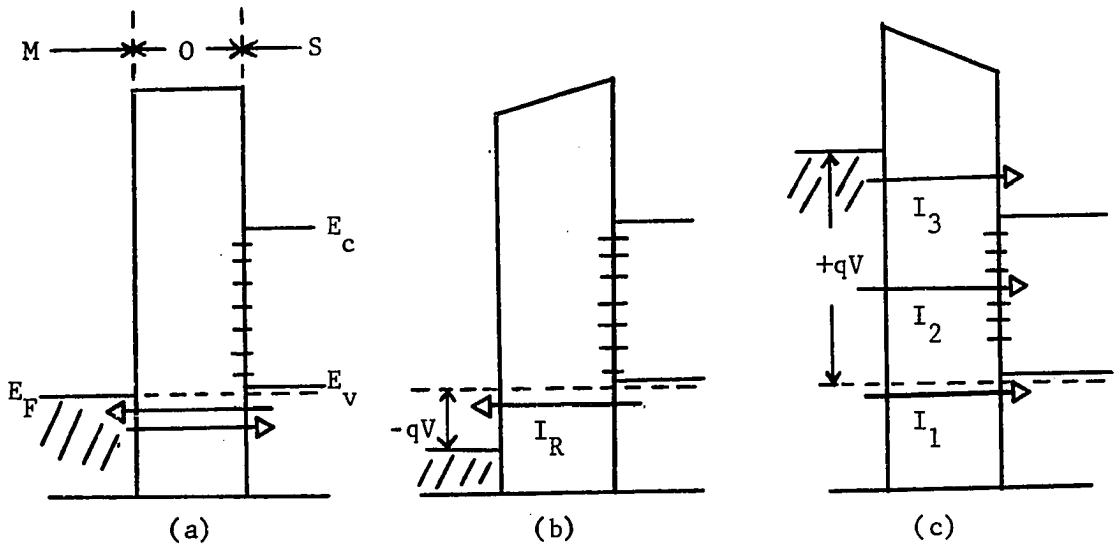


Figure 4. Tunneling in MOS Structure

(a) no bias applied - no current

(b) reverse bias - small current due to valence electrons tunneling into conduction band of metal

(c) forward bias

I_1 = tunneling from metal to valence band at low voltage

I_2 = tunneling from metal to interface states and subsequent recombination with hole from valence band at moderate voltages

I_3 = tunneling of electrons directly into conduction band of semiconductor at high forward voltages

Note that Figure 4 illustrates a method of obtaining information concerning the energy level of interface states and the band edges of the semiconductor. However, the situation shown in Figure 4 neglects two

important effects, i.e., trapping in the oxide or at the oxide-semiconductor interface and possible bending of the semiconductor energy bands near the surface. Band-bending near the surface of a semiconductor will be discussed later.

Gray (10), using vacuum-cleaved p-type silicon and slowly grown thermal oxide coatings, was able to identify tunneling from a metal electrode into fast surface states on the surface of the silicon. A tunneling expression was derived in the form of a transmission factor, G_o, modified by a factor illustrating the effect of the forbidden band of the semiconductor. Although the tunneling expression did not give the volt-ampere relation, peaks in the measured current did indicate the location of two interface states, one located 0.25 ev below the Fermi level of the semiconductor and one located 0.55 ev above the Fermi level. The states into which electrons from the metal were tunneling were found to be the so-called "fast" states with densities of approximately $10^{12}/cm^2$ in agreement with the measurements of Statz, et. al. (14).

CHARGE TRANSPORT via TRAP SITES

Charge transport in the presence of electron (or hole) traps is extremely complex and only a few simple cases have been calculated. When free charge carriers flow through a material containing trapping levels, a certain percentage of the free carriers will be trapped if certain energy considerations are met and the ratio of free charge density to the density of trapped carriers is given by

$$\frac{n_c}{n_t} = \frac{N_c}{N_t} \exp\left[-\frac{\Delta E_t}{kT}\right] \tag{13}$$

where N_c = density of states in conduction band

N_t = density of traps

ΔE_t = ion energy of trap site measured from the appropriate band edge.

As the density of free charge carriers in an insulator with a discrete trap level is increased, the trap sites become filled and the free charge carrier density is no longer reduced because of trapped carriers. Thus, when a discrete trap level becomes filled, the current flow through the

insulator should show a sharp increase. However, the current flowing after the traps are full will not be equal to that of a trap free case because of reduced carrier mobility due to increased scattering by the trap sites.

A calculation of current flow through an insulator assuming a single discrete trap level has been performed by Frenkel (13). This process, known as the Poole-Frenkel effect (3) assumes a conduction process limited by the field-enhanced thermal emission of electrons from a trap level into the conduction band. The current for this process is given by

$$I = A\, G_o \exp\left[KV^{\frac{1}{2}} - X/kT\right] \tag{14}$$

where A = cross-sectional area

G_o = constant conductance term

V = applied voltage

X = energy difference between trap level and bottom of insulator conduction band.

The coefficient K is given by

$$K = 2\left[\frac{q}{\epsilon\epsilon_o a}\right]^{\frac{1}{2}} (q/kT) \tag{15}$$

where the parameters of equation (15) have been identified earlier.

Note that the form of equation (14) is very similar to that of equation (1) for Schottky emission with the slope of the ln I versus $V^{\frac{1}{2}}$ curve twice that for Schottky emission.

Hartman, et. al., (3) by measurements on metal-evaporated SiO-metal structures, determined that conduction through SiO was neither Schottky emission nor a Poole-Frenkel process but a form of bulk-limited conduction with trapping influences. An empirical relation of the form

$$I = Ka \exp\left(BV^{\frac{1}{2}} - \gamma/kT\right)\left[1 - \exp\left(-B^2V\right)\right] \tag{16}$$

was found where a = oxide thickness, $B = \frac{1}{\sqrt{a}}\left(\frac{\psi}{kT} + \varphi\right)$, and K, ψ, φ, and γ are constants. A calculation of B (the slope of the curve of ln I

versus $V^{\frac{1}{2}}$) for a 100 Å film at room temperature yields a value of $B \approx 8.5\ (\text{volts})^{-\frac{1}{2}}$.

The processes by which electrons enter and leave trap sites all tend to have long time constants, particularly for the discharge of a trap site. Thermal equilibrium then exists only under dc conditions in a material with large trap concentrations. Ac voltages applied to systems with large numbers of trap sites exhibit large hysteresis effects because of the difference between charge and discharge times for the traps. To a certain extent, therefore, transient or dc excitation and the resulting charge storage illustrate trap presence.

SEMICONDUCTOR SURFACES

The conditions at the surface of the semiconductor may influence charge transport through MOS structures in a number of ways. If the surface of the semiconductor has surface states in which charge may be trapped or surface states which act as recombination centers both the oxide layer on top of the surface and the bulk semiconductor underneath will be affected or disturbed. Four basic conditions may exist in which the bulk semiconductor properties near the surface are influenced by the surface states. These four conditions are illustrated in Figure 5 using p-type semiconductor as an example.

Let us call the electrostatic potential at the surface ϕ_s. The potential V at any point with respect to the potential in the bulk far from the surface is given by

$$V = \phi - \phi_b \tag{17}$$

where $\phi_b = (E_i - E_F)/q$, E_i = intrinsic position of Fermi level and E_F = position of Fermi level for p-type material. The surface barrier potential is

$$V_s = \phi_s - \phi_b \tag{18}$$

and the four conditions of Figure 5 may be described as follows:

(a) $V_s < 0$, $\phi_s < \phi_b$; an accumulation of majority carriers

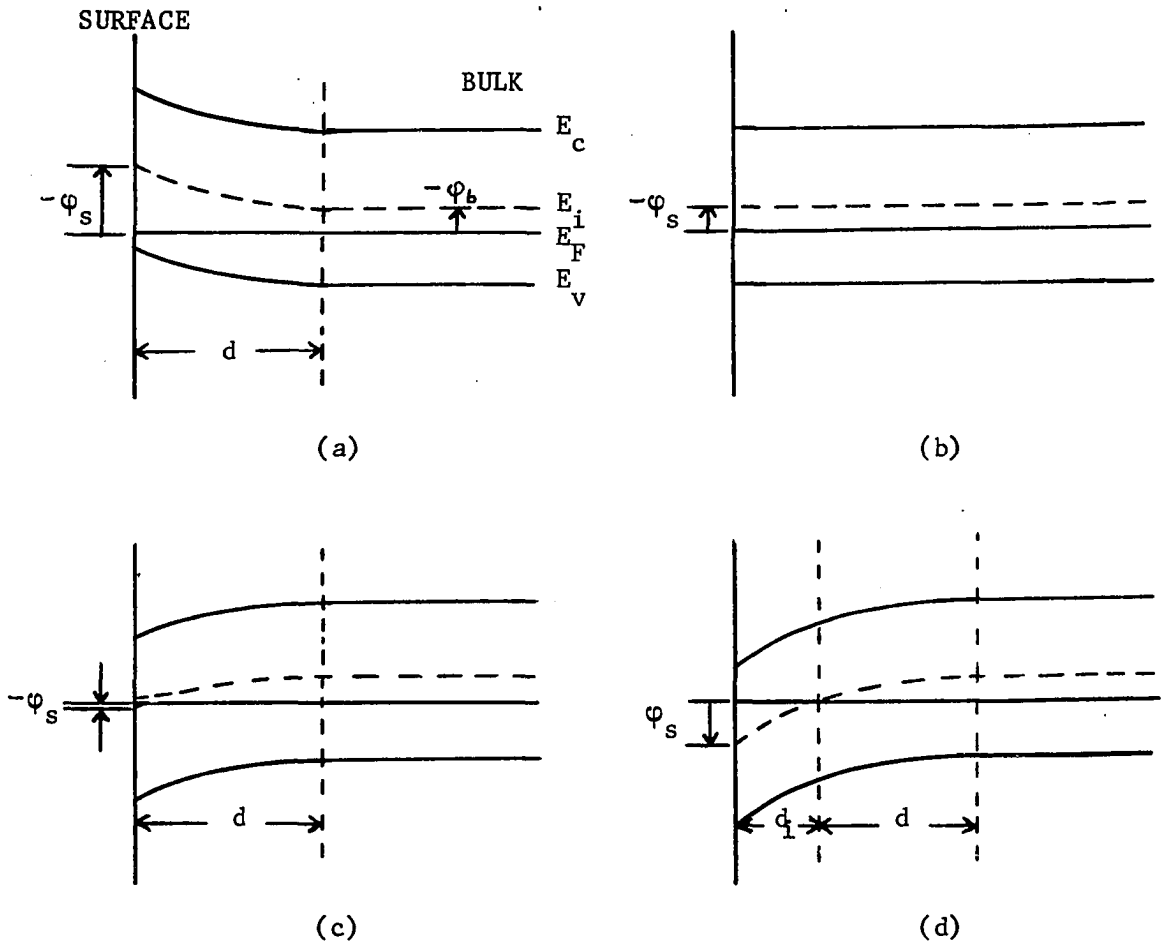


Figure 5. Surface Conditions on p-type Semiconductors (a) accumulation layer formation, (b) flat band condition, (c) depletion layer formation, (d) inversion layer formation.

occurs at the surface, energy bands bent up; d is the depth of space-charge region -

(b) $V_s = 0$, $\phi_s = \phi_b$; no surface barrier, bands are flat, no space-charge region -

(c) $V_s > 0$, $|V_s| < |\phi_b|$; depletion of majority carriers near surface occurs, surface itself is near-intrinsic -

(d) $V_s > 0$, $|V_s| \geq |\phi_b|$; majority carrier density near surface depressed below minority carrier level, n-type inversion layer forms on p-type material.

As an example of the range of values of surface potential necessary for the conditions of Figure 5, ϕ_b for p-type silicon with a resistivity of one ohm-cm ($N_A \approx 1.6 \times 10^{16}$) is

$$\phi_b \approx \frac{kT}{q} \ln \frac{N_A}{n_i} \tag{19}$$

$$= -0.36 \text{ volts.}$$

Therefore, the four conditions of Figure 5 could be set up as:

(a) accumulation layer $\phi_s < -0.36$ volts

(b) flat band $\phi_s = -0.36$ v

(c) depletion layer $-0.36 \text{ v} < \phi_s < 0.00$ v

(d) inversion layer $\phi_s > 0.00$ v.

Technical surfaces, even those with grown oxides on top, are usually of type (c) for p-type material or type (a) for n-type material In other words, an etched surface tends to be n-type regardless of the bulk type.

Etched semiconductors exposed to room atmosphere have been found to have an oxide layer of variable thickness plus adsorbed impurities including oxygen molecules and water molecules. This additional surface layer is thought to contain positive charge which induces a negative charge in the semiconductor and thus tends to form the n-type layer. The thickness of this layer of oxide and contaminants has been estimated between 10 and 60 angstroms. (7)

Besides the band-bending in the semiconductor the surface of an etched semiconductor (here the surface includes the contamination layer) introduces what we have called "fast" and "slow" surface states. It is thought that the fast states which are in good communication with the bulk are located at the interface between the actual semiconductor surface and the contamination layer while the slow states reside within the contamination layer. The fast states have been found to have a density of about $10^{12}/\text{cm}^2$ corresponding to something less than one fast state per surface semiconductor atom. This is consistent with theoretical calculations carried out by Tamm and Shockley (7) on the states introduced by abrupt termination of the regular crystalline lattice at

the surface. Much less is known concerning the slow states, although many studies have shown them to be dependent on gaseous ambients. The slow states have been attributed to mobile ions, oxygen or water molecules, gases adsorbed into the surface contaminant layer, and a number of other causes. It has been reported that the silicon-oxygen bond in the oxide layer is partly ionic and partly covalent. Perhaps some lattice polarization of the ionic bond may cause some of the slow state effects. It has been found that the addition of phosphorus during the process of growing silicon dioxide films at high temperatures substantially lowers the slow state density in the oxide and this process is now common in the construction of protective oxide films.

THEORETICAL MODEL

The theoretical model for the metal-evaporated silicon monoxide-p-type silicon under consideration is pictured in Figure 6. The model illustrates the following ideas developed in the preceding sections;

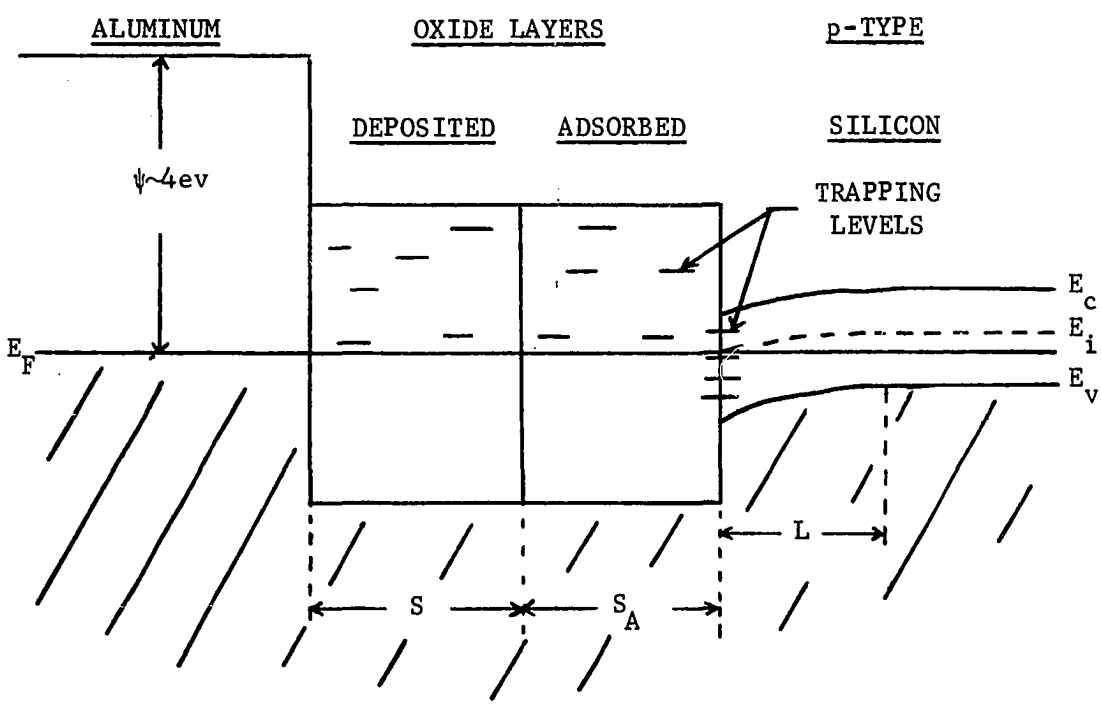


Figure 6. MOS Model

(a) the deposited oxide layer is shown as a perfect insulator (band gap $\approx$ 4 ev) with the addition of electron trapping levels distributed throughout the oxide and with energies within the band gap.

(b) the layer of oxide, impurities, etc., normally found on a technical surface is shown and labeled as the adsorbed layer; this layer also contains various trap sites.

(c) the silicon surface is characterized by additional trap sites and band-bending in the semiconductor which produces a depletion layer in the p-type semiconductor.

The parameters identified in Figure 6 are:

S = deposited oxide layer thickness ($\sim$ 50 Å)

S_A = adsorbed oxide layer thickness ($\sim$ 10 - 60 Å)

L = effective width of depletion region

E_c, E_v, E_i = conduction, valence, and intrinsic energy levels in semiconductor

E_F = Fermi energy level.

The depletion region width is of the order of one effective Debye length given by

$$L = \left[\frac{\epsilon_s kT}{q^2 p_b}\right]^{\frac{1}{2}} \tag{20}$$

where ϵ_s is the dielectric constant near the surface and p_b is the bulk hole density. For the sample under consideration with 1Ω-cm p-type silicon, L is of the order of 3×10^{-6} cm.

Because the evaporated oxide layer can be expected to have a large defect density, it is probable that current flow through this structure will be controlled by traps in the oxide layers. However, at larger bias where the field across the oxide approaches the breakdown field, current flow will probably be dominated by the properties of the semiconductor, in particular by operations taking place in the depletion region.

The expected high trap densities will cause considerable hysteresis in ac volt-ampere measurements and introduce additional bias dependence in the ac capacitance measurements. The ac capacitance of the MOS structure of Figure 6 is expected to be composed of basically

two capacitances: the parallel-plate capacitance of the oxide layer in series with the depletion layer capacitance of the semiconductor. In the simplest model of ac capacitance it could be expected that the oxide capacitance is independent of bias while the depletion capacitance will increase with forward bias in some fashion.

CHAPTER III

DEVICE PREPARATION - EXPERIMENTAL PROCEDURES

DEVICE PREPARATION

The experimental MOS devices were constructed on p-type 1.0 Ω-cm silicon single crystals. The crystals were approximately one inch in diameter and 0.02 inch thick with the surface in the (111) crystal plane. After polishing with fine aluminum oxide powder, the surfaces of the crystal were washed and then etched to remove scratches and mechanical damage for about 5 minutes in an acid etch composed of 3 parts hydrofluoric acid, 15 parts nitric acid, and 5 parts acetic acid. The etching process was stopped by flooding with distilled, de-ionized water until the solution achieved a volume resistivity of 10 megohm-cm. The silicon crystals were then removed from the water bath and allowed to dry on a laminar flow clean table.

After drying, the crystal slice was placed in a holder and mounted in a Veeco VE-400 Vacuum Evaporator unit. A tungsten filament was charged with aluminum chunks and the system was evacuated to a pressure of 5×10^{-6} mm Hg. The back electrode contact was then formed by evaporating the aluminum using resistance heating. A thickness of greater than 2000 $\mathring{A}$ of aluminum was deposited for the back contact. All thickness measurements were made during the evaporation runs using a Sloan Instruments DTM-2a Deposition Monitor in conjunction with a Hewlett-Packard model 524 Counter which measures thickness of deposits in terms of the frequency shift of an exposed 5 MHz crystal oscillator.

After returning the vacuum system to atmospheric pressure, the crystal was turned over in its holder and a baffled tungsten evaporation source was prepared with chunks of silicon monoxide. A layer of silicon monoxide was evaporated on the exposed silicon surface after a second

pump-down to 5 X 10^{-6} mm Hg pressure. The oxide evaporation was stopped at an indicated thickness of 50 Å.

The vacuum system was again recycled and an evaporation mask of stainless steel, 3 mils thick, was clamped over the oxide surface. About 20 small square openings (area $\approx$ 0.14 cm^2) had previously been photo-etched in the stainless steel mask. After pump-down the aluminum top electrode was deposited to a thickness of about 2000 Å.

Final preparation of the sample devices concerned lead attachment. The back contact was soldered to the copper foil of a small section of copper-covered printed circuit board. A mixture of tin-lead and indium-tin solder was used along with a special aluminum flux and a low-temperature soldering iron. Contacts were then made from small copper islands on the printed circuit board to the top aluminum contacts. The contact wires (gold-plated copper) were soldered to the copper islands and then attached to the aluminum top contacts using two methods: (1) on some samples the contact wire was soldered to the aluminum contact using indium-tin solder and an aluminum flux and (2) other samples used a silver paste to seal the contact wire to the aluminum after slight pressure was applied to break through the aluminum oxide coating. No differences could be observed between the electrical volt-ampere characteristics of the samples made with the different methods. Therefore, it is believed that good, low-resistance, ohmic contacts were achieved to the aluminum electrodes.

EXPERIMENTAL MEASUREMENTS

The first measurements made on the samples were dc volt-ampere measurements using a battery and potentiometer to set various bias voltages with a Keithley model 600 Electrometer to measure current and a Keithley model 610 B Electrometer to measure the voltage across the device. The current measurement included leakage current through the voltmeter. However, because the 610 B has an impedance of 10^{14} ohms shunted by 22 picofarads, this additional current was negligible compared with the current through the sample devices. Because of the small voltages and currents being measured, the samples, along with the adjustable bias source, were placed in a well-shielded enclosure and

shielded cables were used to eliminate static field influences on the metering equipment. All measurements with respect to bias voltage were carried out as near as possible in equilibrium conditions, i.e., the bias voltage was changed slowly and all readings were given several minutes to stabilize. This same procedure was followed for the capacitance and conductance measurements.

Ac volt-ampere measurements were made using the Tektronix model 575 Transistor Curve Tracer. Because the curve tracer applies a sweeping bias voltage at 60 Hz to test devices which is either positive or negative depending on a switch setting, a battery source was connected to bias the devices to -4.5 volts so that the curve tracer could display a characteristic from reverse through forward bias levels. Photographs were obtained of several samples to illustrate in particular the charge storage hysteresis effect and breakdown effects.

The volt-ampere measurements described above were performed at room temperature and, also, several samples were cooled to 195^{o} K (dry ice temperature) and the runs were repeated. The data obtained from the low-temperature runs was not too reliable because of difficulties in reading the small currents involved and difficulties in maintaining the temperature constant enough to eliminate fluctuations in readings.

Ac capacitance and conductance measurements were made on the samples using the Boonton Measurements model 74C-S8 Capacitance Bridge which has a test frequency of 100 kHz. A high frequency bridge was used for the differential capacitance and conductance measurements to eliminate hysteresis effects due to charging and discharging of slow states or electron traps. Charge trapped in slow states would only affect capacitance measurements through space charge influences on the semiconductor depletion region. In all cases but one the bias changes were made slowly as before. However, a series of measurements were made involing rapid switching of bias voltage and subsequent measurements made at regular time intervals.

Additional measurements of capacitance were made at a lower frequence (1 kHz) using the General Radio model 1650 A Impedance Bridge. These measurements were made to determine if the capacitance was frequency dependent.

CHAPTER IV

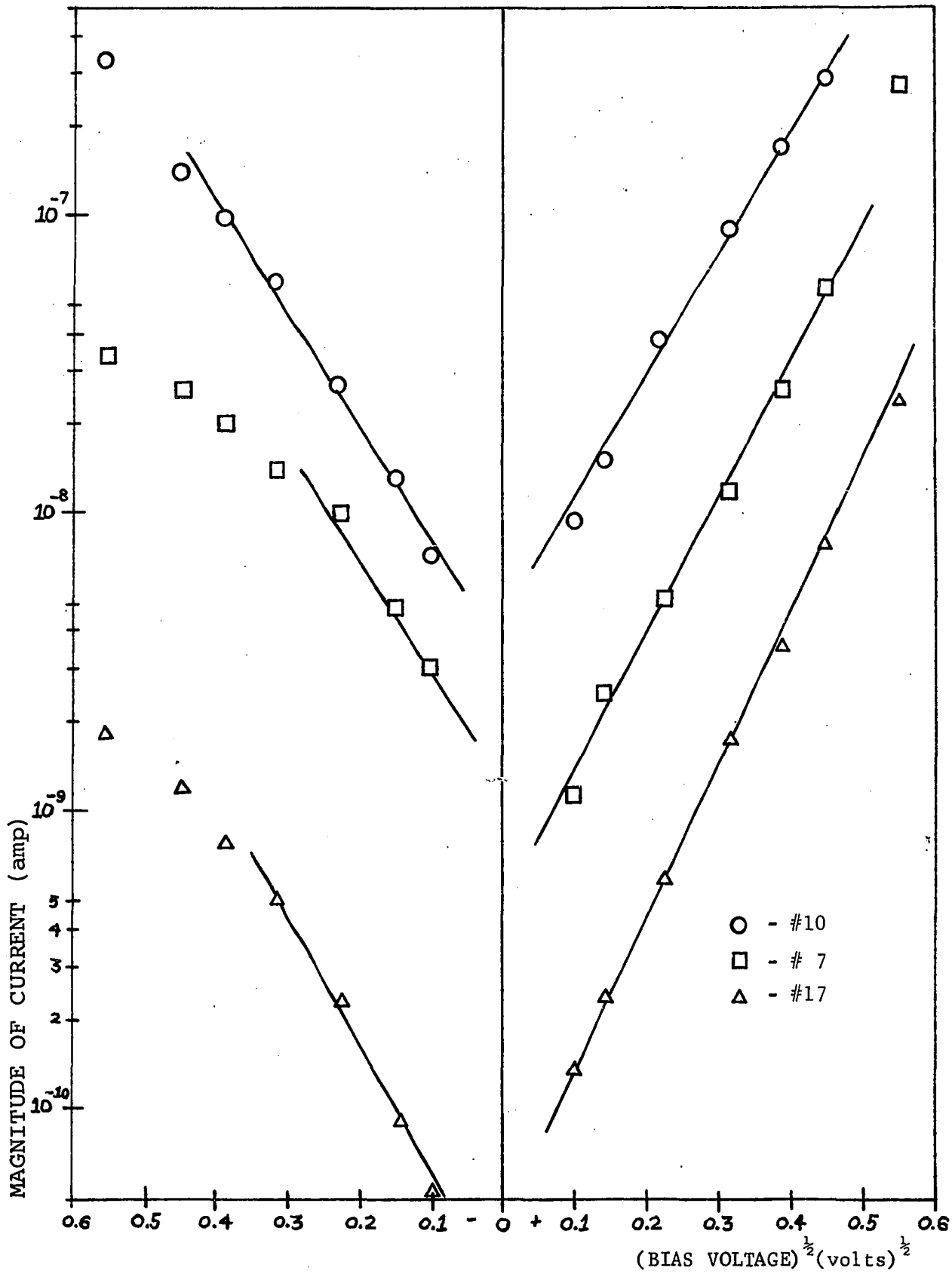
EXPERIMENTAL RESULTS

The results of the static (dc) volt-ampere measurements of typical sample MOS devices are shown in Figure 7 where $\ln|I|$ is plotted versus the square root of the bias voltage. The applied voltage was described as forward bias when the positive of the bias source was connected to the semiconductor in agreement with previous practice. Although the curves for all samples exhibited roughly the same slope for low bias voltages, the zero-voltage current intercept varied considerably among the various samples as shown for the three samples in Figure 7. The straight line portions of the curves shown in Figure 7 illustrates how well the measured data agrees with a current mechanism which is dominated by electron trapping.

In order to illustrate the behavior for large bias voltages, the results of one sample are plotted in Figure 8 where $\ln|I|$ is plotted versus V. Figure 7 illustrates a current dependence at low voltages on $\exp(cV^{\frac{1}{2}})$ while at larger voltages, Figure 8 indicates a shift to the form $I \propto \exp(cV)$.

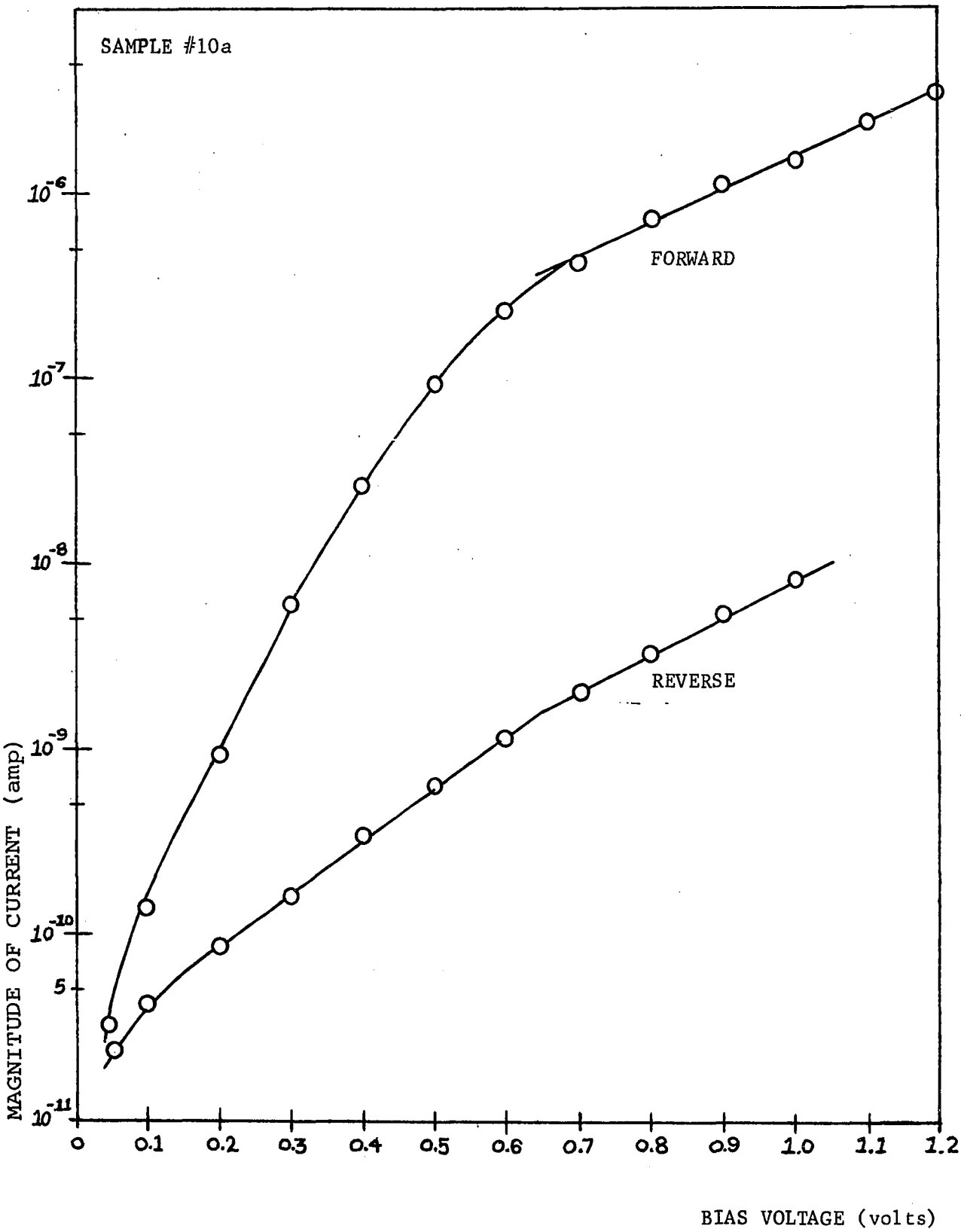
Representation of typical ac volt-ampere characteristics for three samples are shown in Figure 9 where the charge storage is very evident. Also, ohmic behavior is indicated at about +2.0 volts while all the devices tested exhibited reverse breakdown voltages in excess of 10 volts. Figure 9 also indicates the abrupt decrease in charge storage for voltages greater than 2 volts and less than -1 volts illustrating filling of electron traps.

High frequency capacitance measurements as a function of bias voltage for a typical sample are shown in Figure 10. Part (b) of Figure 10 is an expanded plot of the data of Figure 10(a) for low



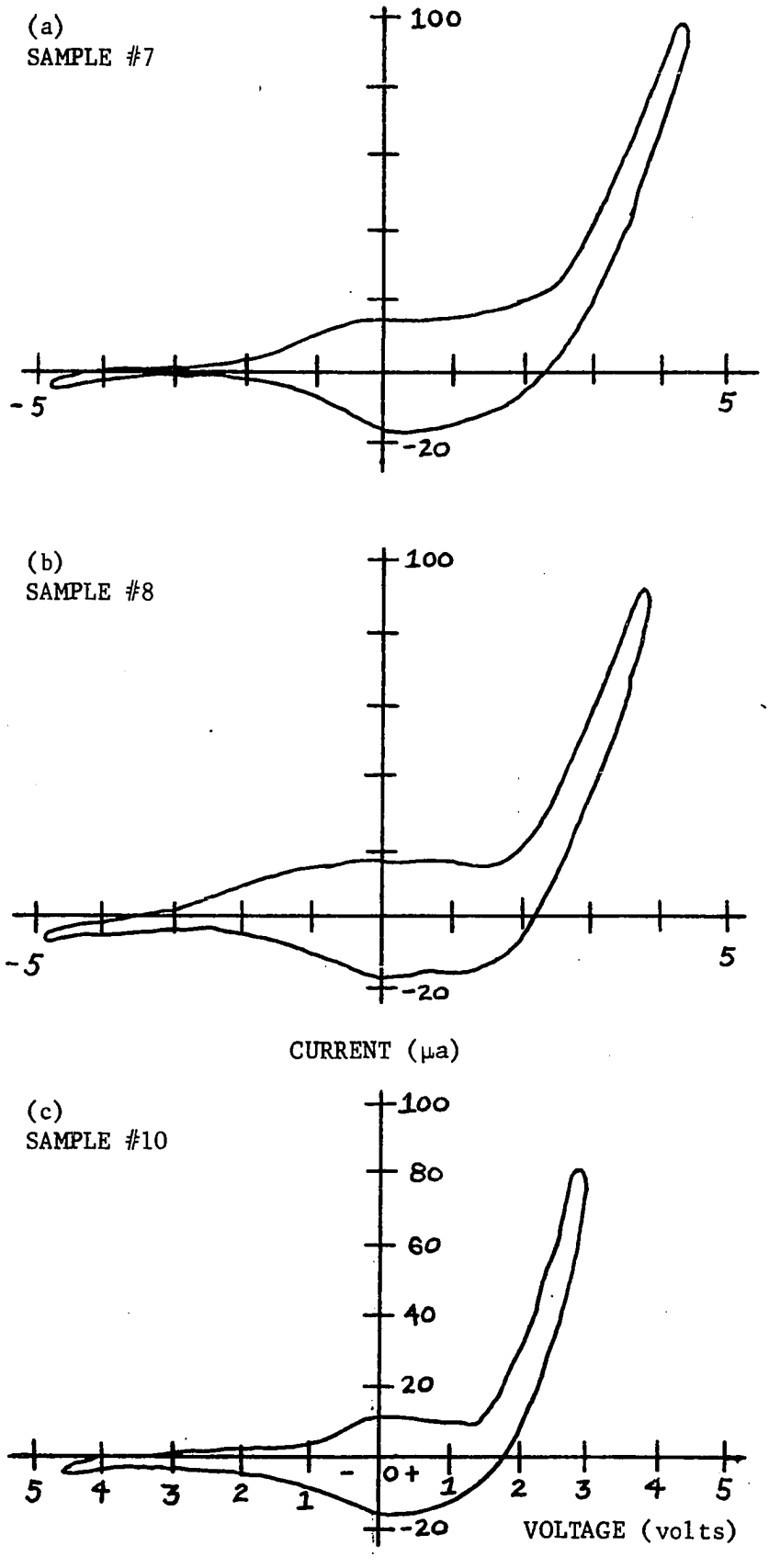
Low-Voltage Static Characteristics

Figure 7.

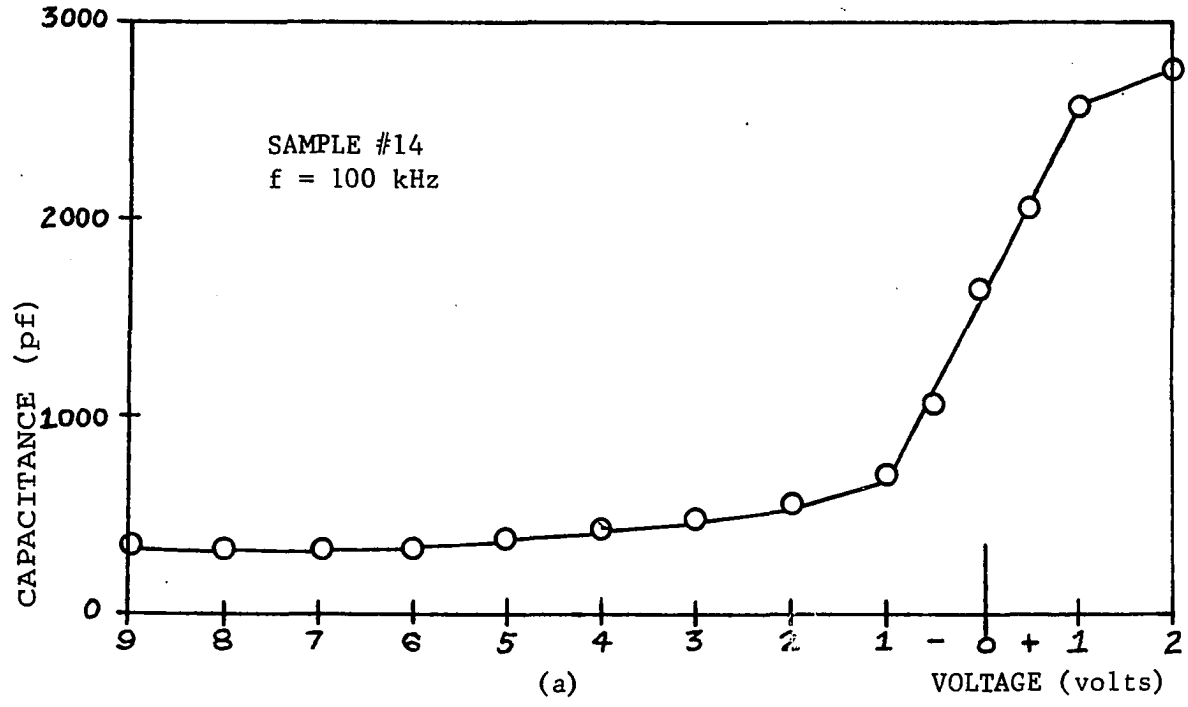


Medium-Voltage Static Characteristics

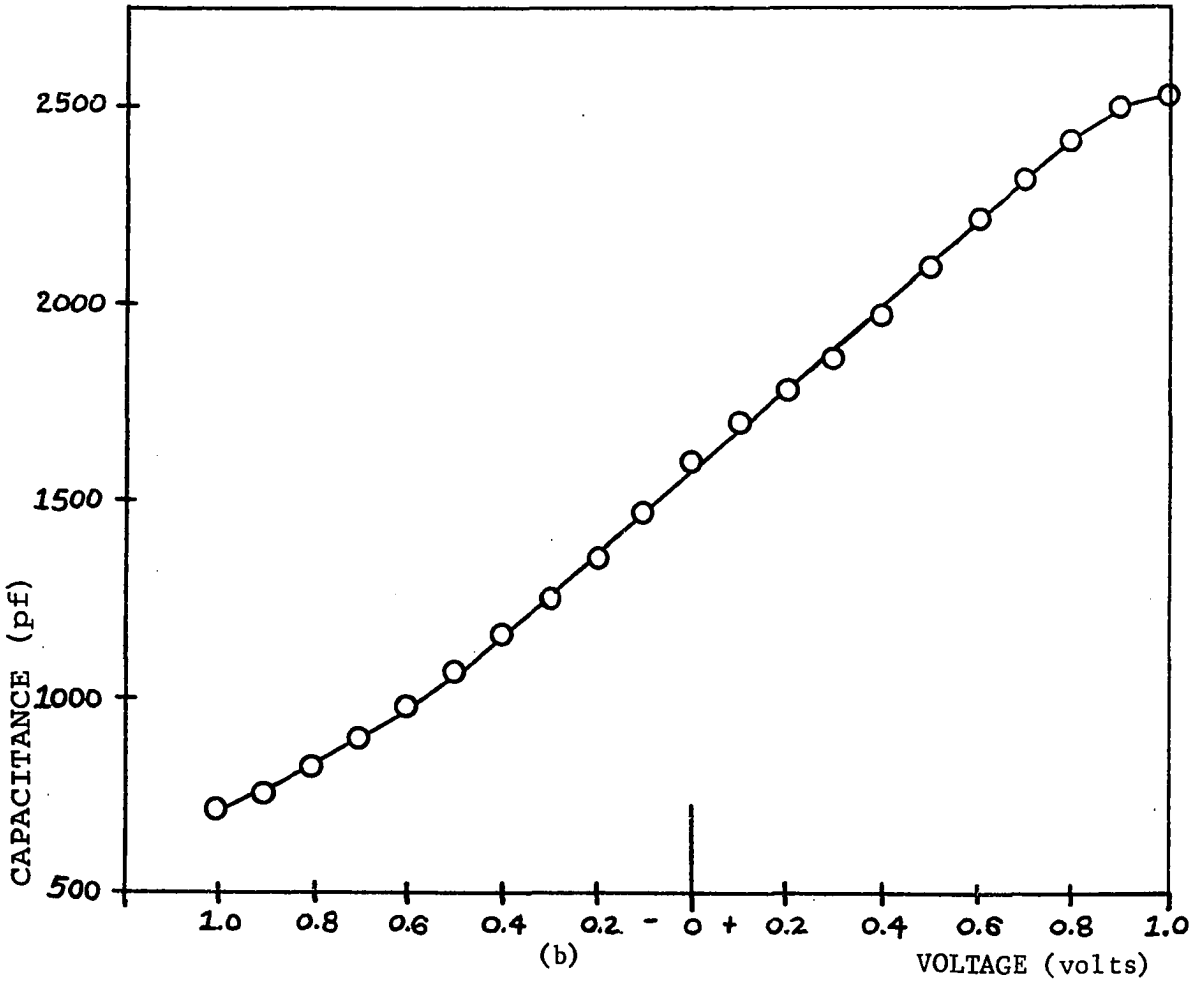
Figure 8.



Dynamic Characteristics
Figure 9.



(a)



(b)

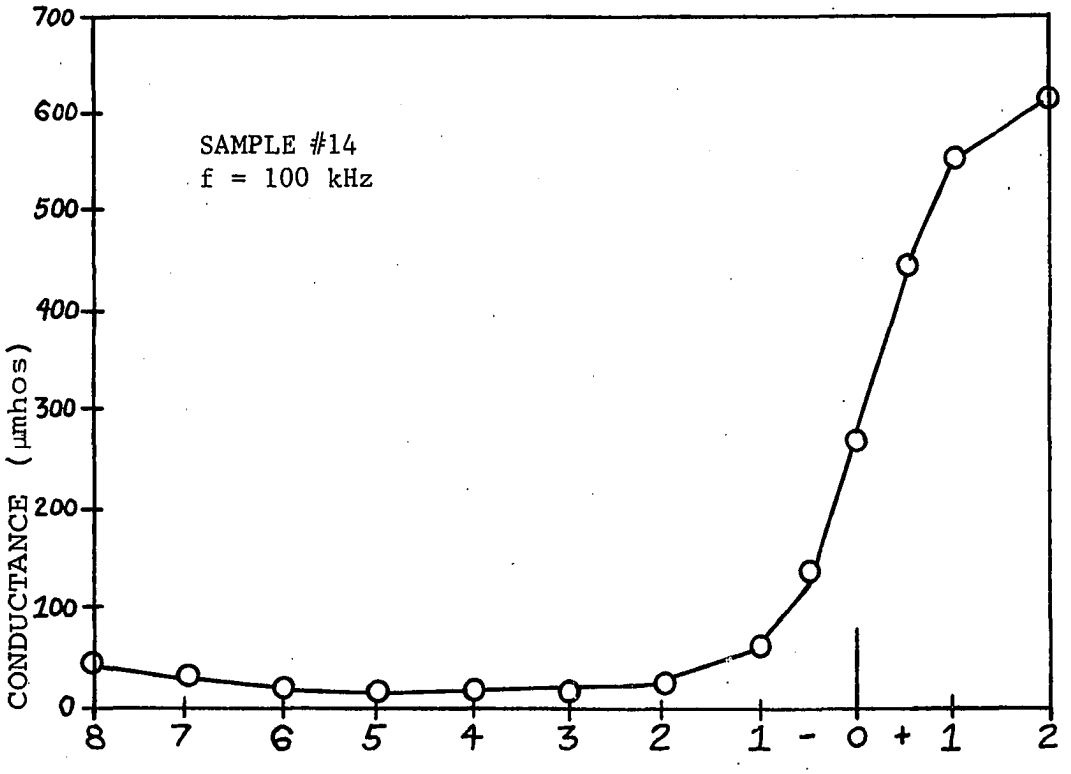
Ac Cap vs Bias (100 kHz)
Figure 10.

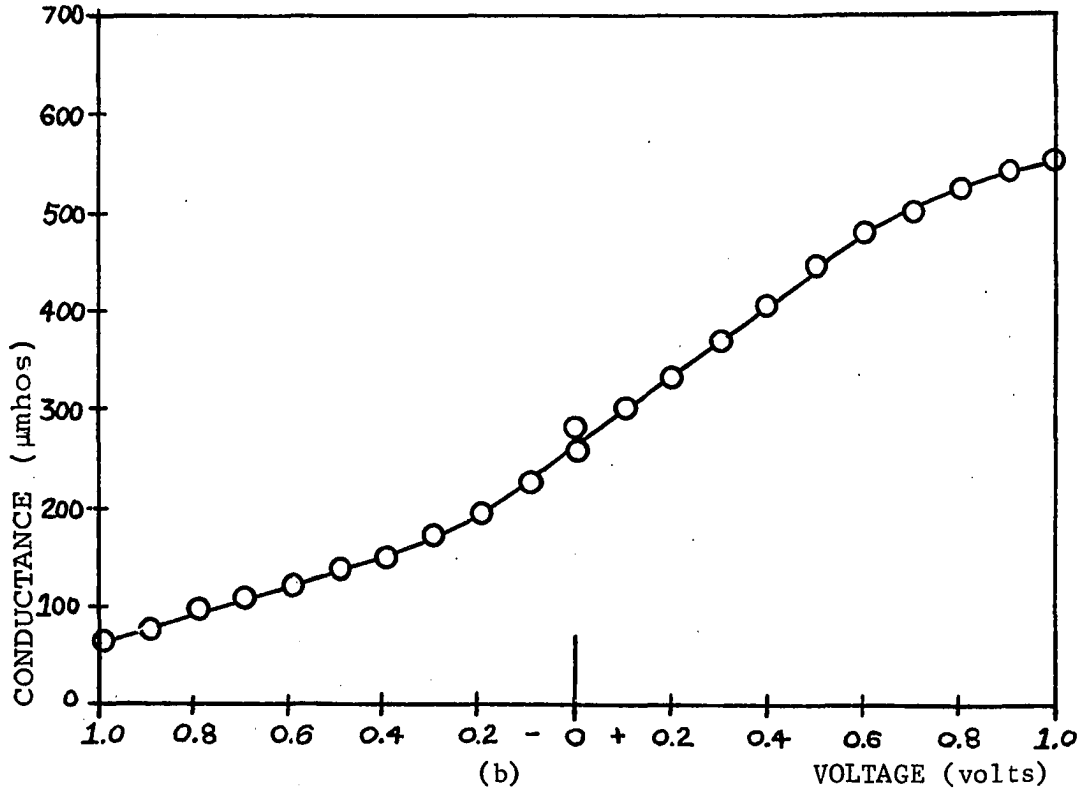
voltages. The straight-line portion of the curve in Figure 10(b) indicating a linear capacitance versus voltage variation covers about the same bias voltage range as the linear range of the curve of $\ln |I|$ versus $V^{\frac{1}{2}}$.

The high frequency conductance of a typical sample is shown in Figure 11. Two values of conductance at zero bias are shown in Figure 11(b), the upper value obtained at the beginning of the test and the lower value at the end of the test. The discrepancy between the zero voltage conductance values is indicative of the long times required to discharge trapped charges. In general, the high frequency conductance varied with bias in the same fashion as the high frequency capacitance. This variation with bias is indicative of the changes in the semiconductor depletion layer because of charge trapped in the oxide trap sites.

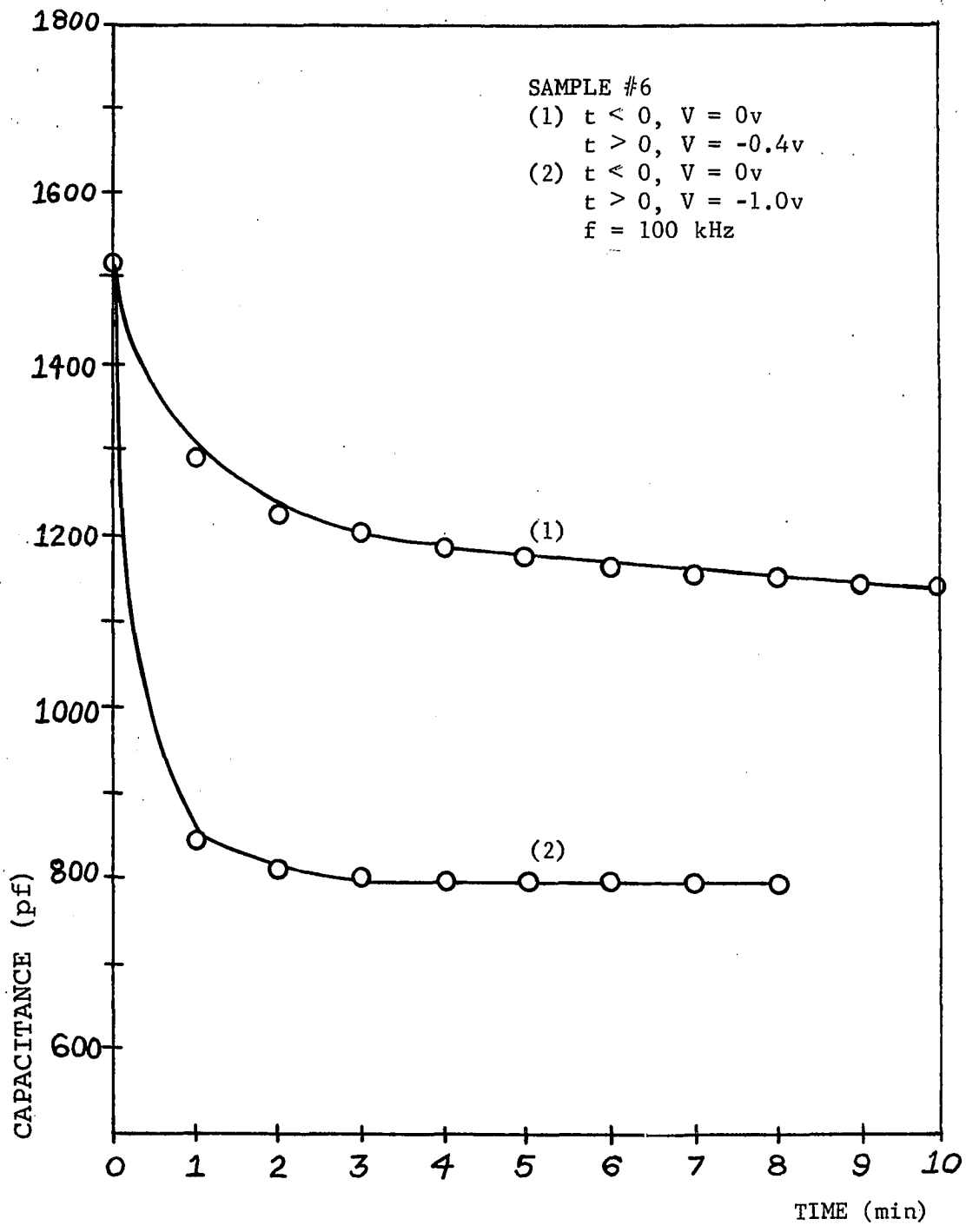
In order to gain some insight into the times required to charge and discharge the slow trap sites a number of experiments were conducted in which the ac capacitance and conductance were measured at regular time intervals following the sudden application or removal of bias voltage. The resultant charge and discharge curves are shown in Figures 12, 13, and 14. Note particularly the long recovery times indicated in the figures. In most cases the original value of capacitance or conductance was only achieved after a period of about one-half hour after the bias was switched off.

The capacitance of several samples was measured at a frequency of 1 kHz and the results for a typical sample are shown in Figure 15. Although the accuracy of these readings is somewhat less than that of the high frequency measurements (because of equipment limitations), the curves of Figure 15 do indicate that the device capacitance has a considerable frequency dependence, which is to be expected if the trapping sites in the oxide have a distribution of time constants. The peak in the low frequency capacitance curve at a forward voltage of about 100 millivolts indicates the probable existence of a large trap density either in the oxide or at the silicon surface with an energy level about 0.1 ev above the Fermi level.



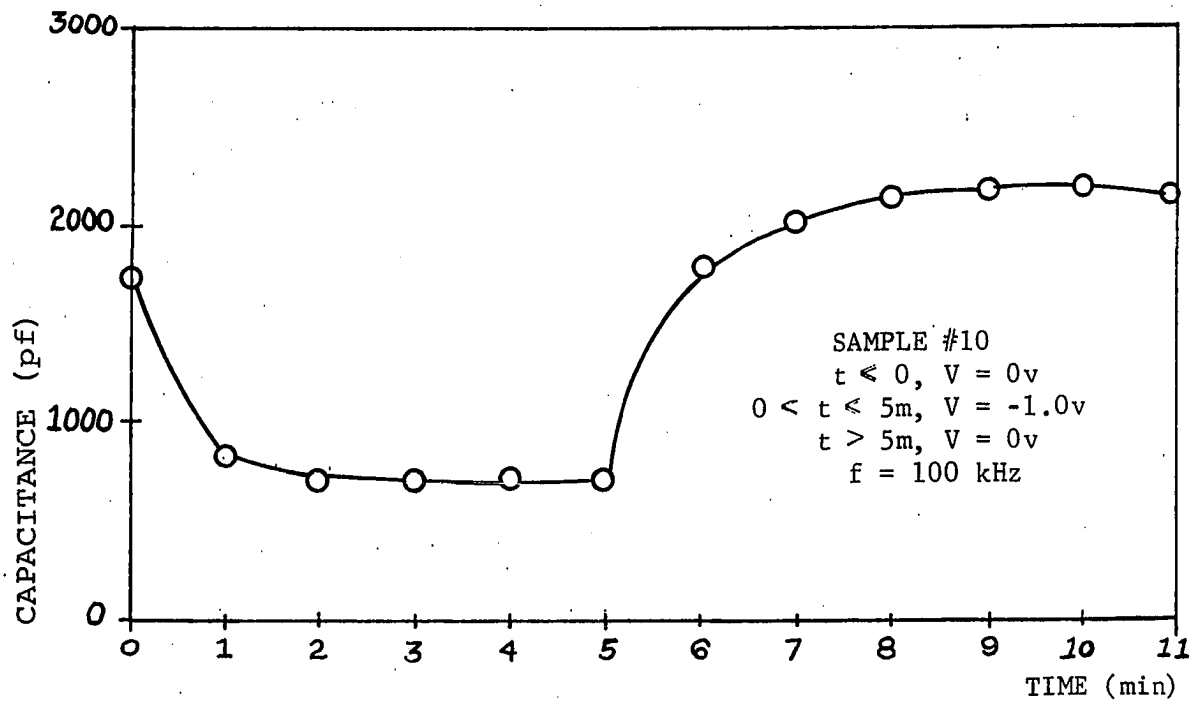


Ac Conductance vs Bias
Figure 11.

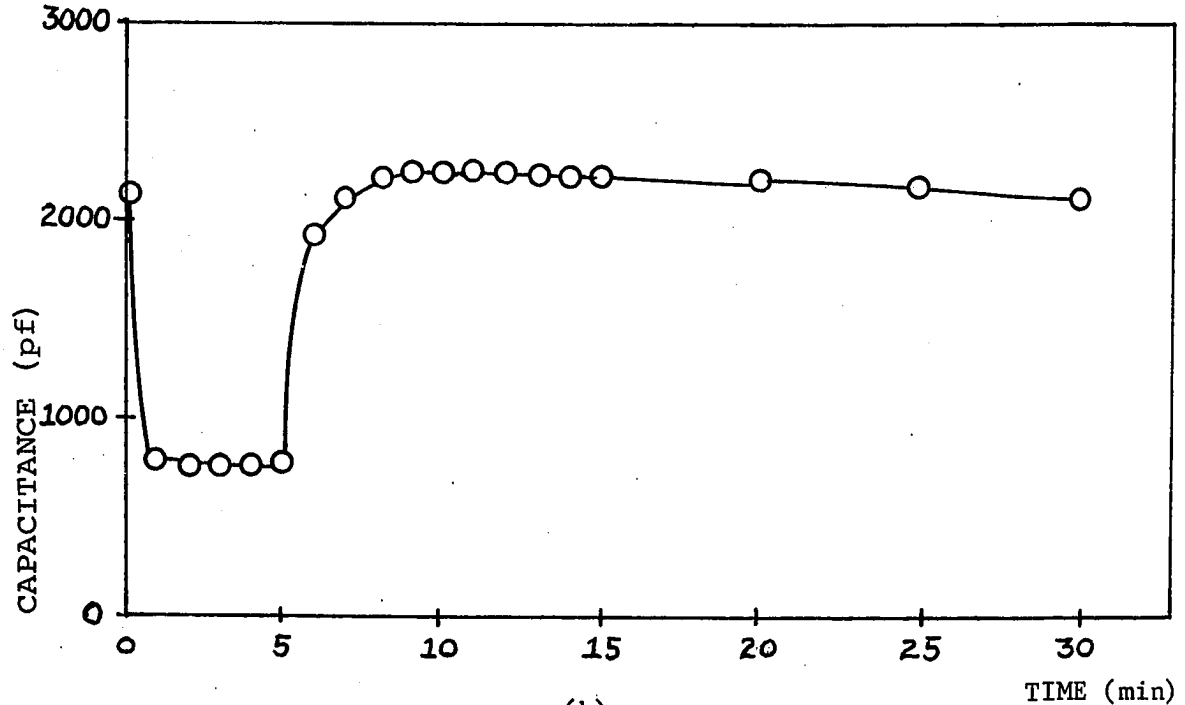


CAPACITANCE TIME DEPENDENCE (REVERSE BIAS)

Figure 12.



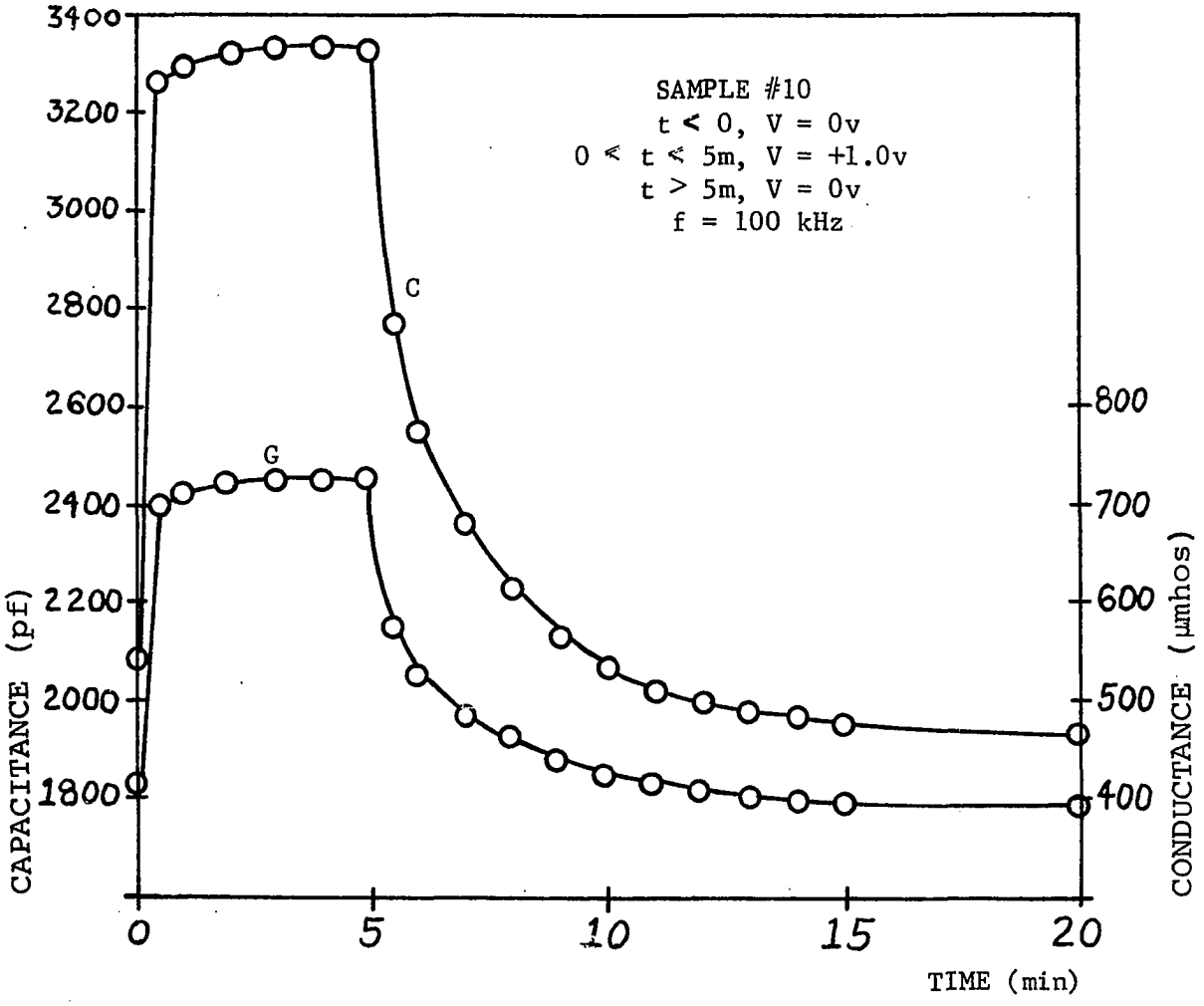
(a)



(b)

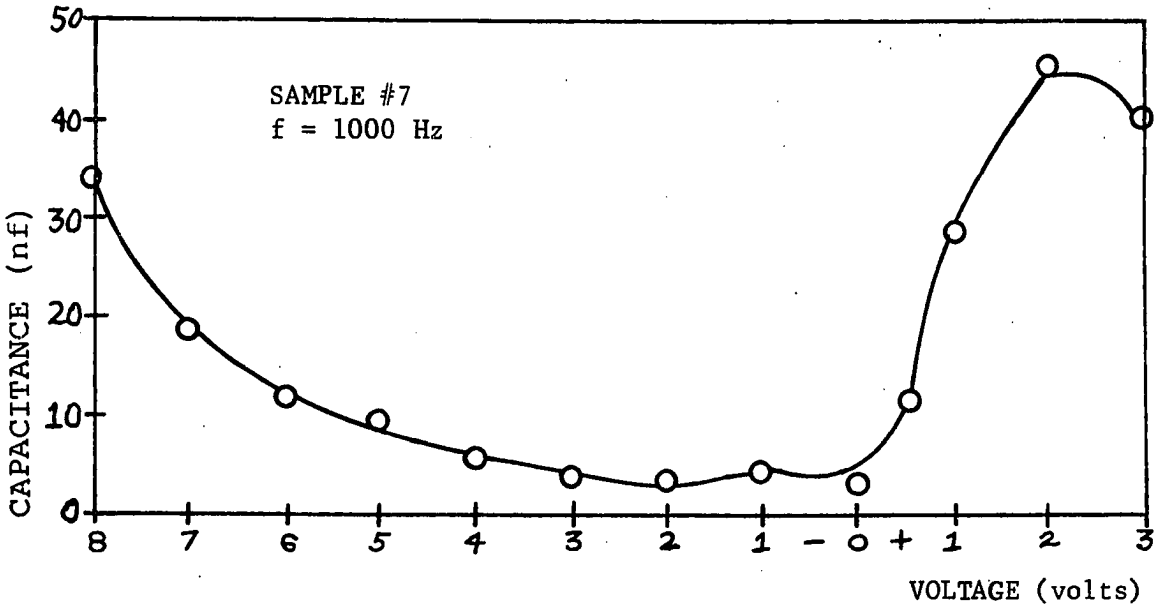
CAPACITIVE CHARGE AND DISCHARGE (REVERSE BIAS)

Figure 13.

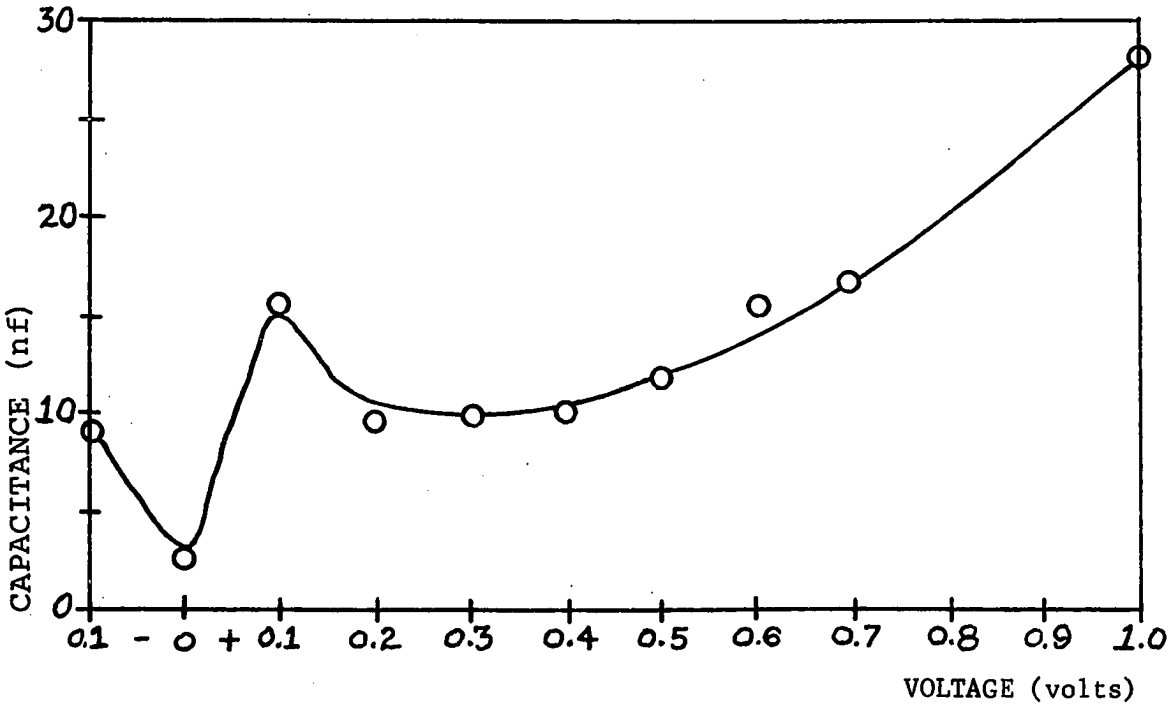


CAPACITANCE AND CONDUCTANCE TIME DEPENDENCE (FORWARD BIAS)

Figure 14.



(a)



(b)

LOW FREQUENCY CAPACITANCE vs. BIAS

Figure 15.

CHAPTER V

INTERPRETATION AND DISCUSSION OF RESULTS - CONCLUSIONS

The measured dc volt-ampere characteristics along with the results of the ac measurements indicate three regions of operation for the MOS devices investigated according to the level of bias voltage applied. For low bias voltages, corresponding to values of voltage which place the metal Fermi level opposite the band gap of the silicon, the current through the device is dominated by trapping processes in the oxide. In this region the current can be expressed as

$$I \propto \exp\left(BV^{\frac{1}{2}}\right) \text{ for } -0.5V < V < 0.5V. \tag{21}$$

The value of B as determined from the curves of Figure 7 is approximately 10 $(\text{volts})^{\frac{1}{2}}$. This value compares closely to the value of voltage coefficient, B, determined by Hartman, et. al., (3) as 8.5 $(\text{volts})^{-\frac{1}{2}}$ for an oxide thickness of 100 Å. Although the current equation (21) is of the same general form as equations for Schottky emission and Poole-Frenkel conduction, it is believed that the conduction process is controlled by a distribution of trapping levels in the oxide layer with the factor B given roughly as

$$B \approx \frac{1}{2}(q/\varepsilon\varepsilon_o a)^{\frac{1}{2}}(q/kT) \tag{22}$$

The slopes of the ln I versus $V^{\frac{1}{2}}$ curves calculated assuming Schottky emission and Poole-Frenkel conduction are

$$B \sim 21 \text{ (volts)}^{-\frac{1}{2}} \text{ (Schottky)}$$

$$B \sim 43 \text{ (volts)}^{-\frac{1}{2}} \text{ (Poole-Frenkel).}$$

O'Dwyer (15), assuming an oxide with a distribution of shallow traps plus a deep trap level, has machine-calculated data which is in agreement with the results reported here.

For forward bias between 0.5 volts and about 2.0 volts, and for reverse bias from about -0.5 volts out to the reverse breakdown value, the dc current through the MOS devices is of the form

$$I \propto \exp\left(\frac{q}{kT\alpha} V\right) \tag{23}$$

where $\alpha \sim 100$. The measured slope of $\ln |I|$ versus V yields a value

$$q/kT\alpha \approx 0.4 \text{ (volts)}^{-1}. \tag{24}$$

This relationship is similar to the effect of space-charge build-up at high injection levels for p-i diodes where $\alpha = 2$. The current in this bias range is most likely limited by a similar space-charge build-up due to the filling of electron trap levels. An additional possibility which may account for the large value of α is the increased scattering due to ionized trap levels. The large scattering effect of large numbers of filled traps would tend to restrict the current build-up with increasing bias voltage.

At a forward voltage of about 2 volts, all the MOS samples exhibited a sharp increase in forward current and above this voltage the current was directly proportional to the voltage. This region of operation is believed due to the breakdown of the oxide layer which occurs for fields larger than about 10^6 volts/cm. If the total oxide layer thickness (deposited layer plus adsorbed layer) is assumed to be about 100 Å, then the field in the oxide will be close to the breakdown field at an applied voltage of 2 volts. However, it is also possible that this situation represents the region where injection over the metal-oxide interfacial barrier takes place with the current being limited only by the resistance of the oxide layer in series with the semiconductor. Hartman (3) reported a photoresponse threshold voltage

for the aluminum-evaporated SiO system of 1.8 volts which was interpreted as the Al-SiO barrier voltage. This is in agreement also with estimated values of the spacing between the bottom of the conduction band and the Fermi level in SiO (2 electron volts).

Under reverse bias all samples exhibited breakdown voltages in excess of 10 volts. This is attributed to the fact that, under reverse bias, the depletion region near the surface of the silicon is expanding and, consequently, the applied voltage is distributed over two regions of fairly high resistance: the oxide layer and the semiconductor depletion region. It is not clear which region is undergoing breakdown first at high reverse voltages because not enough is specified to determine the field distribution in the two sections. However, the rather large breakdown voltages observed are probably due to avalanche or Zener breakdown of the silicon depletion region.

No evidence of tunneling current was found in the results on the MOS devices tested. Although tunneling currents might have been expected by a cursory view of conduction through a 50 Å thick oxide film, a closer inspection shows that the effective barrier to tunneling currents will be increased by two factors over the barrier represented by the evaporated oxide. For one thing, the adsorbed oxide layer on the etched silicon surface must be added. In addition, space charge due to thermal ionization of trap sites located within the evaporated oxide layer will increase the effective tunneling barrier.

That large trapping densities are present in the MOS system is shown by the large charge storage effect in ac measurements. Traps in the oxide layers and on the surface of the silicon appear to be distributed throughout the forbidden band of the materials. The abrupt increase in current shown at forward voltages of about 2 volts coupled with the decrease in charge storage indicates that the trap levels extend virtually up to the conduction band in the insulator. The linear capacitance increase with bias at high frequencies is due to the capacitance variation with voltage of the semiconductor depletion region. This linear variation corresponds to a linear variation of depletion layer width with voltage as indicated by Zaininger in reference (9). It should be pointed out that this linear capacitance versus voltage effect would have little use in varactor circuits because of the slow bias change

requirement in order to maintain equilibrium with traps. However, it may be possible to eliminate the slow trapping times by the addition of phosporus or other material to the oxide. This has been found to be effective with grown silicon dioxide layers in reducing slow trap densities.

The saturation value of high frequency capacitance (about 3×10^{-9} farad) at large forward bias theoretically should give the equivalent parallel-plate capacitance of the oxide layer. However, a rough calculation of the oxide capacitance yields a value of 72×10^{-9} farad. The discrepancy can be accounted for by assuming that the depletion layer in the silicon is not reduced to zero width at high forward bias. Evidently, the capacitance, made up of oxide capacitance in series with depletion layer capacitance, increases with forward bias because of the decrease of depletion layer width. However, before the depletion layer is completely eliminated, the current flow through the device increases abruptly because of the filling of trap levels. This larger current, which could be thought of as being hole current injected into the depletion layer from the p-type silicon, causes the depletion layer width to remain fixed in the same fashion as occurs for forward bias in pn junction diodes.

At lower frequencies the charge storage in trap sites during capacitance measurements is much larger because the longer period of ac excitation allows more charge to be trapped during the charging half-cycle. The very long discharge time prevents most of this charge from being recovered during the discharge half-cycle. Thus, at low frequencies a space-charge is built up in the oxide layer. Because this space charge is due to electron trapping, the oxide charge becomes more negative. The effect of this space charge is to decrease the width of the depletion region in the semiconductor at forward bias levels. Therefore, at low frequencies the maximum capacitance at forward voltages should more nearly approach the theoretical oxide capacitance. This effect has been found in a number of MOS samples tested where the maximum low-frequency capacitance was about 45×10^{-9} farad which is of the same order as the theoretical oxide capacitance of 72×10^{-9} farad.

Additional theoretical work is needed to characterize the conduction process through insulators in the presence of large trap densities. At

the present time the origin of trapping levels in oxide layers is not definitely known. A series of experiments to determine the trapping energy levels and densities in evaporated oxide films, perhaps using optical or thermal trap quenching, would likely yield valuable data to improve the conduction process theory.

Although the measurements of current at temperatures lower than 300° K were not reliable enough to be used to specify the temperature dependence of the currents measured, the fact that the currents and, also, the charge storage effects, were considerably reduced at low temperatures agree with the general conclusion of trap-dominated conduction. Further measurements over a wide range of controlled temperatures should be useful in determining the complete volt-ampere relationships.

CONCLUSIONS

This work has been concerned with determing which of several possible charge transport mechanisms is dominant in controlling current flow through vacuum evaporated oxide films. A number of theoretical processes have been reviewed and the hypothesis of charge transport via electron trapping sites in the oxide has been proposed. Electrical measurements were performed on samples of MOS devices constructed by evaporating a thin film of silicon monoxide onto the surface of a slice of p-type silicon. The static volt-ampere characteristics obtained were found to be consistent with a model for the oxide consisting of a distribution of shallow trap sites along with one deep-lying trap level.

Further evidence of large concentrations of electron traps was indicated by the large charge storage hysteresis effect noted in ac volt-ampere measurements. The use of etched p-type silicon with the consequent formation of a surface depletion layer in the silicon was instrumental for the observation of the effects of trapped charge in the oxide on the high frequency differential capacitance of the MOS devices. Measurements of differential capacitance and conductance at high frequency with the bias voltage on the MOS devices rapidly switched on and off were used to determine the charge and discharge

time constants of the electron traps. Charge times of less than one minute and discharge times of one-half hour or more were observed.

It is believed that the results of this work will be useful in characterizing the conduction processes for a large class of dielectric materials and in improving the knowledge of electron transfer processes taking place on the surface of semiconductor devices.

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