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UNIVERSITY OF OKLAHOMA

GRADUATE COLLEGE

IV-VI SEMICONDUCTOR STRUCTURES FOR LASER FABRICATION ON SILICON

A Dissertation

SUBMITTED TO THE GRADUATE FACULTY

in partial fulfillment of the requirements for the

degree of

Doctor of Philosophy

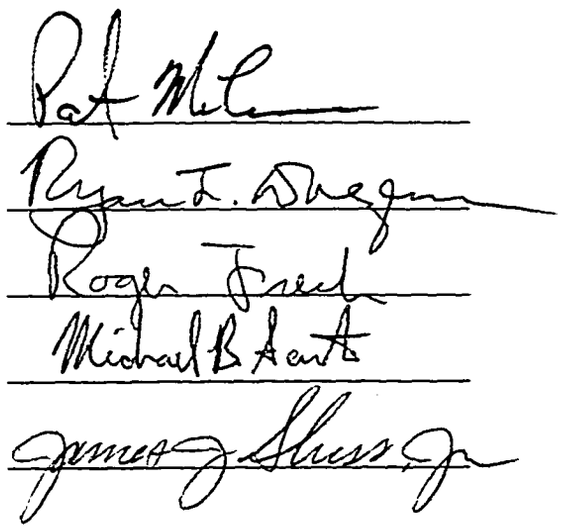
By

BRIAN NOEL STRECKER
Norman, Oklahoma
1998

IV-VI SEMICONDUCTOR STRUCTURES FOR
LASER FABRICATION ON SILICON

A Dissertation APPROVED FOR THE
SCHOOL OF ELECTRICAL AND COMPUTER ENGINEERING

BY



Acknowledgments

This work would not have been possible without the supervision and support of my advisor, Patrick McCann. While studying at the University, I have taken lectures from—or obtained assistance from—a number of other excellent faculty. Among them are the other members of my committee, whose names are listed two pages back. Not listed there is Matthew Johnson. His critical eye was greatly appreciated during preparation of the paper that eventually became chapter 5 of this text. A co-author of that paper, Robert Hauenstein, spent many hours acquiring—and explaining to me—the x-ray diffraction data presented therein. I would also like to mention Lynn Halverson, who made sure that my paperwork was kept up to date, and Marita Hardcastle, who made sure that my paycheck always showed up at the first of the month—both, very important jobs. For the first three years of my studies, the funding for these paychecks came from a GANNS fellowship provided by the U.S. Department of Education.

Among my peers are members of the Solid State Lab: Denton McAlister, I-Na Chao, Harpreet Sachar, Kevin Lewelling, Tathagata Chatterjee, and Xiao-Ming Fang. Xiao-Ming performed the MBE growths described throughout this project. Kevin pursued the epitaxial lift-off techniques and thermal modeling described in Chapter 1 and worked in parallel on the cleaving jig described in Appendix C. Harpreet has taken over LPE growth on silicon and has already extended this work by demonstrating aqueous liftoff of self-cleaved structures. Denton spent many hours assembling equipment, cleaning diffusion pumps, setting up furnaces, and the like. Tathagata... There are too many things to list here. Suffice it to say that some people are indispensable.

It is my family to which I dedicate this work. The people listed above have supported my efforts while at the University, but without the earlier efforts of my parents and grandparents—and the support of my wife—they would never have had the chance.

Lastly, I would like to express my appreciation to God, who at the beginning of my studies delivered the GANNS fellowship mentioned above and at the end of them, an article describing the integer quantum Hall effect. The fellowship arrived unexpectedly on the day of my wedding, when I was jobless and uncertain what to do. The article on the integer quantum Hall effect turned up in a popular magazine five minutes after I had re-read a section that mentions it in this dissertation and could not recall the mechanism. These are two of many pleasant coincidences which have occurred to me and which I attribute to Him.

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Abstract

Fabrication of commercially competitive IV-VI tunable diode lasers has been hampered by lack of suitable substrates. Lasers grown on IV-VI materials themselves are acceptable for low temperature operation, but poor substrate thermal conductivity limits their operation to the cryogenic regime. An alternative substrate material, BaF_2, is a promising alternative, but available substrates are often of questionable crystalline quality. High quality silicon, however, is readily available and may be used to grow epitaxial BaF_2. This BaF_2 epilayer may then be used as a substrate for further growth of IV-VI diode lasers. In addition, the water solubility of BaF_2 permits lift-off of the laser structures and remounting on a more electrically and thermally accommodating substrate—such as copper.

This dissertation describes experiments undertaken to develop techniques required to develop IV-VI lasers grown on silicon. A review of the IV-VI materials system, diode laser structures, recent IV-VI laser results, epitaxial growth techniques, and thermal modeling results introduces the reader to the structures and materials to be discussed. Designs for three different IV-VI laser structures on silicon follow. Three types of experimental structures are investigated next: those grown on BaF_2 substrates by liquid phase epitaxy (LPE), those grown on silicon by molecular phase epitaxy (MBE), and those grown on silicon by a combination of MBE and LPE. The author's recommendations for future work sum up the body of the text. Five appendices are included to document procedures (BaF_2 chemical mechanical polishing and IV-VI material preparation for LPE,), to provide supplementary material (cleaving jig

preparation for epitaxial lift-off of IV-VI layers and the effects of oxygen adsorption upon IV-VI materials), and to act as a repository for program code generated during this project (six programs and their supporting code for acquiring, displaying, and converting measurement data).

Chapter 1: Introduction

The aim of this project is to enable development of thermoelectrically cooled mid-infrared tunable diode lasers (TDL) through the use of new epitaxial growth techniques. Such lasers would reduce the cost and size of TDL spectrometers, greatly increasing existing spectrometer markets. However, the poor thermal conductivity of IV-VI substrates—used for fabricating presently available TDLs—is preventing realization of the necessary lasers. Silicon provides a promising alternative substrate: its thermal conductivity is much higher, it is available in larger sizes, it is less expensive, it has a higher structural quality, and it permits the application of epitaxial lift-off techniques.

This chapter begins with an overview of TDL spectroscopy and its potential applications. Discussions of the IV-VI materials family, common diode laser heterostructures, methods available for growing such structures, mechanisms for producing laser cavities, and expected improvements in TDL operating temperature follow. A set of laser structures leading to the realization of TDLs grown on silicon are proposed in Chapter 2. Fabrication and characterization of IV-VI layers grown on BaF_2(100) substrates by liquid phase epitaxy (LPE) are described in Chapter 3. Experiments designed to investigate current conduction through IV-VI single layers, IV-VI *p-n* junctions, and fluoride buffer layers grown by molecular beam epitaxy (MBE) on Si(111) substrates were performed. Chapter 4 describes these results. Growth of crack-free PbSe layers on Si(100) by LPE is described in Chapter 5 along with growth on Si(111). Chapter 6 concludes by summarizing the progress made during this project and recommending directions for future work.

1.1 Tunable diode laser spectroscopy

1.1.1 Overview

Tunable diode laser spectrometers were first developed in the early 1970's at MIT's Lincoln Laboratories [1] and then subsequently commercialized by Laser Analytics Inc., now Laser Photonics Inc. of Andover, MA. TDL spectrometers have also been independently developed by atmospheric chemists and other scientific research groups for specialized applications such as stratospheric trace gas measurements using high altitude balloons [2]. The key component in a TDL spectrometer is the tunable infrared laser used to excite molecular vibrations in a sample gas. Typically, an IR detector facing the tunable laser provides a signal proportional to the intensity of laser light transmitted through the sample gas, and the spectrum obtained by tuning the laser frequency yields a "fingerprint" of the gas sample. Absorption features associated with particular molecular ro-vibrational modes can be used in conjunction with gas standards to give quantitative concentration data for specific gases.

The small sizes of the essential components of a TDL spectrometer make this type of instrument suitable for miniaturization. This is in contrast to other infrared spectrometers such as Fourier transform infrared (FTIR) or grating spectrometers that require complicated electromechanical systems. The primary problem with mid-infrared lasers, those that emit in the 3 μm to 30 μm spectral range, is that they presently need to be cooled to cryogenic temperatures. Available TDL spectrometers are thus equipped with liquid nitrogen cryostats in which the lasers are mounted. In addition to adding significant bulk and weight to the instrument, the cryostat must be periodically refilled, imposing considerable inconvenience. Increasing mid-infrared laser operating

temperatures so that liquid nitrogen cryostats are not needed is thus the key to miniaturizing TDL spectrometers.

1.1.2 Medical applications for TDL spectroscopy

A potentially significant application for a miniature TDL spectrometer is as a breath testing instrument for non-invasive medical diagnosis. Breath testing has long been recognized as an important non-invasive diagnostic method that is particularly suitable for monitoring certain pathologies and metabolic flows [3]. By measuring the concentrations of particular molecular compounds in the exhaled breath of patients, a TDL spectrometer can provide quick results that can help diagnose and monitor various conditions. A wide variety of metabolic processes (e.g. protein turnover with labeled leucine), inborn errors of metabolism (e.g. amino acid acidemias) and exposure to volatile toxins (e.g. chlorinated hydrocarbons) are monitored using breath tests.

The high spectral resolution provided by the tunable laser source also enables the measurement of isotope ratios, a capability that allows use of non-radioactive isotopes to trace metabolic pathways. For example, measuring the $^{13}CO_2$ to $^{12}CO_2$ ratio in exhaled breath can give the rate of metabolism of a specific ^{13}C-tagged substance that has been administered to a patient. Recent research with liquid nitrogen cooled TDL spectrometers at NASA Ames Research Center [4] has shown that TDL spectrometers can determine $^{13}CO_2$:$^{12}CO_2$ isotope ratios by scanning the laser over closely spaced ro-vibrational spectral lines. An associated medical application would be a test for the *Helicobacter pylori* bacteria, the recently discovered cause of most gastrointestinal ulcers. These bacteria metabolize urea. So by feeding a patient ^{13}C-tagged urea and measuring the $^{13}CO_2$ to $^{12}CO_2$ ratio in exhaled breath, it will be possible to determine the presence of

an infection. By providing immediate results, this test will have a significant advantage over existing *H. pylori* tests such as isotope ratio mass spectrometry (IRMS) [5,6] that involve sending samples to a laboratory. Numerous variations on this ^{13}C tracing theme exist for medical diagnosis of conditions that cannot easily be monitored using other methods. Investigators have used breath tests to monitor NO, H_2O_2, $(CH_3)_2S$, and CO for a variety of clinically significant conditions [3,7-9]. All of these compounds could be potentially monitored with high specificity using the TDL spectrometer based upon the IV-VI laser being developed.

1.1.3 Scientific and Environmental Applications

A second application for TDL spectrometers is in atmospheric chemistry research. Gas molecules such as CO_2, CO, NO, CH_2O, NO_2, CH_4, SO_2, N_2O, HNO_3, NH_3, and ClO have strong absorption bands in the 6.0 μm to 7.5 μm spectral range, and measuring the concentrations of these gases is of great interest in studying global warming and ozone depletion. Accordingly, researchers at NASA have designed TDL spectrometers for both high altitude [2] and low altitude [10] data collection. In addition, researchers in Japan have used tunable diode lasers as local oscillators in a heterodyne TDL spectrometer that can take remote measurements of O_3 and N_2O in the earth's atmosphere [11]. One of the more advanced TDL spectrometers is the ATLAS instrument developed by Loewenstein et al. [12] at NASA Ames Research center. This instrument, which is routinely flown on the ER-2 at high altitudes over the South Pole, is very compact, roughly the size and weight of a desktop computer. Its primary limitation at this time is the short hold time of the small liquid nitrogen cryostat in which the laser is mounted. Use of higher operating temperature, TEC-cooled lasers would greatly extend the data collection time for this and

other TDL spectrometers used for atmospheric chemistry research. Passage of the 1990 Clean Air Act, which requires the EPA to regulate emissions of 189 listed toxic air pollutants, is already expanding the market for gas-sensing instruments. Presently, this market is served by FTIR systems, but the use of TDL spectrometers by atmospheric chemists has shown that these instruments could also be used to monitor trace gas concentrations of such pollutants.

1.1.4 Real-Time Process Control

In addition to monitoring vehicle emission, smokestacks, and fugitive emissions, gas measurement instrumentation can also be used to help optimize chemical processing conditions in order to reduce toxic gas emissions. In this case, TDL spectroscopy has a significant advantage over FTIR spectroscopy in that response times are much faster, allowing real-time process control. *In situ* measurements of gas phase reaction products in both chemical vapor deposition (CVD) [13] and reactive ion etching (RIE) [14] systems have been demonstrated using TDL spectrometers (the liquid nitrogen cooled type). Besides enabling the reduction of toxic gas emissions through process optimization, *in situ* monitoring offers significant benefits in the control of product quality. For example, research at the Stevens Institute of Technology [15] has shown that TDL spectrometers can be used in the semiconductor industry to control the etching of thin layers by monitoring reaction products emanating from underlying layers. This is a very sensitive end-point detection technique which can greatly increase the yields of integrated circuits as well as other products that involve etching steps (such as flat panel displays).

1.2 IV-VI materials system

The type of laser that is presently used in TDL spectrometers is composed of IV-VI semiconductor materials. Basic technology for IV-VI semiconductor laser fabrication was developed 30 years ago at MIT's Lincoln Laboratories, but since the mid-1970's there has been only a low level of intermittent research in this field. Efforts underway at the University of Oklahoma, such as this project, are an attempt to correct this oversight. The improved lasers expected from these efforts will have the same desirable characteristics of large tuning range and wide spectral coverage as existing IV-VI lasers, but with much higher operating temperatures.

Figure 1.1 is a bandgap versus lattice parameter plot showing the IV-VI semiconductor materials systems used for laser fabrication [16]. As can be seen, the quaternary $Pb_{1-x}Eu_xSe_{1-y}Te_y$ alloy system can cover the 3 μm to 6 μm range and the $Pb_{1-x}Sn_xSe_{1-y}Te_y$ system can cover the 6 μm to 30 μm range. Note that both of these quaternary alloy systems can be lattice matched with BaF_2. This feature will be discussed in more detail below. In addition to wide coverage of the IR spectrum, an important property of IV-VI semiconductors that makes them uniquely suited for spectroscopy applications is their large temperature tuning rate, which is more than an order of magnitude greater than any other known semiconductor material. Figure 1.2 shows bandgap data collected [17] for two IV-VI semiconductor alloys, $PbSe_{0.78}Te_{0.22}$ and $Pb_{0.95}Sn_{0.05}Se_{0.80}Te_{0.20}$.

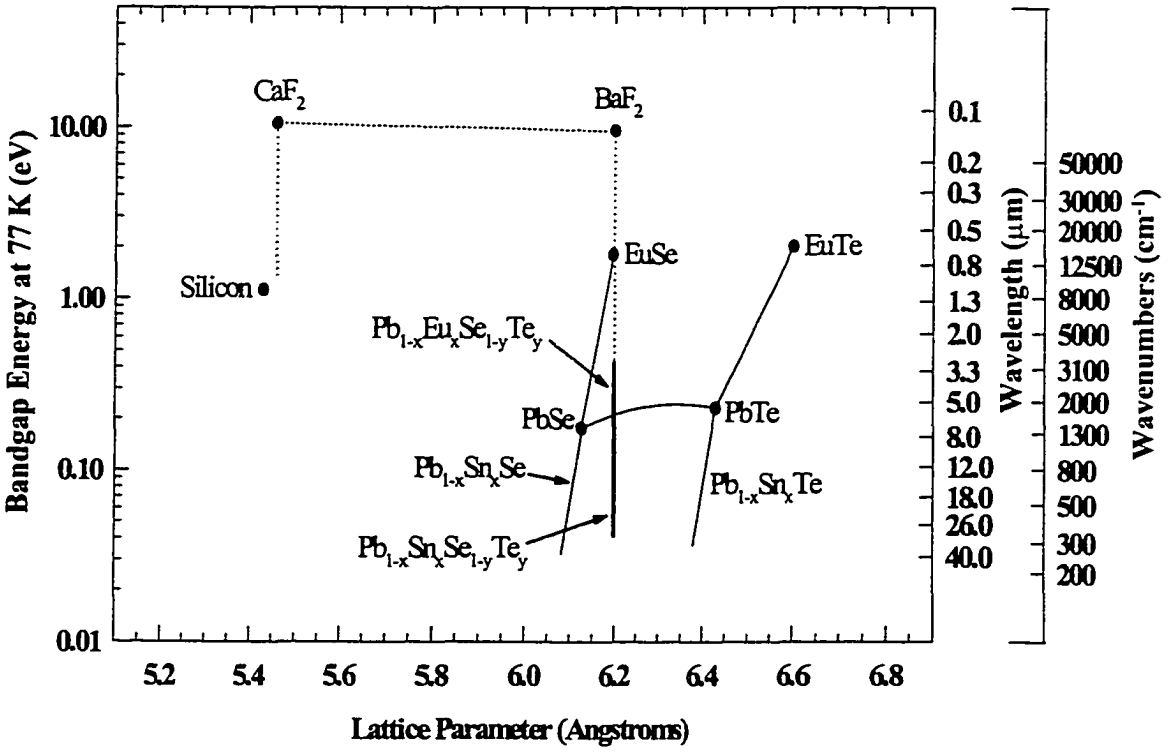

Figure 1.1: Bandgap energy versus lattice parameter for IV-VI semiconductor materials. $Pb_{1-x}Eu_xSe_{1-y}Te_y$ alloys lattice matched with BaF_2 can be grown by MBE while $Pb_{1-x}Sn_xSe_{1-y}Te_y$ alloys lattice matched with BaF_2 have already been grown by LPE [16]. Commercially available TDLs consist of IV-VI semiconductor alloys grown on PbTe or PbSe substrates.

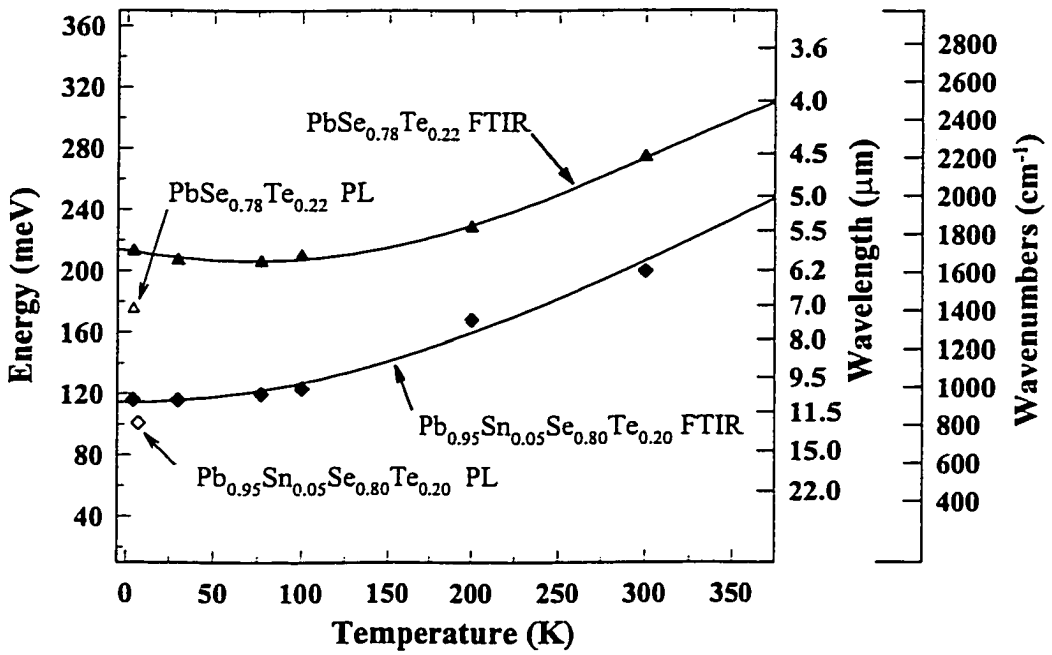

Figure 1.2: Fourier transform infrared (FTIR) absorption edge and photoluminescence (PL) energies versus temperature for $PbSe_{0.78}Te_{0.22}$ and $Pb_{0.95}Sn_{0.05}Se_{0.80}Te_{0.20}$ layers grown by LPE on BaF_2 substrates [17]. Increasing the tin content in the quaternary alloy shifts the bandgaps to lower energies. The differences between the PL and FTIR energies at low temperatures is believed to be caused by the Burstein-Moss effect [18].

Note that between 220 K and 300 K, a temperature range that can be controlled with thermoelectric coolers, the quaternary $Pb_{0.95}Sn_{0.05}Se_{0.80}Te_{0.20}$ alloy can cover the 6.0 μm to 7.5 μm spectral range, a sufficient range to detect all of the 11 molecules listed in section 1.1.3 above. This capability enables the design of TDL spectrometers that can detect multiple gaseous compounds by just controlling the heat sink temperature of the laser.

1.3 Diode laser structures

1.3.1 Homojunction diode lasers

The first injection lasers were made of GaAs and GaP_xAs_{1-x} homojunction diodes in 1962 by groups from General Electric (Syracuse [19] and Schenectady [20]), IBM [21], and the Lincoln Laboratory at MIT [22]. They consisted (except for [21]) of chips of GaAs or GaP_xAs_{1-x} which had two parallel ends polished to produce mirrors comprising a resonant cavity [23]. The p-n junction of the diode was produced prior to cutting and polishing by diffusion of a p-type dopant into the n-type substrate. By 1963, cleaving had been demonstrated as an alternative to polishing for producing laser mirrors [24]. The first IV-VI homojunction laser was produced in 1964 [25] from a diffused junction in PbTe.

Homostructure lasers are characterized by their high threshold current densities, which generate heat in the active region and limit operating temperatures. Typical room temperature theshold currents for homostructure GaAs lasers operating continuously are greater than 26 000 A/cm^2 [26]. Room temperature IV-VI lasers have not yet been developed, but the threshold density at highest pulsed temperature (150 K) for a homostructure device is comparable [27]. This current density may be expressed as

$$J_{th} = J_L + J_0 \frac{d}{\eta} + \frac{d}{\eta \Gamma \beta}\left[\alpha_i + \frac{1}{L}\ln\left(\frac{1}{R}\right)\right], \qquad (1\text{-}1)$$

where J_{th} is the threshold current density; d is the thickness of the active region; Γ is the confinement factor; and J_L, J_0, η, β, α_i, L, and R are independent of d and Γ [28] and will be discussed in Chapter 2. For a homojunction, d is controlled by the diffusion length of carriers (which for GaAs is 1-3 μm at RT [23]); reduction of d, by incorporating a barrier to carrier diffusion, decreases the threshold current. Likewise, the threshold can be decreased by increasing the confinement of light to the active region, as expressed by Γ. This is typically obtained by surrounding the active region by layers with a lower index of refraction. Addition of these improvements results in the double heterostructure laser.

1.3.2 Double heterostructure lasers

The double heterostructure laser was first proposed in 1963 [29] as a means of confining carriers to a thin active region and thereby reducing the threshold current density. However, it had to await development of $Al_xGa_{1-x}As$-on-GaAs LPE in 1967 [30,31] and the single heterostructure laser in 1969 [32-34] before being realized in 1970 [35-38].

A comparison of the homojunction and double heterostructures diodes is presented in Figure 1.3. The effect of the diffusion length of carriers upon the active region thickness in a homojunction diode can be seen in parts (a), (b), and (c) of the figure, which assumes a longer diffusion length for electrons than for holes. Gain is obtained in those regions of the device with a sufficient population of electrons and holes, a condition known as population inversion. In Figure 1.3(a), this region can be seen to extend from the junction toward increasing x. The rightmost boundary for the active region is not well

defined; as the junction current is increased, the boundary between inverted and non-inverted regions will move toward the right.

These variations in carrier concentrations, in turn, affect the refractive index of the material; the resulting uncertainty in the location of the rightmost region of gain is indicated by a dashed line in the refractive index plot of Figure 1.3(b). The change in refractive index arising from increased carrier concentrations is usually quite small as is the resulting optical confinement of photons originating in the active region. Large optical losses result, as represented by the unshaded regions under the curve in Figure 1.3(c). In addition, the photon density in the active region is decreased, reducing the probability of radiative recombination of electron-hole pairs.

By sandwiching a thin active region between two larger bandgap materials, electrons and holes are confined, resulting in higher carrier concentrations for a given current density. The extent of the active region is thus determined by the thickness of the smaller bandgap material and can be made much thinner than the diffusion length of the carriers. This structure also increases optical confinement of light generated in the active region due to the lower refractive indices associated with the larger-gap materials. As discussed in section 1.3.1, reducing the active region thickness or increasing the confinement of light decreases the threshold current for lasing. However, the reduction in active area thickness also lowers the maximum output power of the device.

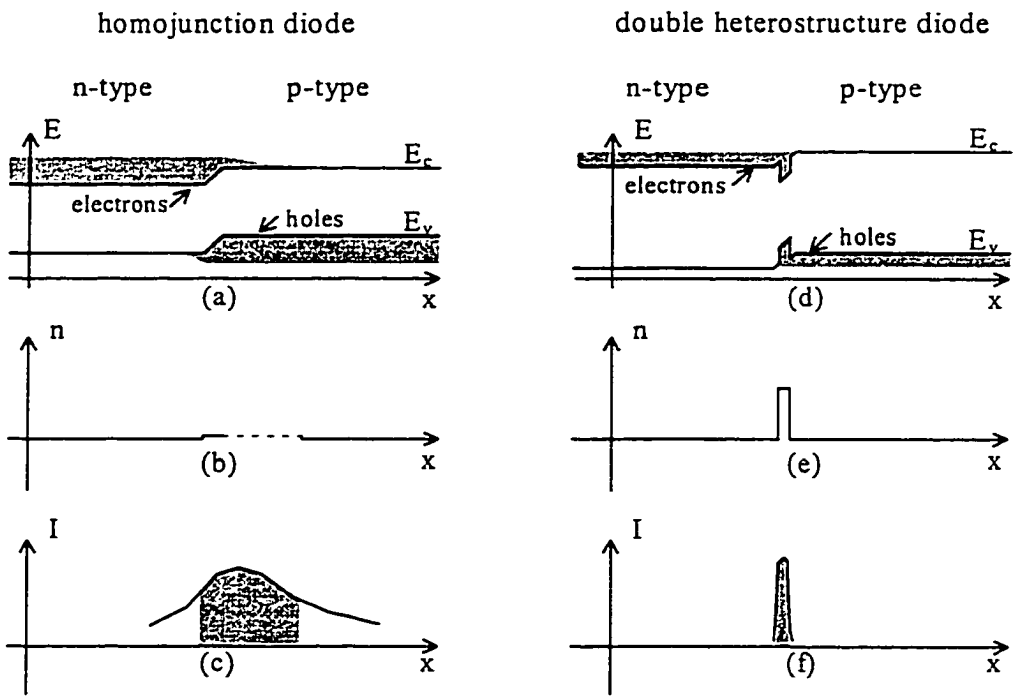

Figure 1.3: Energy band and carrier density (E), refractive index (n), and light intensity (I) versus distance perpendicular to the plane of the p-n junction for a homojunction (a, b, and c) and a double heterostructure (d, e, and f) diode. The greater confinement of carriers and larger step in refractive index exhibited by the DH structure results in increased confinement of light to the active region and a lower threshold current.

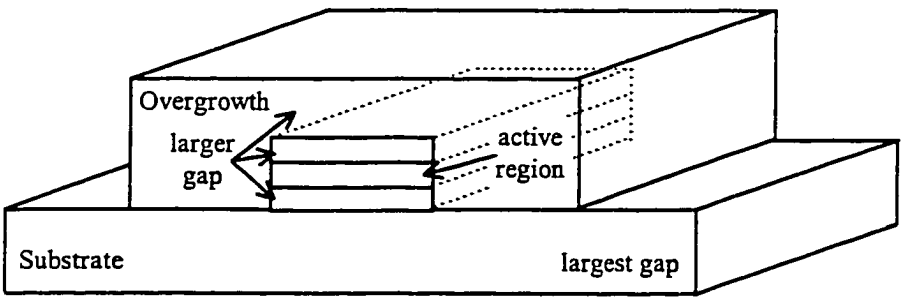

Figure 1.4: Schematic of a buried heterostructure (BH) diode laser. A three layer double heterostructure is grown on a substrate and then etched to produce a stripe. Overgrowth of the resulting stripe provides optical confinement in the horizontal direction. Confinement in the vertical direction is provided by the larger-gap layers above and below the active region, as in the DH laser. The front and back planes of the structure act as mirrors, forming a resonant cavity.

Additional optical confinement can be obtained by surrounding the active region with larger-gap materials on four sides instead of two. This is done by etching through the active layer and regrowing with larger-gap materials, resulting in the buried heterostructure (BH) shown in Figure 1.4. Unfortunately, the etch and regrowth steps increase the difficulty of processing and are not currently feasible in our facilities. For this reason, growth of the homojunction and DH structures was pursued.

1.3.3 Survey of recent results

In 1983, Partin [39] at General Motors Research Laboratory reported the first fabrication of mid-infrared lasers that utilized $Pb_{1-x}Eu_xSe_{1-y}Te_y$ alloys grown by molecular beam epitaxy (MBE). These double heterostructure (DH) lasers, which were grown on PbTe substrates, had a maximum cw operating temperature of 147 K. In 1991, Feit et al. [40] at Laser Photonics, using the same materials technology developed by Partin, reported on the fabrication of a buried heterostructure (BH) $Pb_{1-x}Eu_xSe_{1-y}Te_y$ mid-infrared laser, 4.2 μm to 6.4 μm, with a maximum cw operating temperature of 203 K. In 1996, the same group reported the fabrication of a separate confinement BH laser with a cw operating temperature of 223 K [41]. This operating temperature is much higher than any other cw mid-infrared semiconductor laser and is almost high enough for useful TEC operation. These recent advances, especially the development of single-mode BH lasers, have enhanced the capabilities of TDL spectrometers to the point that sophisticated IR spectroscopy techniques such as isotope ratio measurements are now possible [4]. Unfortunately, these lasers still require liquid nitrogen cooling. Solid state thermoelectric refrigerators (Melcor, Inc.) offer a much more convenient way to cool the lasers, but

maximum TDL operating temperatures must be increased to at least 240 K—and even higher for temperature tuning capability—before such refrigerators can be used.

Recently, Springholtz et al. [42] have grown $Pb_{1-x}Eu_xTe/PbTe$ quantum well structures on BaF_2 substrates of sufficient quality to observe the integer quantum Hall effect for the first time in IV-VI semiconductors. Their growth technique involved use of a 3 μm thick $Pb_{1-x}Eu_xTe$ buffer layer between the quantum well structure and the BaF_2 substrate. This buffer layer enabled high structural perfection in spite of the 4.2% lattice mismatch between PbTe and BaF_2. Additionally, considerable work by Zogg et al. [43-47] has shown that high quality IV-VI semiconductor detector structures can be grown on BaF_2-coated silicon substrates. Based on these results, it should be possible to fabricate $Pb_{1-x}Eu_xSe_{1-y}Te_y$ mid-infrared and $Pb_{1-x}Sn_xSe_{1-y}Te_y$ far-infrared laser structures, see Figures 1.1 and 1.5, on BaF_2-coated silicon substrates. Such growth enables use of a new laser fabrication method that is not presently possible with existing PbTe substrate technology.

This new method, which is similar to recently developed epitaxial lift-off procedures used to fabricate III-V semiconductor near-IR lasers, increases active region heat dissipation by a sufficient amount to raise maximum TDL operating temperatures by at least 50 degrees. Since this places TDL operating temperatures well within the thermoelectric cooling range, this improvement will be the quantum jump necessary to allow widespread application and commercialization of TDL spectrometers.

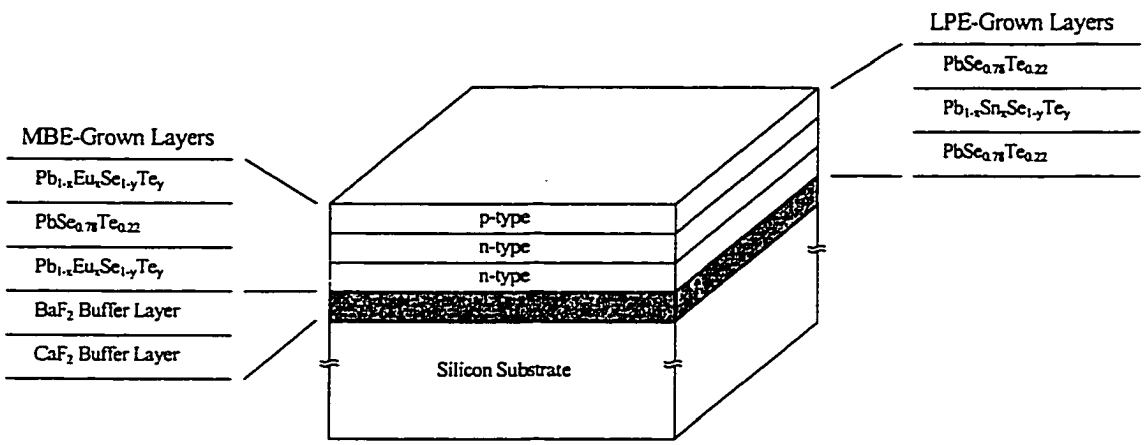

Figure 1.5: Lattice matched double heterostructure (DH) laser structure grown on a silicon substrate by either molecular beam epitaxy (MBE) or liquid phase epitaxy (LPE).

1.4 Available growth methods

The most important methods for growing diode lasers are molecular beam epitaxy (MBE), liquid phase epitaxy (LPE), and organometallic vapor-phase epitaxy (OMVPE) [48]. The University of Oklahoma currently has facilities for growing IV-VI materials by the MBE and LPE techniques. If it can be used, OMVPE provides several advantages for industrial production, such as high throughput and uniformity. However, the toxic gases and associated gas-handling equipment reduce its attractiveness in an academic environment.

1.4.1 Molecular beam epitaxy

Growth by MBE takes place under ultra high vacuum (UHV) conditions, typically 10^{-10} torr [49]. Generation of this vacuum greatly increases the cost of an MBE system and presents technical difficulties to the introduction and manipulation of substrates. However, such low pressures are required to produce the long molecular mean-free-path lengths needed for material transport between the solid source and substrate. Figure 1.6 is a schematic of a typical MBE growth chamber. The three effusion cells contain different solids which are heated to accelerate evaporation. Less commonly, gas sources are used, resulting in gas-source MBE. Due to the long mean free path, the molecules leaving the effusion cell travel as a beam. Dependence of this beam flux upon cell temperature is determined with the aid of an ionization gauge (not shown) mounted on the back side of the substrate holder.

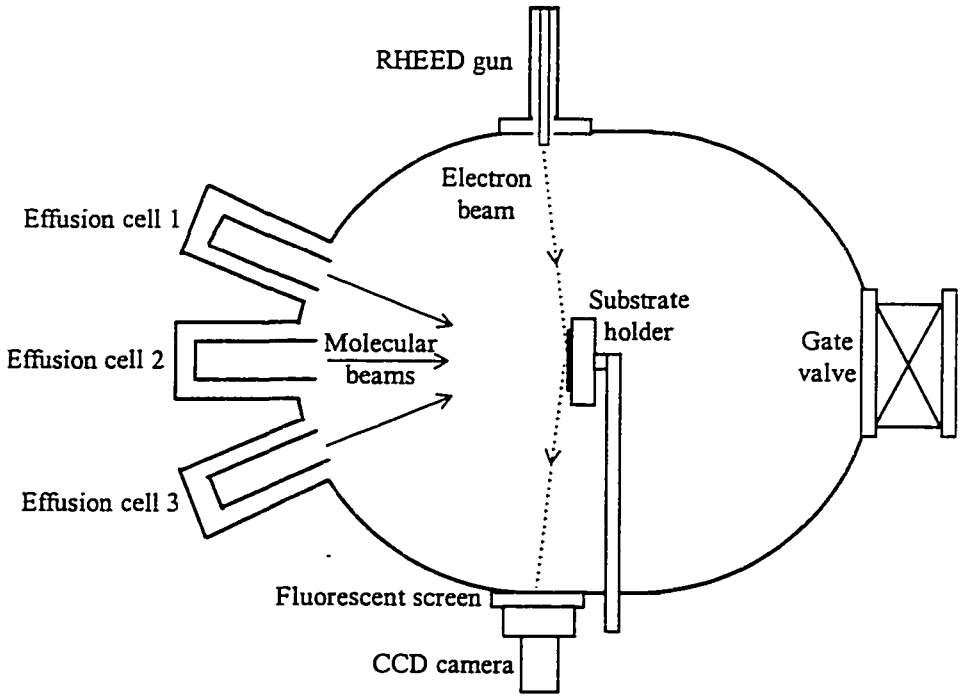

Figure 1.6: Schematic of a three source MBE system. Ion gauges, effusion cell shutters, and cryogenic shielding are not shown. Temperature of the effusion cell is controlled by resistive heaters. The cells are isolated from each other by alcohol/water cooled shields to prevent unwanted thermal crosstalk. Substrate temperature is controlled by a resistive element in the substrate holder. The gate valve allows transfer between the growth chamber and a load/lock or transfer tube.

Rotating the substrate holder toward the sample-transfer gate valve brings the gauge into the molecular beam. This same substrate holder position is required for substrate transfer. For sample growth, the substrate holder is rotated back into the position shown and the shutters (not shown) covering the effusion cells are opened and closed to turn on and off the molecular beams. The migration of molecules across the surface of the substrate is controlled by the substrate temperature and the molecular rate of arrival. This greatly affects the morphology and electrical characteristics of the resultant layers. The low arrival rate of material results in slower growth (1 μm/hr is typical [49]) than either MOVPE or LPE but allows deposition of very thin epitaxial layers and production of complex multilayer structures. These layers can also be easily monitored during growth by using UHV dependent analytical techniques, such as reflection high-energy electron diffraction (RHEED), which are not available for other growth techniques.

1.4.2 Liquid phase epitaxy

Layers of epitaxial material may also be grown from a supersaturated liquid solution using LPE. One common technique employs a horizontal graphite boat placed within an oven [50]. Small wells in the boat are filled with carefully prepared quantities of solvent and solute prior to loading in the oven. A schematic of a graphite boat used to grow the epitaxial layers is shown in Figure 1.7. The four wells, which are each approximately 1 cm^3 in volume, allow multilayer growth. Once loaded with melt materials and a substrate, this boat is placed inside an oven, which is evacuated and then backfilled with hydrogen gas. The temperature of the oven is then raised to dissolve the solute and homogenize the melt. When the temperature of the system is slowly lowered again, the substrate and melt are brought into contact by moving the slider. This is done just above

the nucleation temperature of the melt being used for growth. As the solution cools through its nucleation point, precipitates form on its surfaces. If the substrate is compatible and the growth conditions are proper, precipitation at the substrate/melt interface occurs as epitaxial growth.

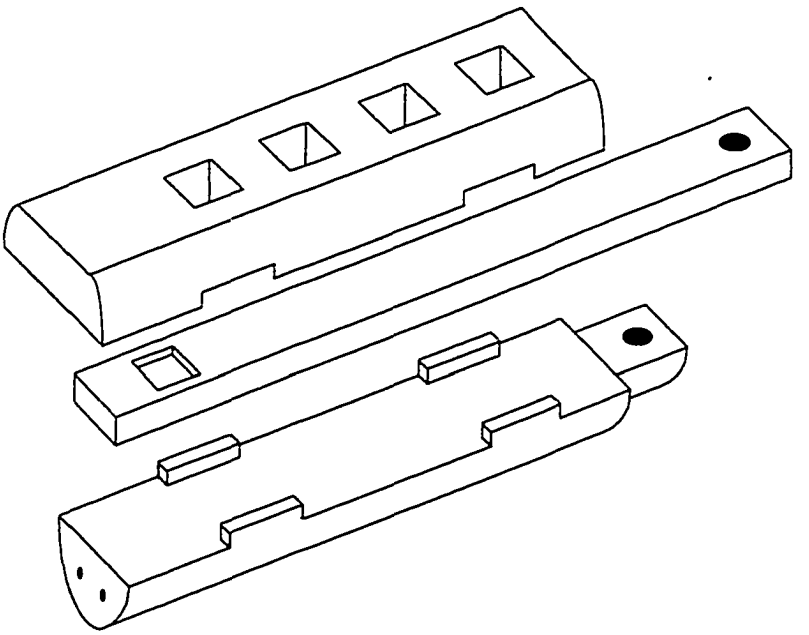

Figure 1.7: Isometric drawing of a graphite boat used in the growth of layers by LPE. The boat separates into three sections. Wells in the top section contain melt solutions from which the layers are grown. The middle section is the slider. A substrate is held in the shallow well toward the left end of the slider. As the slider is pulled to the right, the substrate comes into contact with each of the melts. The bottom section supports the slider and top section and holds them in place with the aid of the tabs and matching notches shown.

1.5 Laser cavity fabrication

Laser structure growth, though critically important, is only part of the TDL fabrication procedure. An optical cavity needs to be formed so that stimulated emission and lasing action can be achieved. This is usually accomplished by cleaving the entire laser/substrate assembly with a razor blade to form parallel facets which function as laser cavity mirrors. Laser structure growth on BaF_2, however, offers alternatives to this approach. Such a new approach is presently being developed at the University of Oklahoma. This new laser fabrication method involves use of a cleaving jig which consists of thin copper plates that are held together mechanically. This jig is bonded to the top epitaxial layer using a metallic bonding medium such as the silver/indium eutectic compound. With such a top-side support, the water-soluble BaF_2 can be completely removed leaving just the semiconductor laser structure bonded to the edges of the thin metallic plates. Mechanical support is then removed to cleave the laser structure forming Fabry-Perot optical cavities, the length of which are determined by the thickness of the metallic plates. This patented [51] laser fabrication procedure is outlined in Figure 1.8.

Such laser processing is not as radical as it may appear. Yablonovitch et al. [52] have shown that AlGaAs/GaAs/AlGaAs DH laser structures can be removed from a GaAs substrate by using a 500 Å thick AlAs selectively etchable release layer interposed between the laser structure and the substrate. This epitaxial lift-off (ELO) process, developed to enable hybrid device packaging, was shown not to degrade the performance of the laser device. An important aspect of this new laser fabrication technique is that the resulting laser device consists of the epitaxial layer structure only. This structure can be sandwiched between two thermally conductive materials such as copper, enabling a

dramatic increase in laser operating temperatures, as discussed in section 1.4. The success of these steps can be seen in Figure 1.9, which is a scanning electron micrograph (SEM) of cleaved epitaxial layer. The results shown here establish the proof of concept for this new laser fabrication method.

It should be pointed out that this bonding procedure is very similar to one that is used in the flip-chip packaging process that is commonly used in the semiconductor industry [53]; obtaining a good bond between the copper and the epilayer is not a fundamental problem.

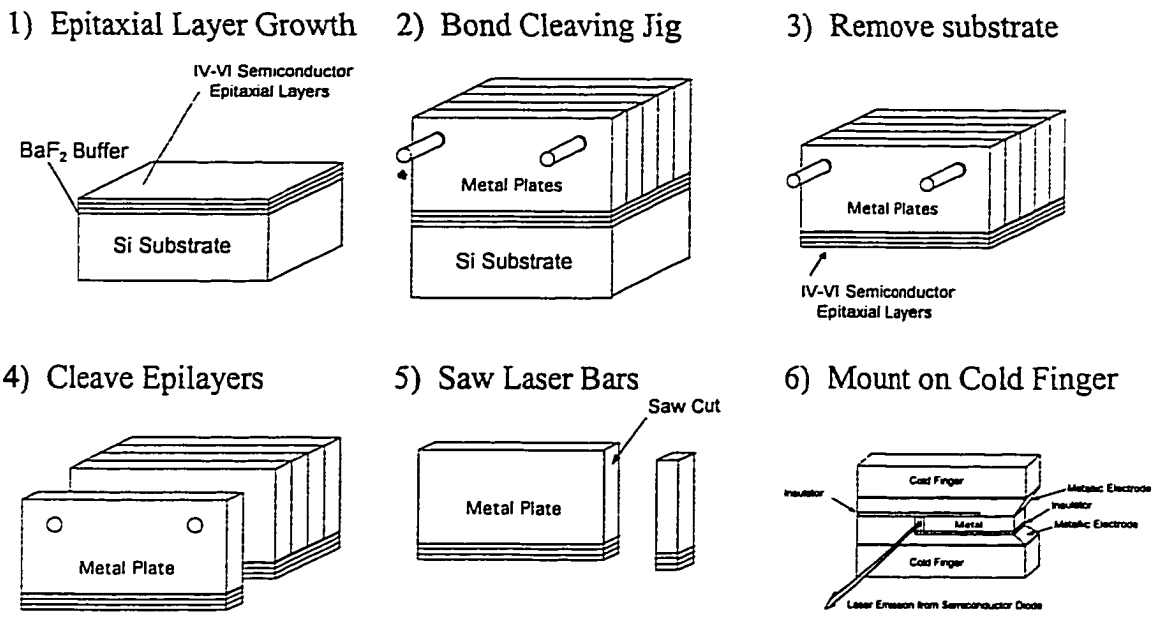

Figure 1.8: Fabrication procedure for IV-VI semiconductor laser structures grown on Si substrates: (1) grow epitaxial layers, (2) bond cleaving jig to epitaxial layers, (3) remove Si substrate by selectively etching BaF_2 buffer, (4) cleave IV-VI semiconductor layers, (5) saw cut individual laser bars, and (6) mount laser on cold finger. (These figures are not drawn to scale.) To enhance heat dissipation, the insulator identified in step 6 could be a thin plate of high thermal conductivity chemically vapor deposited (CVD) diamond [54]. The device structure shown in step 6 is patented [51].

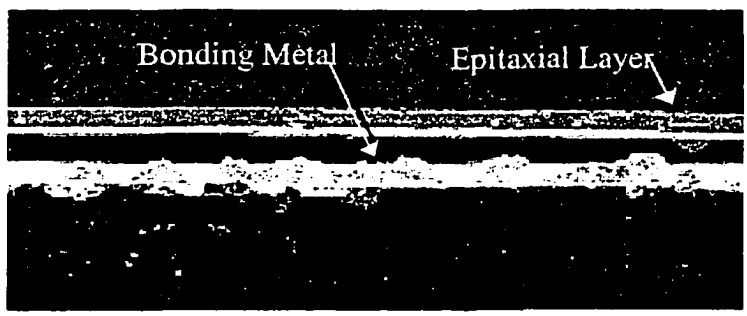

Figure 1.9: Scanning electron micrograph (SEM) of a $PbSe_{0.78}Te_{0.22}$ epitaxial layer lifted off and cleaved using the techniques outlined in Figure 1.8. This cleave actually extends several hundred microns beyond what is seen in this SEM. The ~15 μm gap between the PbSn bonding metal and the epilayer is a problem that is presently being worked on.

1.6 Thermal Modeling

All previous IV-VI semiconductor lasers have been packaged on copper heat sinks with a relatively thick (~200 μm) PbTe or PbSe substrate still attached to the device structure. Active region heat, generated by the large pumping currents, is thus effectively removed from only one side of the device since PbTe and PbSe are less than 0.5% as thermally conductive as copper. This implies that there is considerable room for improving active region heat dissipation in IV-VI semiconductor lasers.

By eliminating the substrate entirely and placing a second heat sink within microns of the active region—allowed by growing the device on silicon and using the new laser fabrication method just described—heat dissipation is effectively doubled. Finite element thermal modeling results [55], see Figures 1.10 and 1.11, show that under the same output power conditions the active region temperature is 50 degrees cooler when this second copper heat sink is used.

This result is consistent with the work of Rosman et al. [56] who explain the large difference between pulsed and cw operating temperatures in terms of active region heat accumulation. Use of the new laser fabrication procedure described here should increase maximum cw operating temperatures by 50 degrees, placing TDL operating temperatures well within the thermoelectric cooling range. For example, thermoelectric cooling between 220 K and 250 K of a laser composed of the materials shown in Figure 1 will have a tuning range between 7.5 μm and 6.8 μm. Use of different active region alloys will allow coverage of other regions of the infrared spectrum. Other anticipated improvements resulting from better active region heat dissipation include faster tuning

rates, improved mode stability, higher reliability, and the ability to fabricate high power laser arrays.

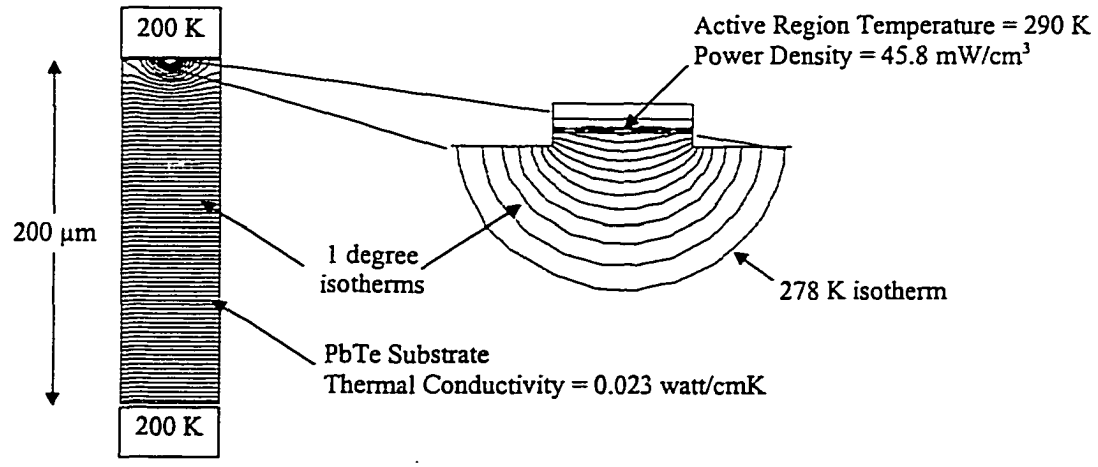

Figure 1.10: Finite element modeling results for lasers on PbTe. Low PbTe thermal conductivity, 0.023 W/cm K, causes high active region temperatures. Poor active region heat dissipation is responsible for the large difference, as much as 100 degrees, between cw and pulsed maximum operating temperatures.

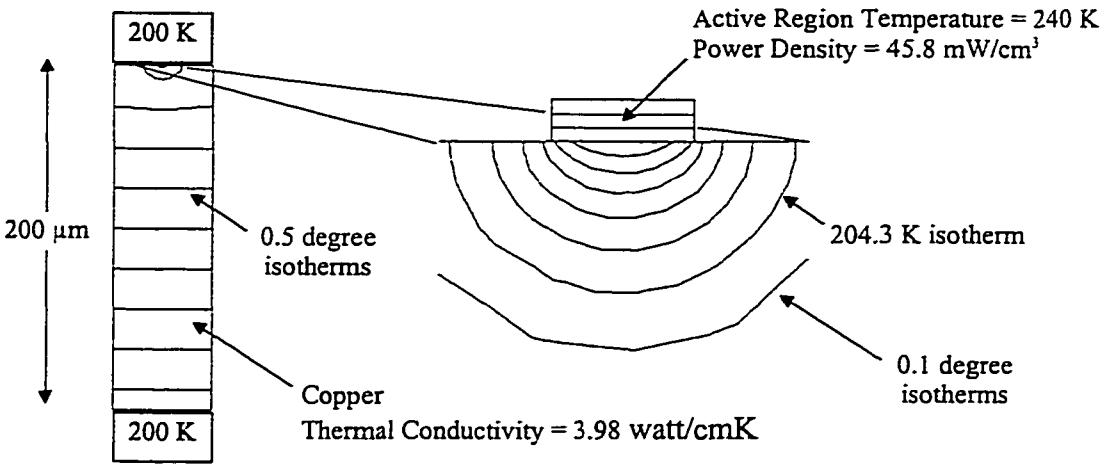

Figure 1.11: Finite element modeling results for a TDL fabricated using the new methods outlined in Figure 1.8. Replacing PbTe with copper, which has a thermal conductivity of 3.98 W/cm K, reduces active region temperatures by 50 degrees. Heat sink temperatures can be raised by this amount thus allowing thermoelectric cooling.

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Chapter 2: Proposed Laser Structures

Due to uncertainties associated with developing new growth and processing techniques, the success of a particular approach to producing tunable IV-VI diode lasers on silicon should not be taken for granted. To increase the probability of obtaining an operational laser, three structures are proposed: an LPE-grown double heterostructure (DH) on (100)-oriented silicon, an MBE-grown DH on (100)-oriented silicon, and an MBE-grown vertical-cavity surface-emitting laser (VCSEL) on (111)-oriented silicon. Each of the structures — at the expense of uncertainty introduced by including untested procedures — addresses a particular device processing concern which might inhibit laser cavity formation.

The LPE-grown DH on (100)-oriented silicon is the closest to realization; similar structures have been grown in the Solid State Laboratory at the University of Oklahoma by the author and others [1] on BaF_2 substrates, and the LPE growth of crack-free PbSe (the first layer of the proposed DH) on (100)-oriented silicon has been demonstrated [2].

Use of molecular beam epitaxy allows the addition of europium to the active region of the MBE-grown DH on (100)-oriented silicon. This increases the bandgap of the active region, so that shorter wavelength lasers can be produced. Substitution of the MBE technique for LPE also allows for greater active region thickness control (which may be needed to lower the threshold current for the device) and avoids the scalloped surfaces typical of horizontal furnace LPE.

A final structure, the VCSEL on (111)-oriented silicon, eliminates the problem of polishing or etching mirrors by incorporating Bragg reflectors. This necessitates a vertical cavity arrangement. The structure proposed precludes electrical pumping through

the substrate, but redesign—using a more complicated Bragg reflector or sophisticated photolithography and metallization—would alleviate this limitation.

2.1 Double heterostructures (DH)

Before developing the proposed DH laser structures, one must consider the DH structure and IV-VI materials system more carefully than presented in the overview of Chapter 1. General equations, extracted from the literature, relating the active region thickness, confinement factor, lasing wavelength, and threshold current aid in determining the thickness and composition of the active region. The generation and effect of defects in the active layer are also discussed, providing guidelines for selecting materials composition and growth procedures.

2.1.1 Effect of active region thickness upon lasing threshold

As mentioned in Chapter 1, it is desirable to limit the threshold current for the laser so that active region heating is minimized. The threshold current density for lasing was given by equation (1-1) for a homojunction laser. An equivalent equation for a DH laser may be expressed as [4]

$$J_{th} = J_0 \frac{d}{\eta} + \frac{d}{\eta \Gamma \beta}\left[\alpha_i + \frac{1}{L}\ln\left(\frac{1}{R}\right)\right], \qquad (2\text{-}1)$$

where J_{th} is the threshold current density; J_0 is the current density required to obtain a g_{max} (described next sentence) of zero at d = 1 μm and $\eta = 1$, d is the thickness of the active region, η is the internal quantum efficiency, Γ is the confinement factor, β is the gain constant, α_i represents the internal losses, L is the cavity length, and R is the reflectivity of the mirrors. The gain of the active region is a function of the energy of the photons amplified, so that lasing occurs first at $g_{max} = \max_{PhotonEnergy}[\text{gain}(PhotonEnergy)]$.

Minimization of active region heating requires that d and Γ be balanced to minimize the threshold current.

Approximating the DH active region and its adjacent layers as a three-layer, symmetric, lossless, planar dielectric waveguide and applying ray-optics provides the condition [5]

$$M = 2\frac{d}{\lambda_0}\left(n_1^2 - n_2^2\right)^{\frac{1}{2}} \tag{2-2}$$

where M is the number of modes supported, n_1 and n_2 are the active and surrounding layer refractive indices, and λ_0 is the free-space wavelength of the confined light. By setting M to one and substituting the appropriate material parameters, the maximum thickness of the active region for single mode operation is obtained. Since the zero-order mode is the most confined mode in a waveguide [5], elimination of the less confined higher orders results in a higher Γ. A lower limit to the active region thickness is set by

$$d = \frac{\lambda_0}{2n_1}, \tag{2-3}$$

which is the point at which diffraction losses begin to become significant [6].

2.1.2 Effect of lattice matching upon lasing threshold

Following the example of the III-V system, early workers growing IV-VI TDLs moved to DH lasers in an attempt to lower threshold currents and raise maximum operating temperatures [7]. As expected, operating temperatures increased, allowing continuous wave operation above 77 K [8-12], but low temperature threshold currents increased as well [13]. This increase in threshold current has been attributed to misfit dislocations in the active region due to lattice mismatch [13]. Etch pit studies of the

interface of nearly lattice-matched PbSnTe layers grown by LPE [14] indicate that a mismatch of as little as 2 x 10^{-4} between epilayer and substrate is sufficient to generate defects at the interface. These defects migrate through the epilayer during growth—even in the case of a 50 μm thick layer [14]—and act as recombination centers. Reduction of the internal quantum efficiency by 80 % has been reported due to these centers in LPE-grown 2 μm thick $Pb_{0.85}Sn_{0.15}Te$-between-PbTe (a mismatch of about 30 x 10^{-4} [15]) [16]. Equation (2-1) indicates that a sharp increase in threshold current can be expected in the case of such a lattice-mismatched structure. DH structures should be matched to the PbSe lattice parameter when feasible.

2.1.3 LPE-grown DH PbSe/$Pb_{1-x}Sn_xSe_{1-y}Te_y$/PbSe on (100)-oriented Si

Design of the PbSe/$Pb_{1-x}Sn_xSe_{1-y}Te_y$/PbSe double heterostructure begins by determining the active region composition and limits for its thickness. Active region composition sets the lasing wavelength and the refractive index used in (2-2). Optical confinement argues for a large difference, but this can only be obtained at the expense of a smaller bandgap. At the higher operating temperatures expected for these structures, a smaller bandgap implies large thermal populations in the bands. This makes inversion more difficult [6] and increases non-radiative Auger recombination[17].

Two of the parameters required in equation (2-2) for determining the active region thickness are the refractive indices of the active and confinement layers. Although the refractive index for PbSe is known as a function of wavelength [18], no such data are available for the quaternary $Pb_{1-x}Sn_xSe_{1-y}Te_y$ [19]. An estimate of the refractive index based upon the empirical relation [20],

$$n^4 E_g = constant, \tag{2-4}$$

is used for obtaining the maximal thickness of the active region for single mode operation. Taking the refractive index for PbSe of 4.94 at its bandgap energy (E_g = 0.27 eV at 300 K) and deflating by the percent reduction in the square root of the PbSe low-frequency permittivity between 300 K and 77 K (4.97 %) [21], results in an refractive index estimate for PbSe of 4.69 (E_g = 0.175 eV at 77 K, λ = 7.1 μm). Using (2-4) and the 77 K estimate for n_{PbSe} and E_g results in a value of 84.7 for the *constant*, and an estimate of 4.83 for the refractive index of $Pb_{1-x}Sn_xSe_{1-y}Te_y$ (E_g = 0.155 eV at 77 K, λ = 8.0 μm). These 77 K indices of refraction, the 8.0 μm active region lasing wavelength, and (2-2) indicate an upper limit of 3.5 μm for the active layer thickness. The lower limit, from (2-3), is then 0.82 μm.

Choice of an active layer thickness is also affected by the expected minority-carrier diffusion length. As the diffusion length decreases, the distribution of minority carriers across the active region deviates from a constant value [6]. This results in lower carrier concentrations—and lower gain—away from the injection junction, distorting the distribution of light in the cavity and negating the electrical confinement effects of the other heterojunction. It is therefore preferable to make the active region thickness smaller than the diffusion length of the carriers, so that the entire active region is sufficiently pumped and does not contain absorptive regions. Measurements of minority carrier diffusion length in LPE-grown *p*-type $Pb_{0.8}Sn_{0.2}Te$ indicate that it is a strong function of temperature and epilayer growth conditions; it varied from more than 14 μm to approximately 10 μm over the range 10-100 K for a sample grown near 500 °C, but remained near 1 μm over this range for a sample grown near 600 K [22]. At temperatures

above 100 K, Auger recombination is expected to become the predominant mechanism for non-radiative recombination, further limiting the diffusion length [22]. Investigation of the effect of In-doping of PbTe and $Pb_{0.8}Sn_{0.2}Te$ layers concluded that minority carrier diffusion lengths drop by at least an order of magnitude in both materials [22]—from > 10 μm to < 1 μm for PbTe doped at 0.135 at. % in the melt and from > 1 μm to < 0.1 μm for $Pb_{0.8}Sn_{0.2}Te$ doped at 0.1 at. % in the melt. With a diffraction-imposed lower limit of 0.84 μm on the active layer thickness and an estimated 1 to 10 μm minority carrier diffusion length, an undoped active layer with a thickness of 1 μm is a good design target.

Although equations (2-2) through (2-4) allow optical confinement to be considered while designing the double heterostructure, they provide no consideration for carrier confinement. A band diagram of the proposed structure may be constructed—based upon the bandgap energies for the selected active and confinement layers—to verify carrier confinement for the structure. In the procedure adopted [36], the first step is to determine the energy steps, ΔE_c and ΔE_v, of the conduction and valence band discontinuities at each junction, using the fact that $\Delta E_g = \Delta E_c + \Delta E_v$ [36] and assuming that—as in PbTe/PbEuTe structures [37, 38]—$\Delta E_c = \Delta E_v$. The location of the Fermi level in each layer is estimated by assuming an electron or hole concentration of 6×10^{17} cm^{-3} and using the equations developed in reference [39] and presented in reference [6] for $Pb_{0.82}Sn_{0.18}Te$ at 77 K. At equilibrium, the Fermi level through the device will be constant and the bands will align as shown in Figure 2.1. Band discontinuities at the junctions are maintained.

Under applied forward bias, the barrier to hole injection at the right junction decreases; the hole barrier at the left junction remains stable, at approximately 20 meV, due to the degeneracy of the two *n*-type regions. Since the barrier to hole injection into the active region is about 20 meV lower than that for electron injection into the *p*-type cladding layer, current is expected to be carried primarily by holes, which pump the active region. The expected 20 meV barriers to holes and electrons should be sufficient for confining carriers to the active region. A measure of the effectiveness of the barrier may be obtained by comparing the barrier heights (20 meV) to 3kT (6.6 meV at 77 K)—which is used here as a surrogate for the thermal energy available to the carriers for jumping the barriers. This measure indicates acceptable carrier confinement to the active region.

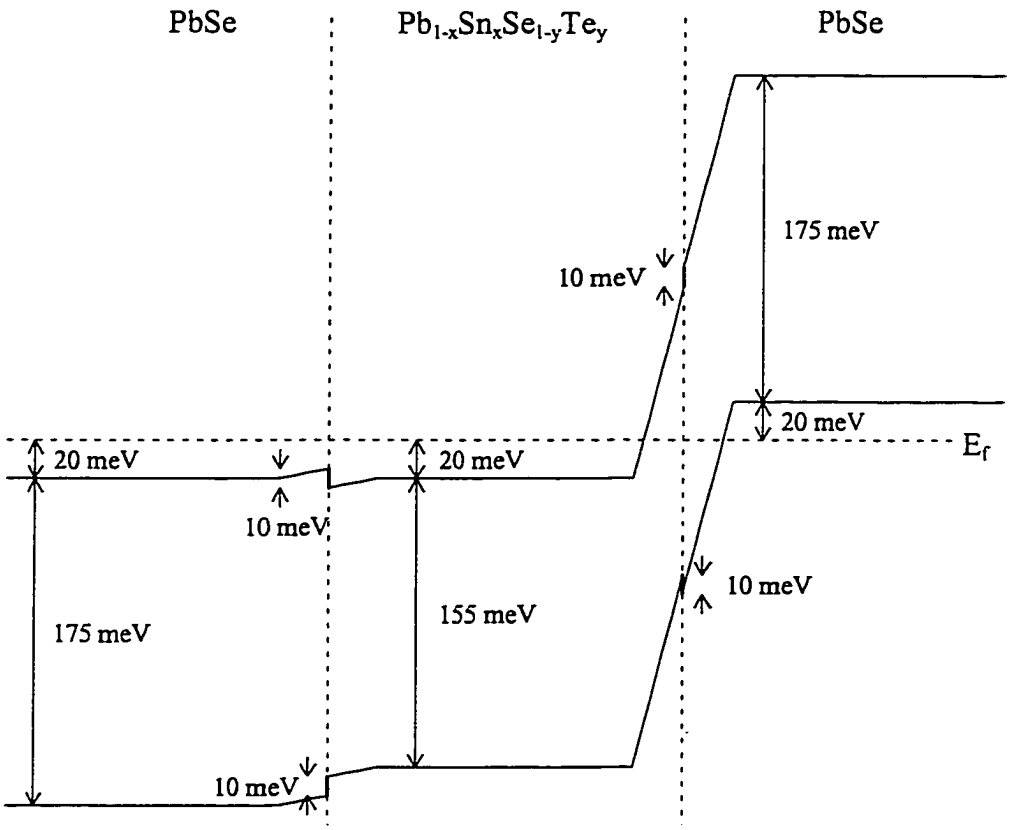

Figure 2.1 Equilibrium band alignments and Fermi level locations for a $PbSe/Pb_{0.9809}Sn_{0.0191}Se_{0.9929}Te_{0.0071}/PbSe$ DH laser structure.

Data necessary for growing $Pb_{1-x}Sn_xSe_{1-y}Te_y$ layers by LPE, lattice-matched to PbSe have been previously published [23]. The lattice parameter (in Å) of $Pb_{1-x_s}Sn_{x_s}Se_{1-y_s}Te_{y_s}$ is given by

$$a = 6.126 + 0.334y_s - 0.123x_s - 0.009x_s y_s, \tag{2-5}$$

where the subscript s indicates composition of the solid solution. By imposing the condition $a = 6.126$, one obtains

$$y_s \cong 0.369x_s \tag{2-6}$$

for lattice matching to PbSe. In this case, the energy gap of the solution at 77 K is given by [24]

$$E_g = 0.175 - 1.058x_s + 0.696x_s^2 - 0.162x_s^3. \tag{2-7}$$

Setting E_g in (2-7) to 0.155 eV and substituting the obtained x_s into (2-6) results in $x_s = 0.0191$ and $y_s = 0.0071$. From the plotted relations in reference [23] for x_s-versus-x_l —where the subscript l indicates composition in the liquid melt—and y_s-versus-y_l, one can estimate the relations for low-x_s and low-y_s LPE growths near 500 °C,

$$x_l = 1.18x_s \tag{2-8}$$

and

$$y_l = 8.89y_s, \tag{2-9}$$

which indicate values of 0.0225 and 0.0631 for x_l and y_l, respectively. These values can be converted to mass equivalents by selecting an amount of PbSe, m_{PbSe}, and employing the equations [23, 25]

$$m_{PbTe} = \frac{1.17m_{PbSe}y_l}{1 - y_l}, \tag{2-10}$$

$$m_{Pb} = \frac{m_{PbSe}\left(\frac{1}{z} - 2\right)(1 - x_l)}{1.3811(1 - y_l)}, \tag{2-11}$$

and

$$m_{Sn} = \frac{(0.57283 m_{Pb} + 0.41477 m_{PbSe} + 0.35451 m_{PbTe}) x_l}{1 - x_l}, \tag{2-12}$$

where z is the chalcogenide concentration in the $(Pb_{1-x_l}Sn_{x_l})_{1-z}(Se_{1-y_l}Te_{y_l})_z$ melt. The value of z adjusts the liquidus temperature of the melt—the point at which the last piece of solid in the growth solution dissolves—and is determined from [23] to be 0.003, corresponding to a liquidus temperature of 500 °C for the selected values of x_l and y_l. Selecting a PbSe mass of 0.1200 g provides m_{Pb} = 3.00362 g, m_{PbTe} = 0.00095 g, m_{Sn} = 0.03973 g, and a total melt mass of 3.05629 g for the desired active region composition. The small PbTe mass will be difficult to measure, but the available scale (Mettler AE240) provides sufficient resolution, ± 0.00002 g, and its omission produces a calculated lattice mismatch of 3.8 x 10^{-4}, just sufficient to generate dislocations. Fortunately, the lattice pulling effect (observed in growths where $x_l < 0.10$ [23]) mitigates small measuring errors in melt preparation by producing lattice matched layers, even when the melt composition varies slightly from the optimal.

Melt composition for the upper and lower confining layers will be nearly identical and may be determined from equations (2-10) through (2-12) for $x_l = y_l = 0$ and z = 0.0020, which produces a liquidus temperature of about 485 °C. The uppermost PbSe layer should be doped with Tl, 3.2 wt. % in the melt, to obtain p-type material [26]. Tl mass, m_{Tl}, in the PbSe melt may be calculated using [25]

$$m_{Tl} = x_{Tl} 204.38 \left(\frac{m_{Pb}}{207.20} + \frac{m_{PbSe}}{286.16} + \frac{m_{PbTe}}{334.80} + \frac{m_{Sn}}{118.71} \right), \qquad (2\text{-}13)$$

by setting x_{Tl} to 0.032 and substituting the calculated masses. A 40 minute LPE growth of PbSe layers cooled at 2 °C/min produces 2.5 μm thick layers at these chalcogenide concentrations [2]. Assuming that $Pb_{0.9809}Sn_{0.0191}Se_{0.9929}Te_{0.0071}$ grows at the same rate (and that this rate is constant with respect to growth time), a 16 minute growth duration should be used to obtain a 1 μm thick active region. The resulting structure is shown in Figure 2.2.

The effect of Tl doping upon the lattice parameter of the upper PbSe layer is unknown. Two layer LPE-grown $PbSe_{0.78}Te_{0.22}$ structures, in which one of the layers is doped with Tl, have been shown by X-ray diffraction measurements to be lattice mismatched [27]. However, the source of this mismatch—Tl doping or improper melt preparation—could not be determined; measurement of another (nominally identical) structure produced a single diffraction peak with a low shoulder where the second peak was seen in the earlier scan, proving inconclusive.

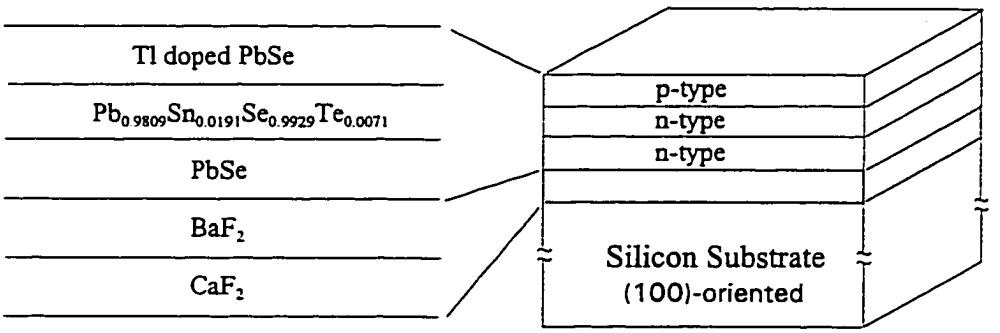

Figure 2.2 Proposed PbSe/$Pb_{0.9809}Sn_{0.0191}Se_{0.9929}Te_{0.0071}$/PbSe DH laser structure on Si(100), lattice matched to PbSe.

This structure is quite similar to one recently grown on a PbSe substrate, in which a thallium concentration of 0.3 at.% in the melt was found to be sufficient for *p*-type doping of the upper PbSe confinement layer and a record 130 K cw operating temperature (for LPE-grown IV-VI TDLs) was reported [28].

2.1.4 MBE-grown DH PbSe/PbEuSe/PbSe/PbEuSe on (100)-oriented Si

As in the LPE-grown DH laser structure described above, the first design step is determining the comprising layer compositions and thickness of the active region. The active region composition is now chosen to be **PbSe**, since its bandgap is smaller than any of the PbEuSeTe compositions—a requirement for carrier confinement. PbSe has the additional advantage of longer minority carrier diffusion lengths, compared to either $Pb_{1-x}Sn_xSe_{1-y}Te_y$ or PbEuSeTe compositions. Estimates of minority-carrier diffusion length in PbSe may be obtained from majority-carrier mobility and minority-carrier lifetimes measured in MBE-grown (100)- [29] and (111)-oriented [30] PbSe films at 77 K. Majority-carrier mobilities in *n*- and *p*-type layers ranged from 4900 cm^2/Vs (doped) to 18700 cm^2/Vs (undoped) [30]; minority-carrier lifetimes, τ, of 1.1 μs and 2.1 μs were reported in *n*-type layers [29]. Using the more conservative values, the Einstein relation

$$\frac{D}{\mu} = \frac{kT}{q}, \tag{2-14}$$

the definition of the diffusion length

$$L = \sqrt{D\tau}, \tag{2-15}$$

and assuming that the minority and majority-carrier mobilities are the same, gives an estimate of 60 μm for the minority-carrier diffusion length, providing a much less stringent limitation on the active region thickness than obtained in the previous section.

Lattice matching between the cladding layers and PbSe is not possible, as indicated by Figure 1.1 of the previous chapter. However, an estimate of the lattice mismatch may be obtained by following the Vegard's Law approach of [24] but substituting the lattice parameters of EuSe (6.185 Å [31]) and EuTe (6.590 Å [32]) for those of SnSe and SeTe. Simplification of the resulting equation produces an expression for the lattice parameter,

$$a = 6.126 + 0.059x_s + 0.334y_s + 0.071x_s y_s, \tag{2-16}$$

of the solid solution $Pb_{1-x_s}Eu_{x_s}Se_{1-y_s}Te_{y_s}$, where the variables are as described in section 2.1.2. Setting $y_s = 0$ gives the lattice parameter of $Pb_{1-x_s}Eu_{x_s}Se$ as

$$a = 6.126 + 0.059x_s. \tag{2-17}$$

The energy gap may be estimated similarly—using E_g = 1.80 eV and 2.00 eV for EuSe and EuTe, respectively [33]—as

$$E_g = 0.175 + 1.625x_s + 0.042y_s + 0.158x_s y_s \tag{2-18}$$

for the quaternary case, and as

$$E_g = 0.175 + 1.625x_s \tag{2-19}$$

in the case of $Pb_{1-x_s}Eu_{x_s}Se$. Unlike lead-chalcogenides, the energy gap of EuSe and EuTe changes little with temperature—it varies less than the uncertainty of the energy gap measurement, ±0.05 eV, between 30 and 300 K [33]. Energy gap values at 300 K were, therefore, used for the europium chalcogenides in obtaining equations (2-18) and (2-19); 77 K data were used for the lead chalcogenides.

The more general equations, while not required for designing the present structure, will allow calculation of the lattice parameter and energy gap for quaternary

solid solutions. These will be needed as cladding layers in a DH structure incorporating a PbSeTe or PbTe active region. As noted above, exact lattice match to PbSe is not possible in the PbEuSeTe system; a high density of dislocation defects is, therefore, quite possible in PbEuSe/PbSe structures. Resulting recombination centers would hamper high temperature operation; however, layer degradation may be compensated by the improved properties of the PbSe active region, compared to $Pb_{1-x}Sn_xSe_{1-y}Te_y$. Once recipes have been developed for growing PbTe and PbSeTe solutions using MBE, these materials should be investigated as replacements for PbSe.

Repeating the procedure used in section 2.1.3 for PbEuSe cladding layers having an energy gap 0.020 eV larger than PbSe results in the following device parameters: $E_{gPbEuSe} = 0.195$ eV at 77 K, $\lambda_{PbEuSe} = 6.36$ μm, $x_s = 0.0123$, $a_{PbEuSe} = 6.1267$ Å, $n_{PbEuSe} = 4.57$, $d_{max} = 2.9$ μm at M=1, $d_{min} = 0.76$ μm, and $\Delta a = 1.1 \times 10^{-4}$. Since the lattice mismatch is below the threshold of 2×10^{-4} given in [14], misfit dislocations may not degrade the device as feared. In addition, the expected longer minority-carrier diffusion length in the PbSe active region should result in more uniform gain and decreased losses due to non-radiative recombination. An active region thickness of 1 μm again seems prudent. The resulting structure—which is similar to one grown on PbSe, also using Eu in the cladding layers, that reached 174 K cw operation [34] and another, using Sr in the cladding, that reached 169 K cw operation [35]—is shown in Figure 2.3.

Applying the procedure for estimating the band structure of the $Pb_{1-x}Sn_xSe_{1-y}Te_y$ active region structure to the present structure produces the equilibrium band structure diagram shown in Figure 2.4. Examination of the figure indicates expected carrier confinement barriers of approximately 20 meV, as in the previous case. Addition of the

PbSe layer nearest the silicon substrate, needed for overcoming the cracking normally found in IV-VI layers on (100)-oriented silicon, does not hinder electron flow into the active region because the degeneracy of the three *n*-type layers.

Should larger barriers be required, Eu concentration in the cladding layers can be increased. However, this would increase the lattice mismatch between the layers in the structure and increase the defect density—and non-radiative recombination—expected in the active region.

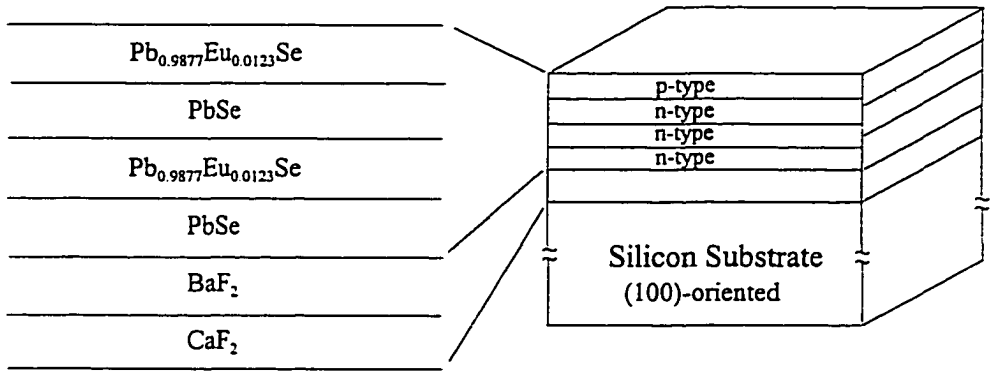

Figure 2.3 Proposed MBE-grown PbSe/$Pb_{0.9877}Eu_{0.0123}Se$/PbSe/ $Pb_{0.9877}Eu_{0.0123}Se$ DH laser structure on Si(100), nearly lattice-matched to PbSe. The PbSe layer closest to the fluoride buffer is grown using a combination of MBE and LPE to produce the crack-free surface needed for further growth [2]. All other layers are grown using MBE. Doping of the uppermost layer is obtained by introducing Se overpressure during layer growth [11, 34].

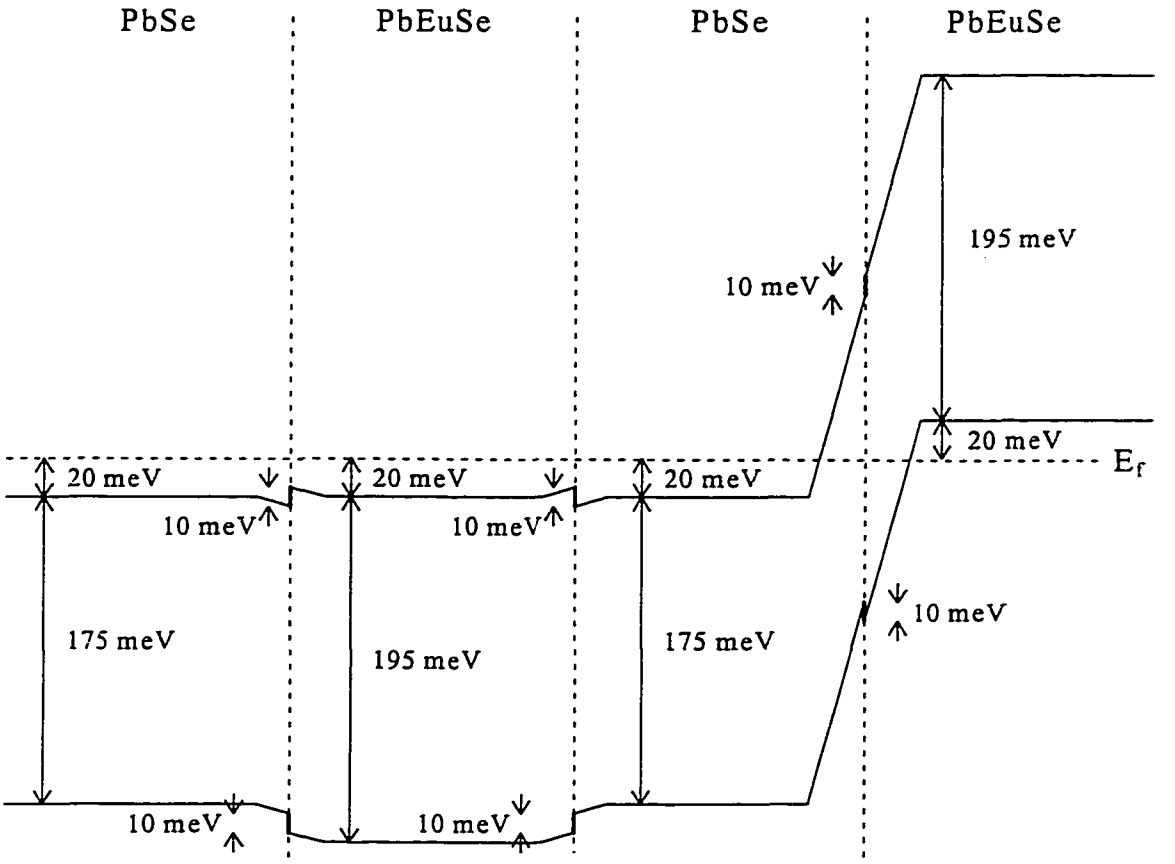

Figure 2.4 Equilibrium band alignments and Fermi level locations for a PbSe/$Pb_{0.9877}Eu_{0.0123}Se$/PbSe/ $Pb_{0.9877}Eu_{0.0123}Se$ DH laser structure.

2.2 *Vertical cavity surface emitting laser structure (VCSEL)*

By switching from a horizontal to a vertical cavity, one can obtain single mode output from a non-cleaved structure. This structure can be grown on (111)-oriented silicon—where continuous IV-VI layers are readily growable—since cleaved mirrors are not required. Bragg reflectors incorporated above and below the active region act as frequency selective mirrors, replacing the cleaved mirrors of the DH structure and reducing the bandwidth of the frequencies reflected. Since this bandwidth can be made smaller than the frequency spacing between modes supported by the shortened cavity, single mode output is possible.

Longitudinal mode spacing in a laser is inversely proportional to the cavity length. By employing a VCSEL configuration, the cavity length can be shortened sufficiently to produce a mode spacing larger than the bandwidth of the Bragg reflector mirrors. Design of the VCSEL structure is then, in large part, determining the desired active region thickness (setting the lasing frequency and the mode spacing) and the composition of the Bragg reflectors (setting the bandwidth and reflectivities of the mirrors). For an optically pumped structure, concerns for the electrical resistivity of the Bragg reflectors—which greatly increases the design difficulty—can be ignored.

A Bragg reflector may be considered to be a stack of simple two layer reflectors, where each simple reflector comprises a pair of low and high refractive index layers whose thicknesses are chosen to be one fourth of the wavelength of the light to be reflected. This $\lambda/4$ rule produces the highest reflectivity for a pair with the lowest thickness. The reflectivity of a single pair increases as the difference in refractive indices between the layers increases. The $\lambda/4$ rule may be understood by examining the

reflection of light at the two interfaces shown in Figure 2.5. As the light approaches from the left, a certain amount will be reflected at the n_0/n_1 interface. If n_0 is less than n_1, then the phase shift of the reflected light will be π. The light transmitted propagates through the n_1 region until it reaches the n_1/n_2 interface, where a portion is reflected. If n_2 is chosen so that $n_2 < n_1$, a phase shift of zero occurs for the reflected wave. After the wave reflected at the n_1/n_2 interface has passed though the layer twice, it has undergone a shift of π (or $\lambda/2$) and is in phase with the wave reflected from the first interface, adding to its amplitude. The light transmitted continues traveling through the structure until it encounters the n_2/n_1 interface, where the next reflective pair begins. This interface produces a shift of π, so that the reflected light reaching the previous n_1/n_2 interface has undergone a phase shift of 2π—from the shift at the interface and from traveling through the layer twice.

The total power reflectivity of a Bragg mirror may be estimated, for non-absorbing layers, as

$$R = \left[\frac{1 - \frac{n_s}{n_o}\left(\frac{n_1}{n_2}\right)^{2m}}{1 + \frac{n_s}{n_o}\left(\frac{n_1}{n_2}\right)^{2m}} \right]^2, \qquad (2\text{-}20)$$

where n_s, n_0, n_1, and n_2 are the refractive indices of the substrate, the material to the left of the stack in Figure 2.5, the leftmost layer of the Bragg stack in Figure 2.5, and the layer to the right of the leftmost Bragg stack layer, respectively. m is the number of layer pairs.

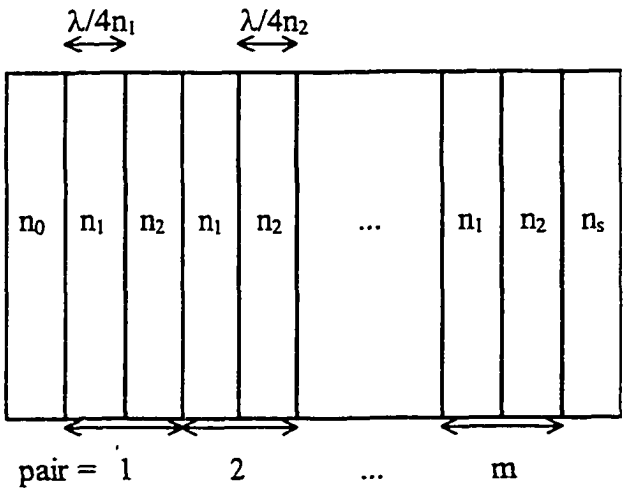

Figure 2.5: A Bragg reflector consisting of m simple n_1-n_2 reflector pairs comprising layers of refractive indices n_1 and n_2 . The reflector is bounded by a materials having refractive indices of n_0 on the left and n_s on the right.

CaF_2 and $Pb_{0.9877}Eu_{0.0123}Se$ are recommended for the Bragg reflector materials due to the large difference in refractive indices and the availability of growth procedures for the materials. PbEuSe is used because of the near lattice matching which can be obtained with PbSe and its larger bandgap—necessary to avoid absorption of the laser light by the mirrors. PbSe is chosen for its large carrier mobility—which will be needed for transporting optically generate carriers away from the VCSEL surface and toward the center of the active region.

The mirror reflectivities needed to attain lasing for a given VCSEL may be evaluated by

$$\alpha = \frac{1}{2L}\ln\left(\frac{1}{R_1 R_2}\right), \tag{2-21}$$

where α is the gain, L is the cavity length (active layer thickness), and R_1 and R_2 are the power reflectivities of the two mirrors. In (2-21), all losses not associated with the mirrors have been subsumed into α, which is then the gain remaining after compensating for all other losses. Because L for single mode operation is limited to a few μm, the reflectivities R_1 and R_2 must be nearly 1. The reflectivity of the light extraction mirror should be slightly lower than its mate so that usable output is not lost.

The normal procedure for calculating the required mirror reflectivities is to assume a gain for the active layer, estimate the cavity length, and then calculate the product R_1R_2. Mirrors can then be designed which exceed this reflectivity product. In the present case, lack of a gain estimate precludes such an approach. The opposite approach is, therefore, taken. Given the materials readily available for growing Bragg reflectors,

the required gain may be calculated for a series of reflectivity products obtained for different mirror structures.

Examination of the VCSEL structure indicates that light may be extracted from the top or through the substrate. Light is often extracted through the substrate via the lower mirror so that metal contacts can be employed for injecting current through the top mirror. Unfortunately, the substrate must then be thinned and anti-reflective coatings on the back side of the device are often needed to assist with light extraction. For an optically pumped laser, contacting the top surface for current injection is not necessary, and it was decided that surface emission was the preferred route. This selection necessitates a higher reflectivity mirror for the bottom of the structure. Calculating the reflectivity of the lower mirror by setting the refractive indices in Figure 2.5 to $n_0 = n_{PbSe} = 4.69$, $n_1 = n_{PbEuSe} = 4.57$, $n_2 = n_{CaF2} = 1.37$, and $n_s = n_{Si} = 3.42$ provides the power reflectivities listed in Table 2.1 for increasing numbers of reflective pairs, m. The refractive indices used for CaF_2 and Si are measured room temperature values. Values for PbSe and $Pb_{0.9877}Eu_{0.0123}Se$ and PbSe are the 77 K estimates obtained in Section 2.1.3.

Repeating this procedure for the top mirror, but with $n_0 = n_{vacuum} = 1$, $n_1 = n_{PbEuSe} = 4.57$, $n_2 = n_{CaF2} = 1.37$, and $n_s = n_{PbSe} = 4.69$ results in the power reflectivities listed in Table 2.2. By selecting mirrors such that $R_{bottom} \approx 10\ R_{top}$, most of the light will be emitted through the top mirror as useful output. According to Tables 2.1 and 2.2 and (2-21), these desired mirror pairs are B_6T_4, B_5T_3, B_4T_2, and B_3T_1.

By calculating the bandwidth of the reflectors in reciprocal wavelength by [42]

$$\Delta\frac{1}{\lambda_g} = \frac{4}{\pi\lambda_0}\sin^{-1}\left(\frac{n_1 - n_2}{n_1 + n_2}\right) \tag{2-22}$$

one can estimate the maximum active region thickness having a longitudinal mode spacing sufficient for single mode operation. For the PbEuSe/CaF_2 stack tuned to 7.1 μm, $\Delta\frac{1}{\lambda_g}$ from (2-22) is 1020 cm^{-1}. From the requirement for single longitudinal mode operation [40]

$$L \leq \frac{c}{\Delta\nu_g} = \frac{c}{\Delta\frac{c}{\lambda_g}} = \left[\Delta\frac{1}{\lambda_g}\right]^{-1} \tag{2-23}$$

an upper limit of 9.08 μm is established for the active region thickness. The minimal cavity length is obtained by the requirement that the round trip phase change of the propagating light must equal an integral multiple of 2π [41]. Since the refractive index change from the active region to the first layer of the Bragg reflector is negative, no phase shift is observed at the mirrors and the cavity length must be a multiple of $\lambda/2$, where λ is the wavelength in the active region—7.1 μm / n_{PbSe} = 1.51 μm. Requisite active region gains (in cm^{-1}) for 0.757 μm and 9.08 μm active layer thicknesses are listed in Table 2.3. (0.757 μm is the thinnest layer consistent with constructive interference and 9.08 μm is the thickest layer consistent with single mode operation.) The resulting structure, incorporating a 9.08 μm active region, is shown in Figure 2.6. It may be desirable to incorporate a thinner active region—to increase the life of the MBE system's PbSe source material. However, thinner layers provide lower gains and the quality of the Bragg reflectors would need to be raised accordingly. This VCSEL can be grown through a shadow mask, avoiding photolithographic steps which might prove harmful to the water soluble CaF_2 layers in the Bragg reflectors.

Table 2.1: Power reflectivities calculated from (2-20) for the bottom mirror of a VCSEL comprising $Pb_{0.9877}Eu_{0.0123}Se$ and CaF_2 layers. m is the number of Bragg pairs. Refractive indices measured at 7.1 μm and 300 K are used for Si and CaF_2; 77 K estimates from Section 2.1.3, also at 7.1 μm, are used for PbSe and $Pb_{0.9877}Eu_{0.0123}Se$.

Label	m	R
B_1	1	0.609277
B_2	2	0.956663
B_3	3	0.996027
B_4	4	0.999642
B_5	5	0.999968
B_6	6	0.999997

Table 2.2: Power reflectivities calculated from (2-20) for the top mirror of a VCSEL comprising $Pb_{0.9877}Eu_{0.0123}Se$ and CaF_2 reflectors. m is the number of Bragg pairs. Refractive index measured at 7.1 μm and 300 K is used for CaF_2; 77 K estimates from Section 2.1.3, also at 7.1 μm, are used for PbSe and $Pb_{0.9877}Eu_{0.0123}Se$; n_{vacuum} is taken as 1.

Label	m	R
T_1	1	0.926208
T_2	2	0.993135
T_3	3	0.999381
T_4	4	0.99944
T_5	5	0.999995

Table 2.3: Calculated active region gain requirements for the selected Bragg reflector pairs and active region thicknesses of 0.757 μm and 9.08 μm.

Mirrors	$\alpha_{0.757}$	$\alpha_{9.08}$
B_3T_1	532	44
B_4T_2	48	4.0
B_5T_3	4.3	0.4
B_6T_4	0.4	0.03

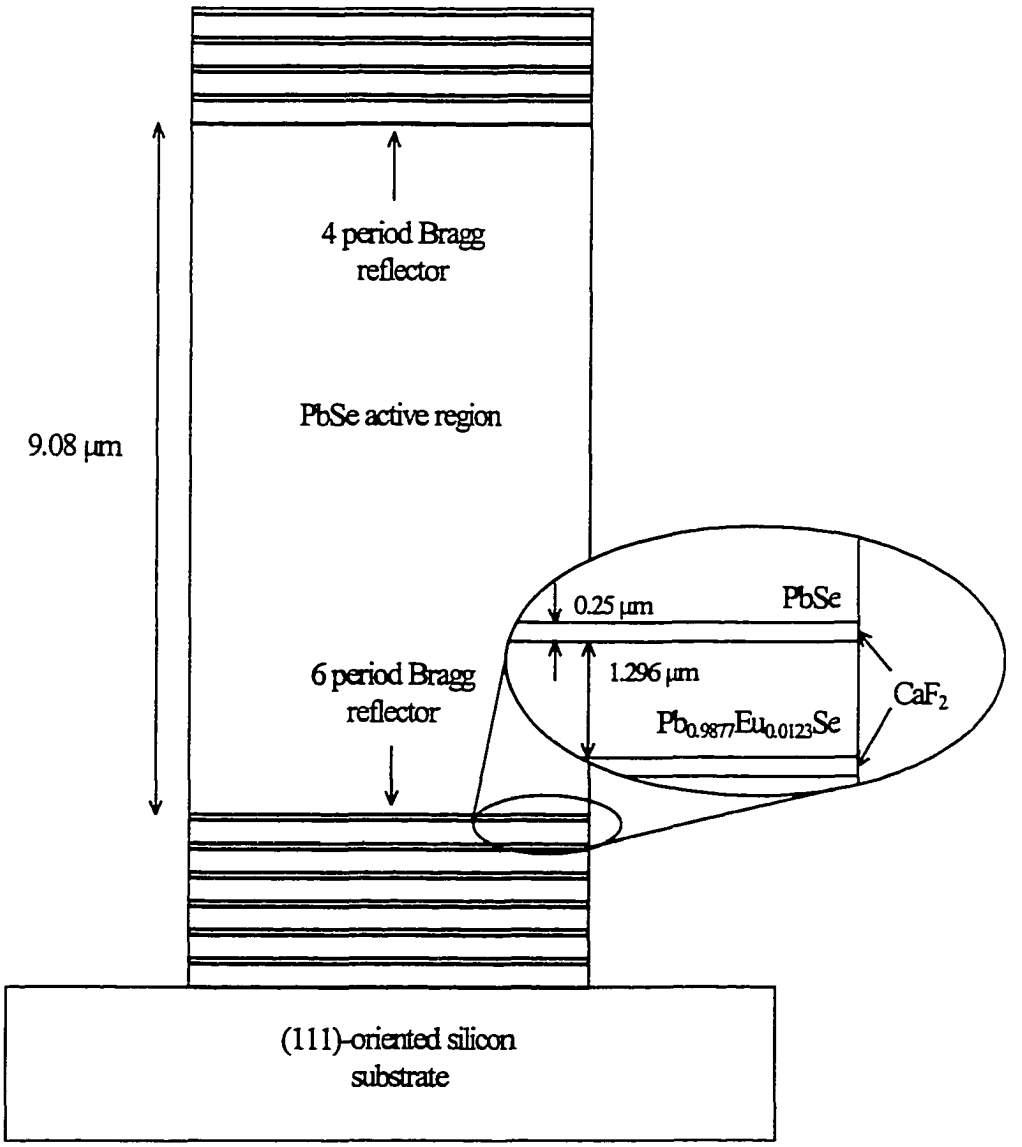

Figure 2.6: Complete VCSEL structure (to scale vertically) consisting of a 4 period top Bragg reflector, a 6 period bottom Bragg reflector, and a 9.08 μm thick PbSe active region. Optical illumination from the sides provides the excess carriers required for lasing. Lateral extent should be greater than 2 μm.

2.3 *References*

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Chapter 3: Growth of IV-VI Heterostructures on (100)-oriented BaF_2 Substrates by LPE

Previous work at MIT by McCann and Fonstad [1] showed that PbSe could be grown epitaxially on polished (100)-oriented BaF_2 substrates by LPE. This work was extended to demonstrate growth of $PbSe_{0.78}Te_{0.22}$ [2,3] and $Pb_{1-x}Sn_xSe_{1-y}Te_y$ [4,5] layers lattice-matched to BaF_2. These results provided the basis for successful attempts to grow multilayer structures for DH lasers [6].

In anticipation of the development of epitaxial liftoff and cleaving techniques, a series of growths was undertaken to develop recipes and to collect electrical data for the IV-VI materials expected to comprise an eventual DH laser. Due to the novelty of growing IV-VI layers on BaF_2 by LPE, carrier concentration data are available only for the $PbSe_{0.78}Te_{0.22}$ alloy [3]. And these are for materials grown at higher temperatures than desired for layers to be used in laser fabrication. Because the electrical properties of IV-VI materials are highly dependent upon their growth and processing history, it is important to collect the data from samples closely approximating the layers to be used for laser fabrication. A total of 48 growths—many of which contained more than one layer—were performed on BaF_2.

3.1 Procedure

IV-VI layers of varied compositions and arrangements were grown on polished (100)-oriented BaF_2 substrates using LPE. Layers deemed suitable for electrical measurement were contacted and their Hall mobilities and carrier concentrations estimated employing a variant of the van der Pauw technique [7]. Optical Nomarski and scanning electron micrographs were taken of representative samples.

The 48 LPE growths on BaF_2 were divided as follows: 17 $PbSe_{0.78}Te_{0.22}$ single layer, 5 $Pb_{1-x}Sn_xSe_{0.78}Te_{0.22}$ single layer, 5 PbTe-on-$PbSe_{0.78}Te_{0.22}$ double layer, 7 PbSe-on-$PbSe_{0.78}Te_{0.22}$ double layer, 8 $Pb_{1-x}Sn_xSe_{0.78}Te_{0.22}$-on-$PbSe_{0.78}Te_{0.22}$ double layer, 2 $PbSe_{0.78}Te_{0.22}$-on-$Pb_{1-x}Sn_xSe_{0.78}Te_{0.22}$ double layer, and 3 $PbSe_{0.78}Te_{0.22}$-on-$Pb_{1-x}Sn_xSe_{0.78}Te_{0.22}$-on-$PbSe_{0.78}Te_{0.22}$ triple layer heterostructures.

The procedure for growing the layers began with preparation of the BaF_2 substrates, as described in Appendix A. Substrates for the earliest growths were prepared using the original polishing procedure with modifications to the procedure being made periodically until growth number 73. (LPE growths on Si were conducted in parallel and numbers were assigned sequentially. This is why there is a growth number 73 but only 48 growths on BaF_2.) The prepared substrate was placed in the pocket of a graphite slider (see Figure 1.7) which transported the substrate within the furnace. Thin graphite spacers were placed below the substrate for leveling and setting the substrate surface-to-slider surface clearance. The slider and substrate were placed in a graphite boat prior to melt preparation, so that melt material could be quickly loaded and the assembly transferred to the furnace. Melt materials were prepared as described in Appendix B and placed in wells in the graphite boat. Although the most complicated structure grown during this project contained only three LPE layers, the boat allows four different melts to be loaded simultaneously. After loading, the furnace was flushed with purified hydrogen gas for a minimum of 30 minutes before the heating coils were energized. Melts were homogenized at least 50 °C above the expected liquidus temperature, the oven was cooled, and the nucleation and liquidus temperatures of the melts were measured and verified. The system was then reheated above the liquidus temperature of the first melt

and cooled at 2 °C min^{-1}. One minute before reaching the nucleation temperature, the substrate was brought into contact with the first melt by moving the graphite slider. Nucleation was observed through a microscope monitoring the top surface of the melt. Growth continued for the desired period, at which point the substrate was slid beyond the well. If additional layers were desired, the oven temperature was brought above the liquidus temperature of the second well and the growth procedure was repeated. After completion of the desired structure, the oven was cooled to room temperature. The system was then flushed with Ar and the sample removed. Electrical contacts were formed by vacuum evaporation of Au or Pb through a shadow mask. Contacting evolved over the course of the project with the sample-to-source distance and rate of evaporation changing. Electrical connection to the Au or Pb spots was made by Cu probes or In/Au leads pressure fit onto the spots or epilayer surface.

3.2 Results

3.2.1 $PbSe_{0.78}Te_{0.22}$

The 17 samples of $PbSe_{0.78}Te_{0.22}$ grown on (100)-oriented BaF_2 are listed in Table 3.1. Samples 9, 11, 13, 14, 15, and 17 were suitable for electrical characterization, but 13 and 17 were used as substrates for further growth and were unavailable. An array of Au contacts was deposited through a shadow mask onto the samples' surface. Connection to the contacts was made by press fitting In spheres formed on the end of Au wire onto the Au-coated surface and connecting the Au wire to the Hall measurement fixture. The measured Hall mobilities and carrier concentrations for the four samples are listed in Table 3.2. Samples labeled 15.a and 15.b were contacted without the Au evaporation step using In spheres on Au wire pressed directly onto the surface of the $PbSe_{0.78}Te_{0.22}$. These

contacts were made at the corners (15.a) or edges (15.b) of the sample. Optical Nomarski micrographs of samples 9 and 11 are shown in Figure 3.1. Dark regions observed on 9 and 11 are believed to be inclusions of melt. These appear as rounded lighter regions on samples 14 and 15, shown in Figure 3.2.

Table 3.1: Samples of $PbSe_{0.78}Te_{0.22}$ grown on (100)-oriented BaF_2 substrates using LPE. z is the chalcogenide concentration in the melt. T_n and T_l are the nucleation and liquidus temperatures of the melt. BaF_2 depth, min, and max are the estimated average, minimum, and maximum clearance between the corners of the BaF_2 substrate and the slider surface. Negative values indicate protrusion above the slider surface.

Sample	z wt%	T_n °C	T_l °C	BaF_2 depth µm	BaF_2 max µm	BaF_2 min µm	Result
1	2.9	635	638	76	90	66	no growth
1b	2.9	593	597	75	90	66	partial coverage
2	2.9	610	613	87	90	79	poor
3	2.9	589	593	47	60	30	complete coverage / sparkles
4	3.2	642	646	10	18	4	poor
5	3.1	600	603	30	40	13	oriented crystals / partial coverage
6	3.1	636	640	11	18	-30	partial coverage
9	3.1	626					continuous / melt adhesion
10	3.1	613	615	14	40	-12	continuous / melt adhesion
11	3.1	613	618	-8	0	-17	continuous / melt adhesion
12	3.1	614	617	-33	18	-55	continuous / melt adhesion
13	3.1	638	641	6	32	-24	continuous / clean
14	3.1	625	628	-1	27	-15	continuous / ½ clean - ½ melt adhesion
15	3.1	605	609	-17	0	-45	continuous / melt adhesion - scratched
16	3.1	619	624	-17	7	-43	continuous / clean
17	3.1	635	639	-21	8	-47	continuous / clean
53	3.2	623	626	30	37	20	surface covered by solid melt adhesion

Table 3.2: Hall mobility, carrier concentration, peak-to-peak surface roughness and thickness of four single layer $PbSe_{0.78}Te_{0.22}$ samples measured at 300 K. Samples 9, 11, 14, and 15 were contacted using Au spots away from the edge of the sample. Samples 15.a and 15.b were contacted using In at the sample corners and edges. Lip is the height of a ridge at the layer's edge, in those samples that had them.

Sample	$\mu_{300\,K}$ cm^2/Vs	$(p\text{-}n)_{300\,K}$ cm^{-3}	Δd μm	lip μm	d μm
9	93	-1.3×10^{20}	2		6
11	56	-6.0×10^{19}	2	18	10
14	61	-2.4×10^{20}	3		6
15	47	-1.6×10^{20}	3	10	12.5
15.a	230	-1.9×10^{19}	3	10	12.5
15.b	150	-3.2×10^{19}	3	10	12.5

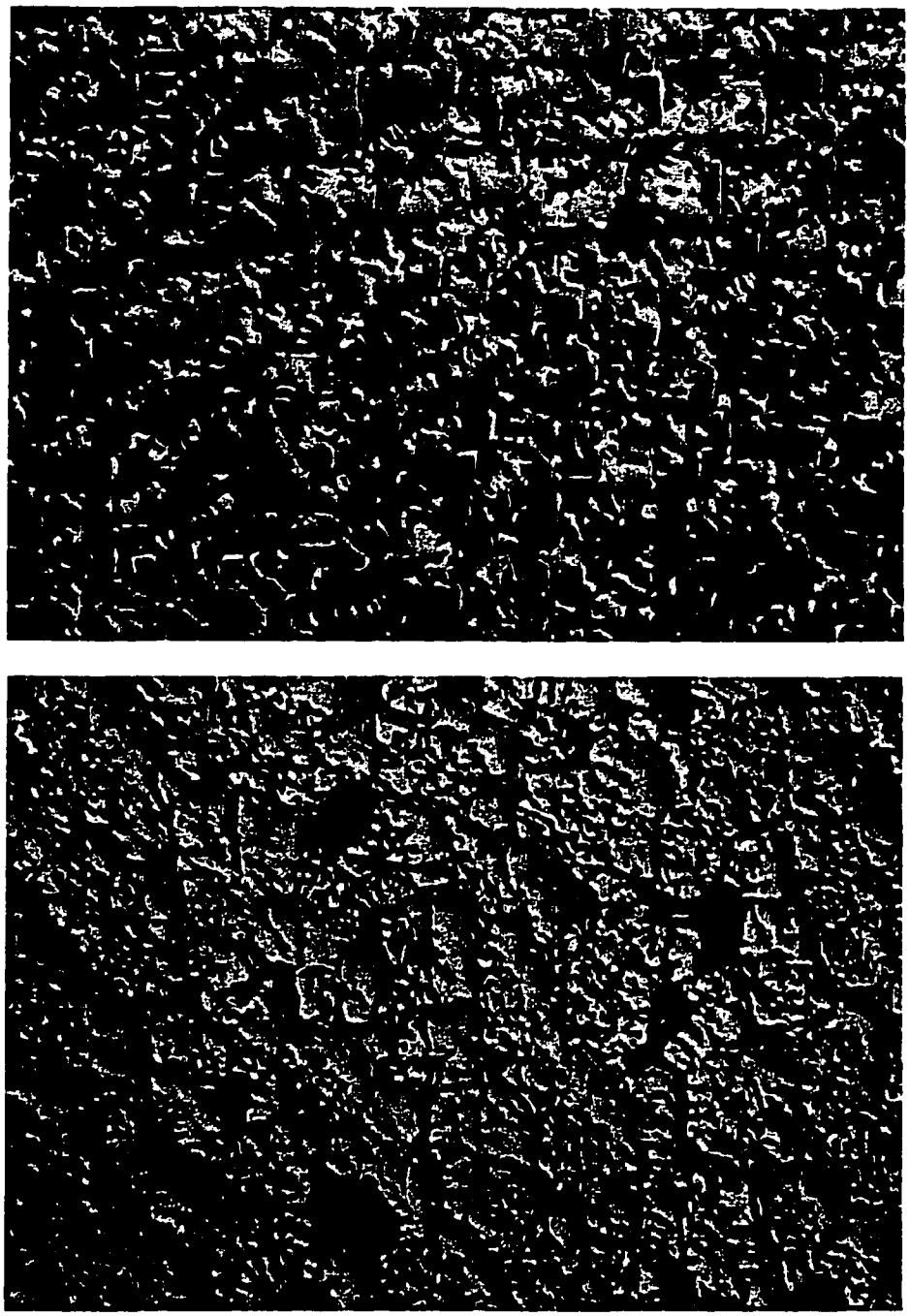

Figure 3.1: Optical Nomarski micrographs of samples 9 (top) and 11 (bottom), ternary single layers grown on $BaF_2(100)$. Dark regions observed on 9 and 11 are believed to be inclusions of melt. The micrographs are 500 x 380 μm^2 in area.

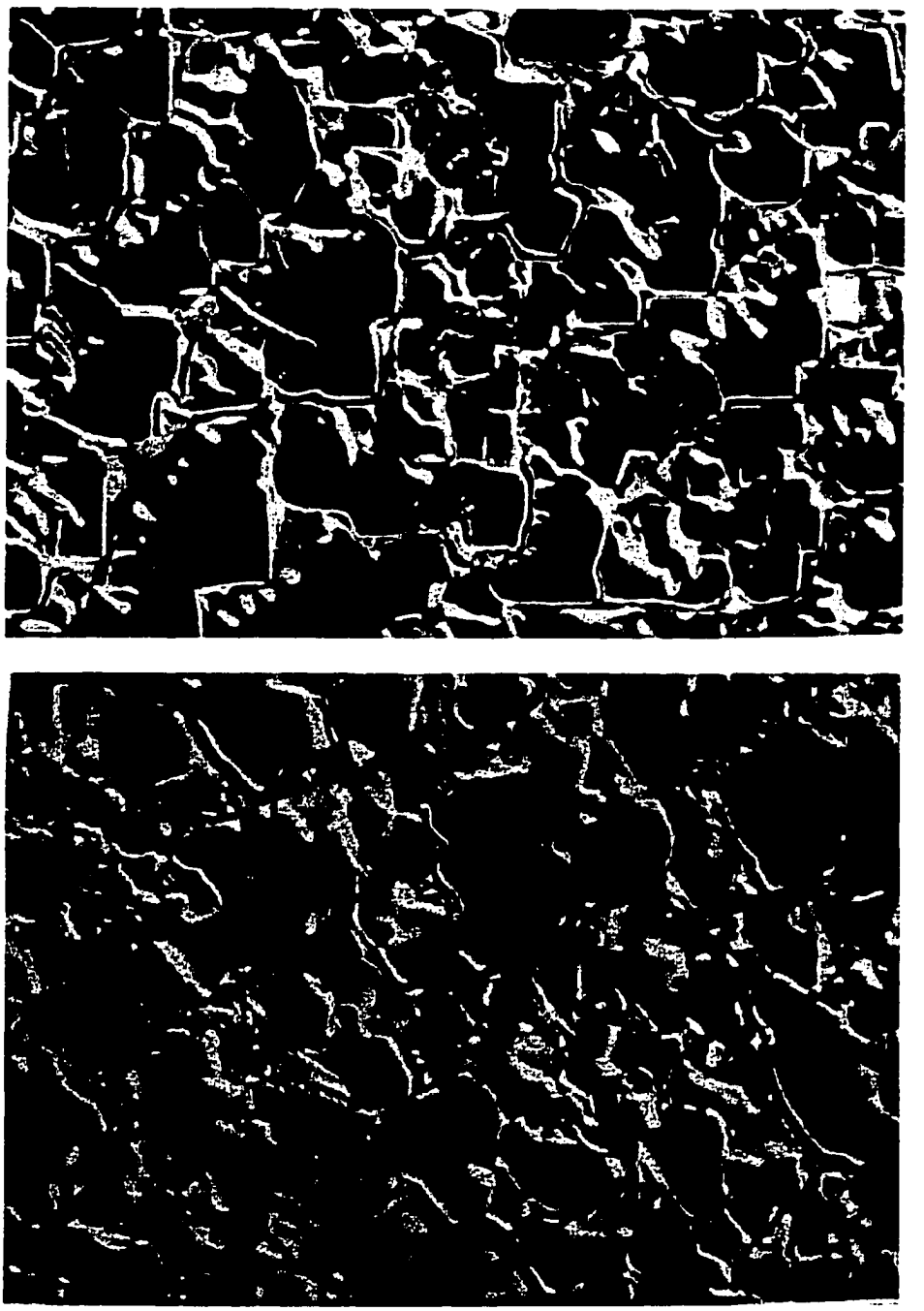

Figure 3.2: Optical Nomarski micrographs of samples 14 (top) and 15 (bottom), ternary single layers grown on BaF_2(100). Light, rounded regions in the 250 x 190 μm^2 micrographs are believed to be inclusions of melt.

3.2.2 $Pb_{1-x}Sn_xSe_{0.78}Te_{0.22}$

The five quaternary layers grown on (100)-oriented BaF_2 are listed in Table 3.3. Surface roughness of layers 75 and 77 was much reduced compared to all previous single layers on BaF_2. Layers displaying excellent surface morphology were obtained. Figure 3.3, an optical Nomarski micrograph, shows a 250 x 190 μm^2 region of the surface of sample 77—which displayed such morphology. Growth 76 unintentionally varied from the described growth procedure due to accidental substitution of the slider (see Figure 1.7). The employed slider placed the substrate at a different location within the boat than expected. Consequently, the substrate was pulled through the melt and not allowed to remain in contact as desired. This provided the view of the initial stage of LPE growth on (100)-oriented BaF_2 shown in Figure 3.4, a 100 x 75 μm^2 optical Nomarski micrograph of sample 76. Located elsewhere on the substrate used for sample 76 were etch pits formed during subtrate preparation. An identically prepared substrate was used for growth 75 and patterns similar to the etch pit patterns in substrate 76 were visible in the LPE-grown quaternary layer. Comparison of the surfaces of the substrate for growth 76 and the layer of sample 75 is shown in Figure 3.5.

Copper probes pressed onto evaporated Au spots made electrical connection to the surface. The results of Hall measurements made with these contacts are presented in Table 3.4.

Table 3.3: Samples of $Pb_{1-x}Sn_xSe_{0.78}Te_{0.22}$ grown on (100)-oriented BaF_2 substrates using LPE. T_n and T_l are the nucleation and liquidus temperatures of the melt. BaF_2 depth, min, and max are the estimated average, minimum, and maximum clearance between the corners of the BaF_2 substrate and the slider surface. Chalcogenide concentration in the melt was 3.4 wt.% for all samples

Sample	x wt.%	T_n °C	T_l °C	BaF_2 depth μm	BaF_2 max μm	BaF_2 min μm	Result
67	12	618	620	16	30	0	good growth
75	12	617	620	21	28	12	good growth
76	5	623	626				15 sec exposure to melt
77	5	623	626	25	39	5	good growth
80	20	609	613	46	70	30	good growth

Table 3.4: Hall mobility, carrier concentration, peak-to-peak surface roughness and thickness of four single layer $Pb_{1-x}Sn_xSe_{0.78}Te_{0.22}$ samples measured at 300 K and 77 K. Samples were contacted using Au spots away from the edge of the sample. Lip is the height of the ridge at the layer's edge.

Sample	μ_{77K} cm^2/Vs	$(p\text{-}n)_{77K}$ cm^{-3}	μ_{300K} cm^2/Vs	$(p\text{-}n)_{300K}$ cm^{-3}	Δd μm	lip μm	d μm
67	1024	-2.2×10^{19}	122	-1.7×10^{19}	2	2	7
75	873	-1.0×10^{19}	120	-5.8×10^{18}	0.25	5	2
77	5300	-5.5×10^{18}	319	-7.5×10^{18}	0.4	4	3

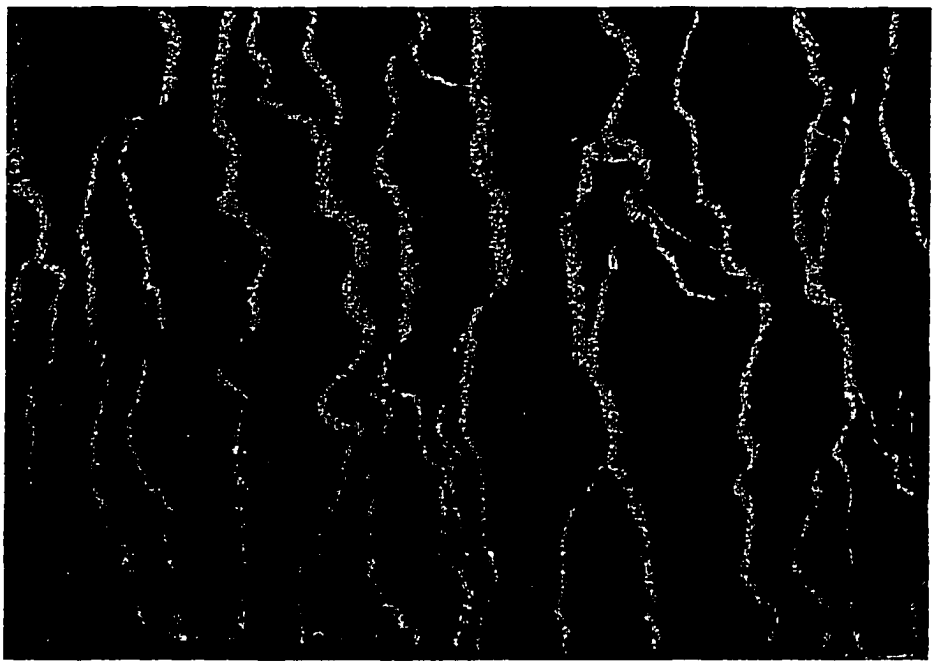

Figure 3.3: Optical Nomarski micrograph of sample 77, a single quaternary layer grown on (100)-oriented BaF_2 by LPE. The layer had excellent surface morphology and lacked inclusions and melt adhesion, seen in other growths. A 250 x 190 μm^2 area is displayed.

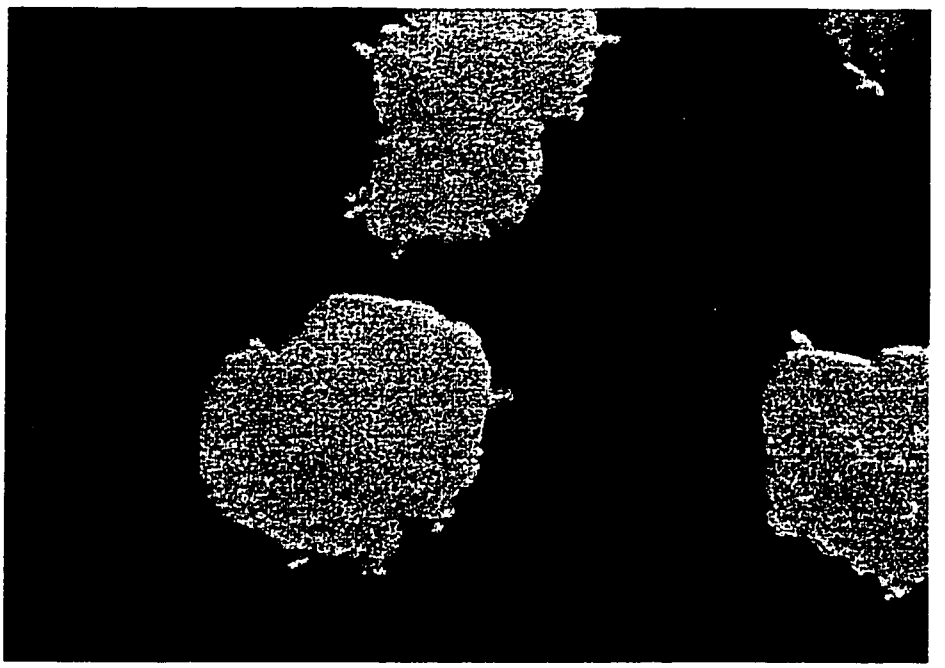

Figure 3.4: Optical Nomarski micrograph of sample 76, the initial stage of LPE growth for a quaternary single layer on (100)-oriented BaF_2. The darker region is the substrate. Shallow etch pits decorate its surface. A 100 X 75 μm^2 area is displayed.

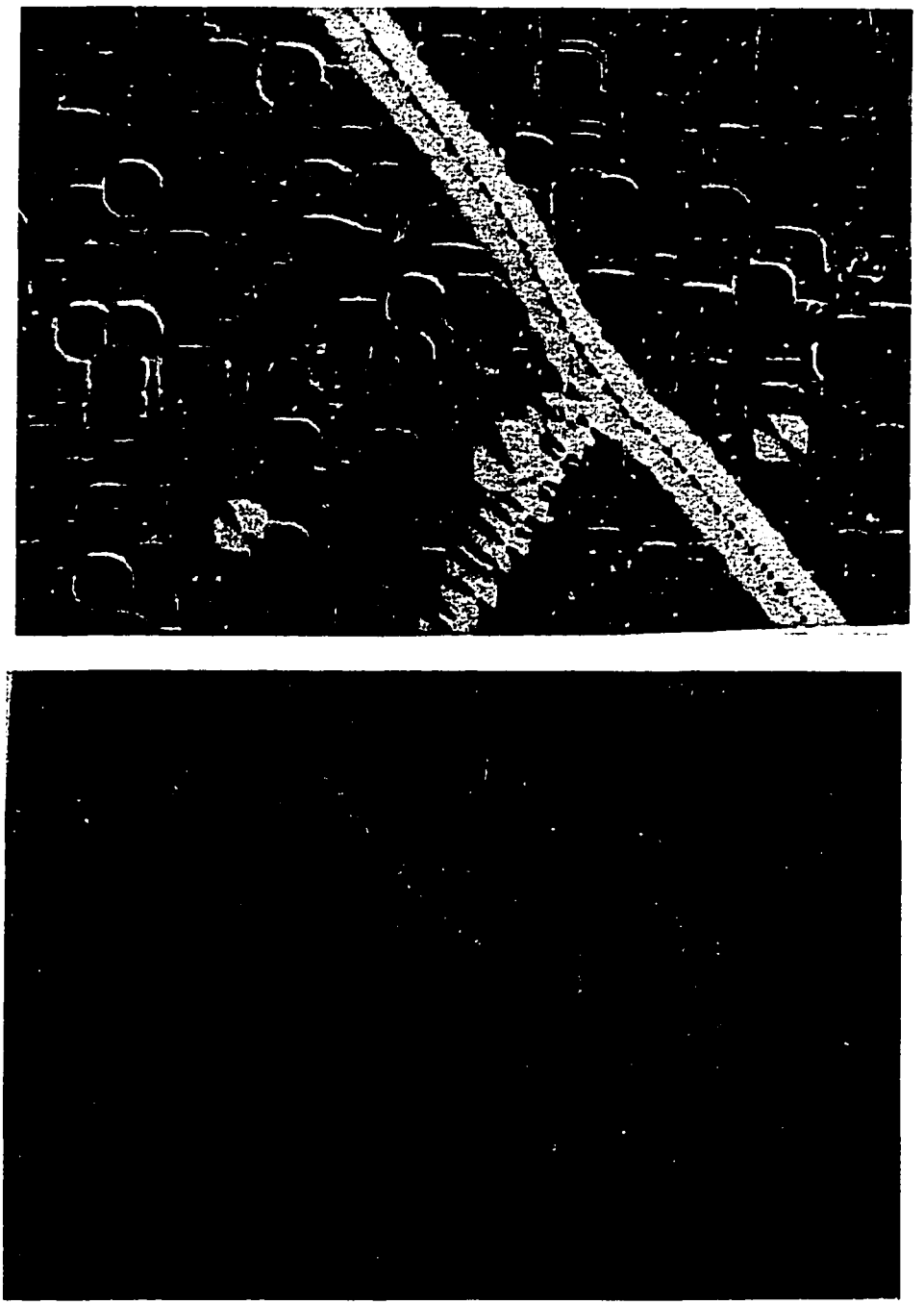

Figure 3.5: Etch pit pattern observed on the prepared (100)-oriented BaF_2 substrate of sample 76 (top), and a similarly shaped pattern of inclusions observed in the LPE-grown quaternary layer of sample 75 (bottom). Substrates were prepared identically. The optical Nomarski micrograph of sample 76 shows 250 x 190 μm^2, and the micrograph of sample 75 shows 500 x 380 μm^2.

3.2.3 *PbSe and PbTe on $PbSe_{0.78}Te_{0.22}$*

Seven two-layer PbSe-on-$PbSe_{0.78}Te_{0.22}$ structures were grown. These are listed in Table 3.5. Two of the layers, 38 and 39, were doped with 2 wt.% Tl in the melt. Five PbTe-on-$PbSe_{0.78}Te_{0.22}$ structures were grown. The growth data for these structures are listed in Table 3.6. A slight decrease in nucleation temperature is observed for compositions of increasing Tl in the PbTe layers of Table 3.6. This trend is not evident in the Tl-doped ternary layers of Table 3.5. It is, perhaps, obscured by melt-to-melt variation in measured nucleation temperature due to other factors. No electrical measurements were taken of these layers.

Table 3.5: $PbSe/PbSe_{0.78}Te_{0.22}$ structures grown on (100)-oriented BaF_2 substrates using LPE. T_n and T_l are the nucleation and liquidus temperatures of the melt. BaF_2 depth, min, and max are the estimated average, minimum, and maximum clearance between the corners of the BaF_2 substrate and the slider surface. Negative values indicate protrusion above the slider surface. Chalcogenide concentration in the melt was 3.1 wt.% for all ternary layers and 0.25 wt.% for all binaries

Sample	3ary			2ary		BaF_2 depth	BaF_2 max	BaF_2 min	Result
	Tl wt.%	T_n °C	T_l °C	T_n °C	T_l °C	μm	μm	μm	
13b		638	641	473		6	32	-24	good
17b		635	639	468		-21	8	-47	scratched
35		623	626	491	496	11	14	8	good
36		629	633	484	498	3	12	0	good
37		621	625	484	496	7	20	-10	good
38	2	625	629	490	492	0	2	-2	good
39	2	623	626	481	490	23	67	0	poor wipe

Table 3.6: $PbTe/PbSe_{0.78}Te_{0.22}$ structures grown on (100)-oriented BaF_2 substrates using LPE. T_n and T_l are the nucleation and liquidus temperatures of the melt. BaF_2 depth, min, and max are the estimated average, minimum, and maximum clearance between the corners of the BaF_2 substrate and the slider surface. Negative values indicate protrusion above the slider surface. Chalcogenide concentration in the melt was 3.1 wt.% for all ternary layers. Binary layer in samples 44, 49, and 50 were doped with Tl.

Sample	3ary		2ary				BaF_2	BaF_2	BaF_2	Result
	T_n °C	T_l °C	z wt.%	Tl wt.%	T_n °C	T_l °C	depth μm	max μm	min μm	
41	625	629	5		624	629	8	30	0	adhesion
43	625	628	3		574	580	0	2	0	good
44	623	626	5	2	616	614	8	19	0	good
49	623	626	5	0.8	616	624	12	14	0	good
50	619	622	5	0.6	618	620	3	10	-2	good

3.2.4 $Pb_{0.90}Sn_{0.10}Se_{0.78}Te_{0.22}$ on $PbSe_{0.78}Te_{0.22}$

Eight two-layer $Pb_{0.90}Sn_{0.10}Se_{0.78}Te_{0.22}$-on-$PbSe_{0.78}Te_{0.22}$ structures were grown lattice-matched to the BaF_2 substrate. These are listed in Table 3.7. Sample 54, 55, and 56 incorporated a Tl doped quaternary layer and were contacted with evaporated Pb (on the ternary) and Au (on the quaternary). Current-voltage measurements between the contacts were made. No diode characteristic was seen in current-voltage measurements taken at room temperature. Samples 57, 59, and 60 were an attempt to obtain low temperature grown quaternary on the thinnest possible ternary. Pre-exposure to the ternary melt (sample 57) and a short 30 second growth from the ternary melt (sample 59) were both found insufficient for producing surfaces suitable for further growth. The ternary layer of sample 60 was grown for 90 seconds and allowed subsequent growth of a continuous quaternary layer. Samples 73 and 74 incorporated Tl in the lower ternary layer. Hall measurement of samples 60 and 74 were made. Results are given in Table 3.8.

A decrease in measured nucleation temperature is evident for the ternary and quaternary Tl-doped layers in Table 3.7. This lowering is somewhat reduced for the ternary layer of sample 74 due to a slight increase in chalcogenide concentration in the melt, compared to 73.

Table 3.7: $Pb_{0.90}Sn_{0.10}Se_{0.78}Te_{0.22}/PbSe_{0.78}Te_{0.22}$ structures grown on (100)-oriented BaF_2 substrates using LPE. T_n and T_l are the nucleation and liquidus temperatures of the melt. BaF_2 depth, min, and max are the estimated average, minimum, and maximum clearance between the corners of the BaF_2 substrate and the slider surface. Negative values indicate protrusion above the slider surface. Chalcogenide concentration in the melt was 3.2 wt.% for all ternary layers, except sample 74 which was 3.3 wt.%, and 1 wt.% for all quaternaries, except 73 and 74 which were 0.2 wt.% and 0.3 wt.%, respectively.

Sample	3ary			4ary			BaF_2 depth	BaF_2 max	BaF_2 min	Result
	Tl wt.%	T_n °C	T_l °C	Tl wt.%	T_n °C	T_l °C	µm	µm	µm	
54		625	628	3	509	512	29	50	8	poor wipe
55		624	627	3	505	511	36	48	23	good wipe
56		625	627	10	494	498	23	30	15	good wipe
57		626	629		516	520	11	15	0	cubes - discont.
59		624	628		515	519	5	9	2	discont - bad wipe
60		624	628		515	519	15	24	4	good wipe
73	3	615	619		407	412	0	0	0	many inclusions
74	3	618	620		435	444	15	35	0	good wipe

Table 3.8: Hall mobility, carrier concentration, and thickness of two double layer $Pb_{0.90}Sn_{0.10}Se_{0.78}Te_{0.22}/ PbSe_{0.78}Te_{0.22}$ samples measured at 300 K and 77 K. Samples were contacted using Au spots away from the edge of the sample.

Sample	$\mu_{77\,K}$ cm^2/Vs	$(p\text{-}n)_{77\,K}$ cm^{-3}	$\mu_{300\,K}$ cm^2/Vs	$(p\text{-}n)_{300\,K}$ cm^{-3}	d µm
60	151	-4.8×10^{20}	30	-3.8×10^{20}	4.5
74	47	-5.5×10^{21}	12	-6.9×10^{21}	4

3.2.5 *$PbSe_{0.78}Te_{0.22}$ on $Pb_{0.90}Sn_{0.10}Se_{0.78}Te_{0.22}$*

Three two-layer $PbSe_{0.78}Te_{0.22}$ on $Pb_{0.90}Sn_{0.10}Se_{0.78}Te_{0.22}$ structures were grown for planned optical pumping experiments. These are listed in Table 3.9. No measurements were performed on these structures.

Table 3.9: $Pb_{0.90}Sn_{0.10}Se_{0.78}Te_{0.22}/PbSe_{0.78}Te_{0.22}$ structures grown on (100)-oriented BaF_2 substrates using LPE. T_n and T_l are the nucleation and liquidus temperatures of the melt. BaF_2 depth, min, and max are the estimated average, minimum, and maximum clearance between the corners of the BaF_2 substrate and the slider surface. Chalcogenide concentration in the melt was 0.8 wt.% for all ternary layers..

Sample	4ary z wt.%	4ary T_n °C	4ary T_l °C	3ary T_n °C	3ary T_l °C	BaF_2 depth μm	BaF_2 max μm	BaF_2 min μm	Result
63	3	628	630	509	515	26	55	0	misweighed
64	3	607	611	509	514	6	5	6	poor growth
65	3.4	618	621	511	516	5	20	0	good

3.2.6 *$PbSe_{0.78}Te_{0.22}$ on $Pb_{0.90}Sn_{0.10}Se_{0.78}Te_{0.22}$ on $PbSe_{0.78}Te_{0.22}$ triple layers*

Three three-layer $PbSe_{0.78}Te_{0.22}$-on-$Pb_{0.90}Sn_{0.10}Se_{0.78}Te_{0.22}$-on-$PbSe_{0.78}Te_{0.22}$ structures were grown for laser fabrication. These are listed in Table 3.10. No follow-on experiments were performed with these structures.

Table 3.10: $PbSe_{0.78}Te_{0.22}/Pb_{0.90}Sn_{0.10}Se_{0.78}Te_{0.22}/PbSe_{0.78}Te_{0.22}$ structures grown on (100)-oriented BaF_2 substrates using LPE. T_n and T_l are the nucleation and liquidus temperatures of the melt. BaF_2 depth, min, and max are the estimated average, minimum, and maximum clearance between the corners of the BaF_2 substrate and the slider surface. Structures were prepared and grown identically and all displayed excellent growth and wipe-off.

Sample	3ary T_n °C	3ary T_l °C	4ary T_n °C	4ary T_l °C	3ary T_n °C	3ary T_l °C	BaF_2 depth µm	BaF_2 max µm	BaF_2 min µm	Result
51	625	627	515	519	473	478	20	30	10	excellent wipeoff
52	624	628	514	520	470	478	23	34	17	excellent wipeoff
58	626	629	515	520	568	474	24	26	20	excellent wipeoff

3.3 Discussion

The most striking result of the electrical measurements of LPE-grown IV-VI layers on BaF_2 (100) is their high carrier concentrations and low Hall mobilities. These compare poorly to previous results obtained in this lab and at MIT for nominally identical material [8]. In the most directly comparable case—undoped $PbSe_{0.78}Te_{0.22}$ single layers—the electron concentrations reported in Table 3.2 are greater than previous results by at least a factor of two. The highest value is greater by a factor of 45. Hall mobilities are lower, on average, by a factor of 10 for the results presented here. Since earlier measurements are self consistent—and consistent with values measured in bulk material—it is difficult to argue that the problem lies in earlier work. Explaining these differences is problematic; the earlier layers were grown in the same system using the same procedures as those reported here, and they were measured similarly.

There are two possible sources of error: inherent and measurement. Inherent error refers to compositional differences between the layers measured in this project and those measured earlier. Measurement error refers to problems contacting the layers and measuring the Hall mobilities and carrier concentrations. The suspected source of inherent error was a change in BaF_2 substrate vendor between the earlier work and that reported here. The quality of the substrate affects the quality of the epitaxy obtained. Many of the substrates used during this project displayed mosaic patterns, as exemplified by Figure 3.4. These are revealed during polishing due to the preferential dissolution of BaF_2 at the defects between misoriented crystalline regions of the substrate and result in poor overgrowth in the area. Randomly located defects also appeared as conical etch pits on the substrate surface. Spots of melt adhesion were noted on all $PbSe_{0.78}Te_{0.22}$ layers

grown on BaF_2 during this project. Trapped regions of Pb, known as melt inclusions, are believed to lie beneath the small balls of melt adhesion seen on $PbSe_{0.78}Te_{0.22}$ layers and extend to the surface defects. No verification of this hypothesis was made, however a correlation exists. The melt adhesion pattern of some grown layers closely paralleled the pattern of mosaics seen on substrates prior to growth. Also, Sample 77, a quaternary layer grown directly on BaF_2, displayed the highest surface quality and lowest number of melt adhesion spots of any layer. It also had the highest measured Hall mobility and lowest carrier concentration of any sample grown on BaF_2 and compared favorably with the earlier data for ternary samples. This improvement in layer quality may have been due to another change in BaF_2 vendor, improvements in substrate preparation, or improved epitaxy arising from addition of Sn to the melt. It is not possible to determine the cause of improved layer quality from available data.

Another source of compositional error is oxidation of the surface of the epilayer. As discussed in Appendix D, this can change the carrier concentration of a layer dramatically, especially those containing Sn. Unfortunately—for the purpose of explaining the high carrier concentrations—oxidation of IV-VI materials produces acceptors at the surface and would decrease the electron concentrations measured. In addition, previously reported layers would have suffered from oxidation as well: the difference between these measurements and those reported earlier cannot be explained away by oxidation.

Hall mobilities and electron concentrations measured for sample 15 (see Table 3.2) indicate a likely source of measurement error. Sample 15 was a single ternary layer. Of the ternary layers produced, it yielded the most reasonable data. The more interesting

result from 15, however, is the variation of measured mobility and electron concentration with contacting technique and contact placement. By moving the contacts from the middle region of the sample to the edges (15.a) and corners (15.b), a more than 40-fold improvement in measured Hall mobility was realized; measured electron concentration dropped 8-fold. While part of this variation could be explained by assuming that the region of sample 15 measured in cases 15.b and 15.a contained fewer inclusions and therefore produced more accurate measurements, it is likely that much of the variation was due to contact placement. In developing his Hall measurement technique, van der Pauw assumed that the contacts would be placed at the circumference of the sample and that they would be small relative to the measured layer. Both of these assumptions are violated by the array-of-spots contacting technique employed for measuring the majority of the samples, but not by measurement 15.b. It should be noted, however, that the samples measured at MIT were contacted differently and met the van der Pauw assumptions. Estimates of the expected error in measured Hall mobility due to contact placement predict a factor of two. Consistency of earlier measurements, using the array-contacting method, with the results obtained at MIT indicates that deviations from the van der Pauw assumptions, although possibly contributing, are not the primary cause of the observed error.

In addition to the problems just discussed, the majority of the structures grown contained multiple layers. This introduced additional uncertainty. Samples 60 and 74 were an attempt to obtain electrical data for the low temperature grown quaternary material expected to form the active region of an eventual DH laser structure grown on BaF_2. The ternary layer upon which the quaternary was grown was doped with Tl in an

effort to isolate the top layer for measurements. These structures also yielded unreasonably high values for carrier concentration.

Efforts to grow diode structures (samples 54, 55, and 56 in Table 3.8) also failed. Melt inclusions, theorized above, are thought to have shorted out the junction, which would produce results consistent with those measured.

Highest quality layers were produced toward the end of the BaF_2 (100) effort. These thin quaternary layers (samples 75 and 77 in Tables 3.3 and 3.4) were grown on substrates, prepared by an improved polishing technique, which displayed shallow uniform etch pits prior to growth. The peak-to-peak surface roughness of the resultant layers was less than 0.5 μm—compared to 2 to 3 μm for thicker layers grown on differently prepared substrates.

3.4 Conclusion

Electrical measurements of the layers grown on (100)-oriented BaF_2 yielded values inconsistent with earlier reports for similar material. It is believed that the discrepancy was caused by a change in substrate material and its effect upon subsequently grown epilayers. Mosaic patterns, indicative of polycrystalline material, and conically shaped etch pits randomly scattered over the substrate surface were observed on many substrates prior to epilayer growth. These features are thought to retard epitaxial growth and produce holes in the epilayer in which melt becomes trapped. These inclusions of melt alter the electrical properties of the layer, producing high carrier concentrations and low Hall mobilities.

Other sources of error were investigated but found insufficient to explain the large discrepancy between measured values and those reported earlier. In addition, these error

sources would have been present in earlier measurements producing a consistent skew, but no discrepancy.

3.5 References

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Chapter 4: MBE-grown IV-VI Structures on Si(111)

High quality IV-VI semiconductor layers can be grown by MBE on (111)-oriented Si using fluoride buffer layers [1, 2]. Electrical injection into these structures from the substrate would allow fabrication of diode lasers, but conduction must occur through a fluoride buffer which is presently required to obtain IV-VI epitaxy on Si. This chapter will review current versus voltage experiments that were performed to investigate the effects of (1) fluoride buffer layer thickness and (2) inclusion of a *p-n* homojunction made by varying chalcogenide concentration during MBE growth.

4.1 Procedure

Four structures were grown upon a Si(111) substrate by the MBE technique. Each comprised a CaF_2 buffer and PbSe epilayers. Two of these structures were grown on high resistivity *p*-type Si and two on low resistivity n^+-type Si. The structures on *p*-type Si were similarly grown, except that the CaF_2 layer thickness was 20 Å for one structure and 100 Å for the other. The two structures on n^+-type Si were grown with identical CaF_2 layers but one had a second layer of PbSe grown to form a *p-n* homojunction in the PbSe epilayers. A summary of the structures is provided by Table 4.1.

3" diameter silicon substrates were cleaned by the Shiraki method [3] followed by an HF dip. They were then loaded into an Intevac Gen II MBE system and heated to 1000 °C for 30 minutes prior to growth to remove the Shiraki-grown oxide.

4.1.1 Structures on high resistivity p-type silicon (111)

Two *n*-PbSe/CaF_2 structures were grown on high resistivity *p*-type silicon (resistivity 17-18 Ωcm at 300 K). The structures and growth procedures were similar—the principal

Table 4.1: Summary of IV-VI on Si(111) structures grown for current versus voltage measurements

Sample Number	Si type	CaF_2 thickness Å	PbSe layer 1 thickness µm	type	PbSe layer 2 thickness µm	type
W189	*p*	100	2.6	*n*		
W195	*p*	20	2.6	*n*		
W209	n^+	50	2.2	*p*		
W211	n^-	50	2.2	*n*	2.2	*p*

difference being the thickness of the CaF_2 buffer layer. Growth of sample number W189, shown in Figure 4.1, began with deposition of 100 Å of CaF_2 at a substrate temperature of 700 °C. CaF_2 growth rate was estimated to be 8.7 Å min^{-1} from a beam equivalent pressure (BEP) of 4.34 x 10^{-8} Torr. This estimate was based—as were those for all other layers presented here—on the measured BEP, the value of which had been previously correlated to growth rate by observing RHEED intensity oscillations for layers grown under similar conditions. Deposition of 2.6 μm of PbSe followed at a substrate temperature of 310 °C and an estimated growth rate of 135 Å min^{-1}, obtained from a BEP of 1.34 x 10^{-6} Torr.

Growth of sample number W195, shown in Figure 4.2, began with deposition of 20 Å of CaF_2 at a substrate temperature of 700 °C. CaF_2 growth rate was again estimated to be 8.7 Å min^{-1} from a BEP of 4.4 x 10^{-8} Torr. Deposition of 2.6 μm of PbSe—broken into two steps this time—followed from a BEP of 1.36 x 10^{-6} Torr. The first 1500 Å was grown at a substrate temperature of 300 °C and the remainder at 280 °C, both at a rate of 135 Å min^{-1}.

4.1.2 Structures on conductive n^+-type silicon (111)

Two structures were grown on conductive n^+-type silicon (resistivity 1-4 x 10^{-3} Ω cm at 300 K). Both structures incorporated a 50 Å layer of CaF_2 and a 2.2 μm layer of PbSe grown with additional Se flux, but one also contained a 2.2 μm layer of PbSe grown without additional Se. Growth of sample number W209, shown in Figure 4.3, began with deposition of 50 Å of CaF_2 at a substrate temperature of 680 °C. CaF_2 growth rate was estimated to be 11 Åmin^{-1}. The BEP was 5.0 x 10^{-8} Torr. Deposition of 2.2 μm of PbSe

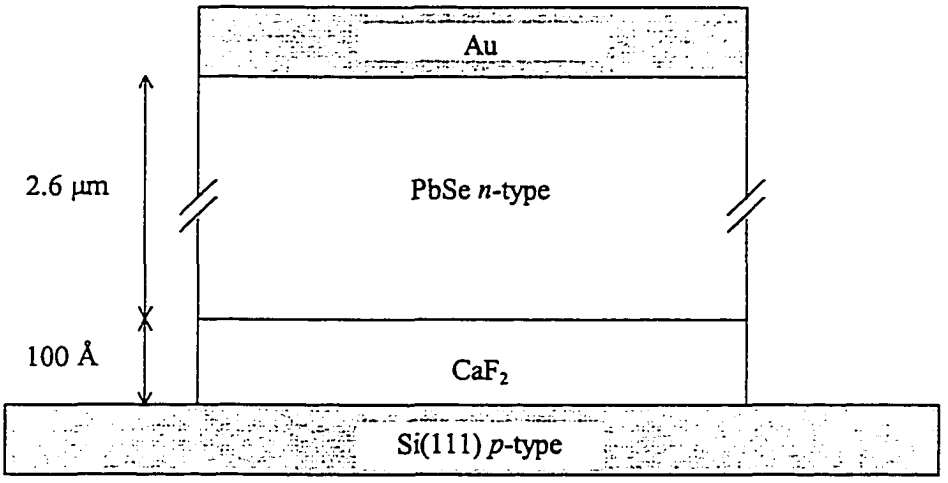

Figure 4.1: Cross-sectional schematic of sample number W189, a "*p-n* heterojunction" containing a thick intervening layer of CaF_2.

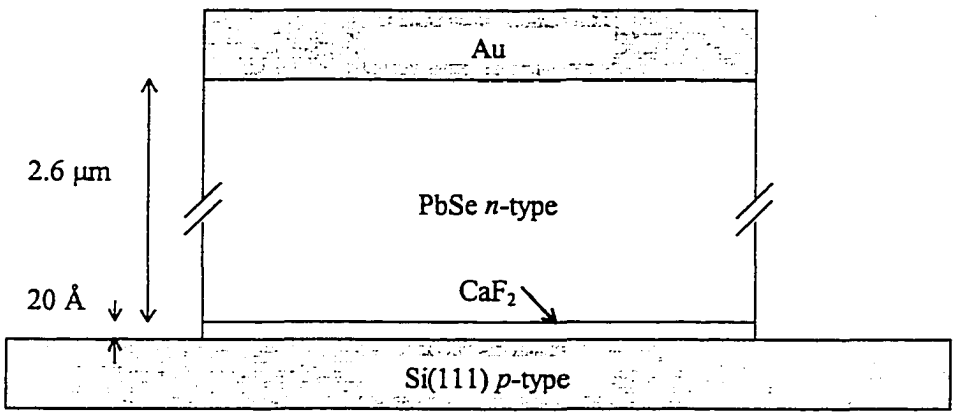

Figure 4.2: Cross-sectional schematic of sample number W195, a "*p-n* heterojuction" containing a thin intervening layer of CaF_2.

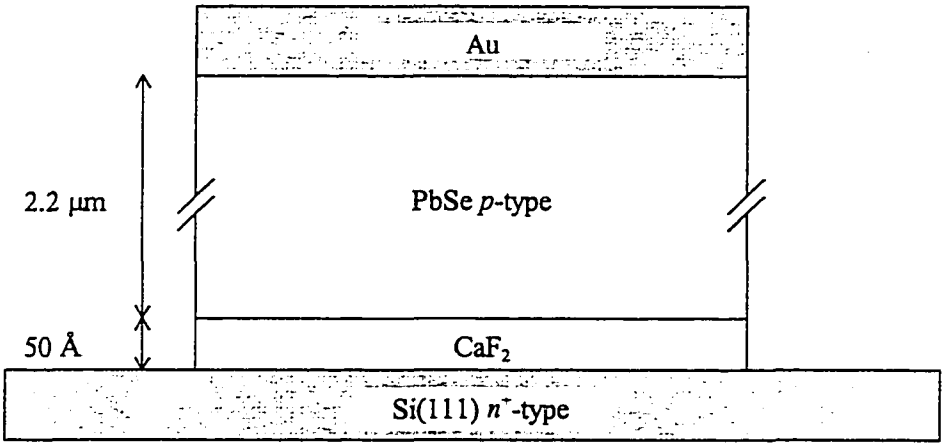

Figure 4.3: Cross-sectional schematic of sample number W209, a single PbSe layer grown on Si(111) using a CaF_2 buffer.

followed at a substrate temperature of 280 °C and a PbSe BEP of 1.3 x 10^{-6} Torr. An EPI, Inc. valved-cracker provided excess Se vapor at a BEP of 4.15 x 10^{-9} Torr. The PbSe growth rate was estimated to be 125 Å min^{-1}.

Growth of sample number W211, shown in Figure 4.4, began with deposition of 50 Å of CaF_2 at a substrate temperature of 680 °C and BEP of 5 x 10^{-8} Torr. CaF_2 growth rate was estimated to be 11 Å min^{-1}. Deposition of 2.2 μm of PbSe followed at a substrate temperature of 280 °C and an estimated growth rate of 125 Åmin^{-1}. BEP from the PbSe source was 1.31 x 10^{-6} Torr. The Se source was shuttered. A second 2.2 μm layer of PbSe was grown with the same PbSe BEP, but the Se source was open and provided a BEP of 4.0 x 10^{-9} Torr. An unexpected shut-down of the cryo-pumps during MBE growth of the second PbSe layer caused an interruption of growth after 0.6 μm had been deposited; the layer was completed the following day. Estimated growth rate was again 125 Å min^{-1}, ignoring any effects of growth interruption.

4.1.3 Contacting and measurement procedures

Each wafer was cleaved to produce samples suitable for further processing. Epilayer surfaces were electroplated with Au using a commercially prepared solution (Pure Gold SG-10, Transene Co., Rowley, MA). Photoresist was spun onto the metallized epilayer surface at 6000 RPM and exposed through a contact mask to define an array of 400 x 400 μm^2 squares. After the photoresist was developed, mesas were formed by etching through the Au, PbSe, and CaF_2 epilayers in a 95:5 $HBr:Br_2$ solution for 10 to 15 seconds, depending upon the PbSe thickness. Residual photoresist was removed with acetone and the samples were rinsed with methanol.

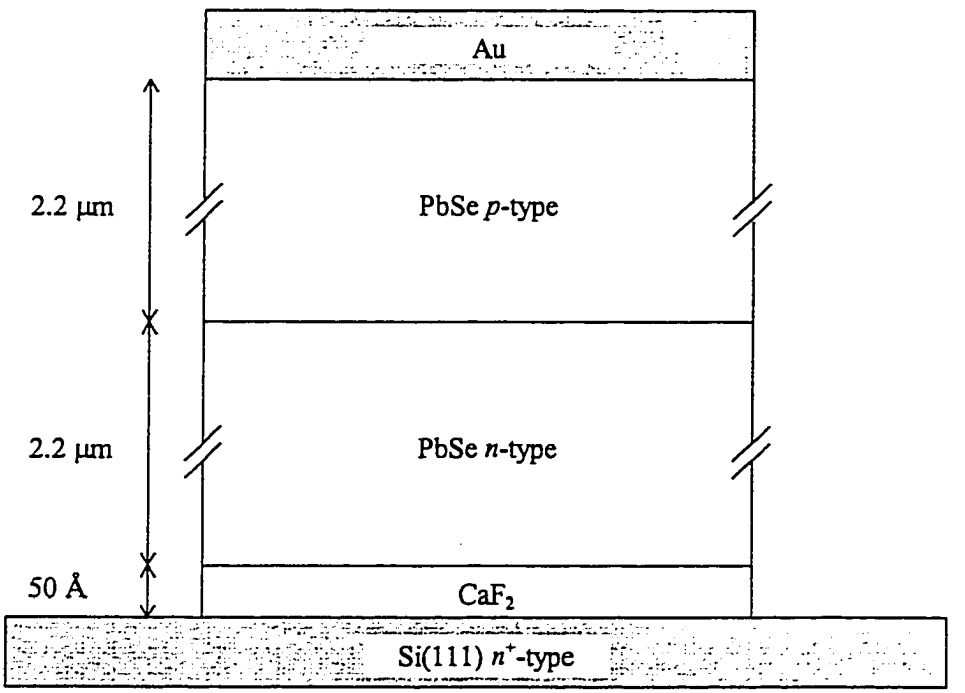

Figure 4.4: Cross-sectional schematic of sample number W211, a PbSe homojunction grown on Si(111) using a CaF_2 buffer.

Contact to the Au surface was made by press fitting a small In ball—which had been previously formed on the end of a thin Au wire—onto the mesa with the aid of a PTFE pencil. The substrate backside was coated with Ag paint and mounted to an Au-coated Cu plate. This assembly was mounted onto a cold head and the surrounding chamber was evacuated. Current versus voltage measurements of the samples were taken over a wide range of temperatures—from 30 K to as high as 395 K. Sample temperature was varied by a Helix Technologies closed-cycle helium compressor and a 25 W resistive heater, stabilized by a LakeShore LS805 temperature controller. A silicon sensor diode monitored the temperature.

Three electrical configurations were used to characterize the structures. The first—referred to below as the unshielded configuration—consisted of a Keithley 224 current source, a Keithley 195A voltmeter, and GPIB-based computer control for acquiring and displaying the current versus voltage measurements. This arrangement was used to characterize samples numbered W195 and W209. Appendix E contains a listing of the QuickBASIC program, IV.BAS, which was used to control the system. The second—shielded—configuration employed a Hewlett-Packard HP4140B voltage-source / picoammeter and revised computer control with temperature data logging. The electrical cabling and the sample mount area on the cold head were also reconfigured to provide greater electrical and optical isolation than supplied by the unshielded system. C++ source code and class listings for the DOS commands used to acquire, HPIV.EXE, and display, PLOT.EXE, the current versus voltage and temperature data are also provided in Appendix E. Samples numbered W189, W195 and W211 were characterized with the shielded system.

Sample number W195, as noted above, was characterized with both the shielded and unshielded configurations. Additionally, an intermediate configuration was used for this sample. In this arrangement, the sample mount had been reworked to provide electrical and optical isolation, but the electronics and control software had not yet been upgraded.

4.2 Results

4.2.1 Structures on highly resistive p-type silicon (111)

The current-voltage data obtained for W189, which contained a 100 Å thick CaF_2 layer, are shown in Figure 4.5 for three different temperatures. Voltage was applied relative to the Au contact, so that positive voltage in this figure—and all others in this sub-section—corresponds to a forward bias across the "*p-n* heterojunction" formed by the substrate and epilayer. A large shift in turn-on voltage can be seen with variation in temperature. Reverse bias breakdown voltage is more than 30 V.

Using the intermediate measurement configuration, similar curves were obtained for W195 and are shown in Figure 4.6. The forward bias region displays more abrupt turn-on at room temperature than observed in sample W189. A more substantial shift in turn-on voltage with respect to temperature is also apparent in W195. Breakdown voltage in reverse bias is reduced to 12-14 V, compared to greater than 30 V for sample W189. Expanding the forward bias region to examine the shift in turn-on voltage more closely provides Figure 4.7. At 259 K, the current is seen to have a sharp turn-on at about 0.5 V. As the structure is cooled, the curve bends over at higher currents until approximately 200 K is reached, indicating the likelihood of competing conduction mechanisms.

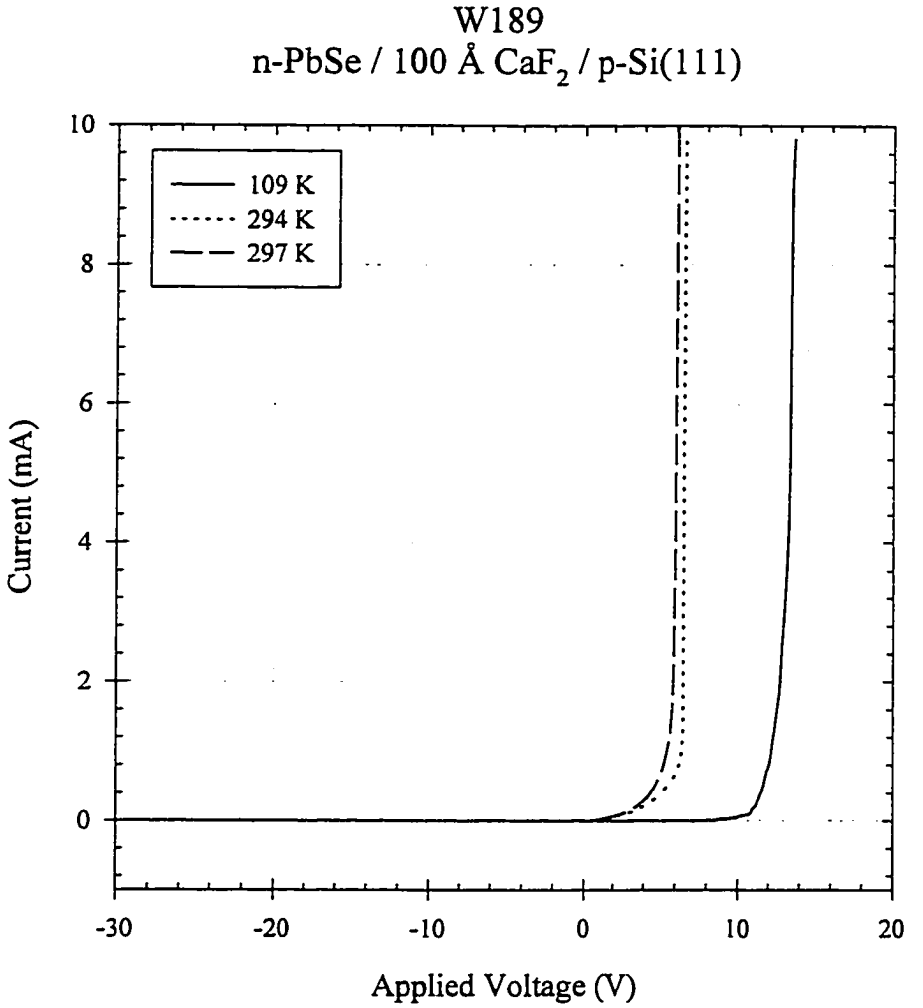

Figure 4.5: Current versus voltage curves for sample number W189, a "*p-n* heterojunction" containing an intervening layer of 100 Å thick CaF_2. Bias is expressed relative to the PbSe epilayer, so that positive bias in the figure corresponds to positive bias across the "*p-n* heterojunction". These forward and reverse bias curves were taken using the shielded measurement configuration.

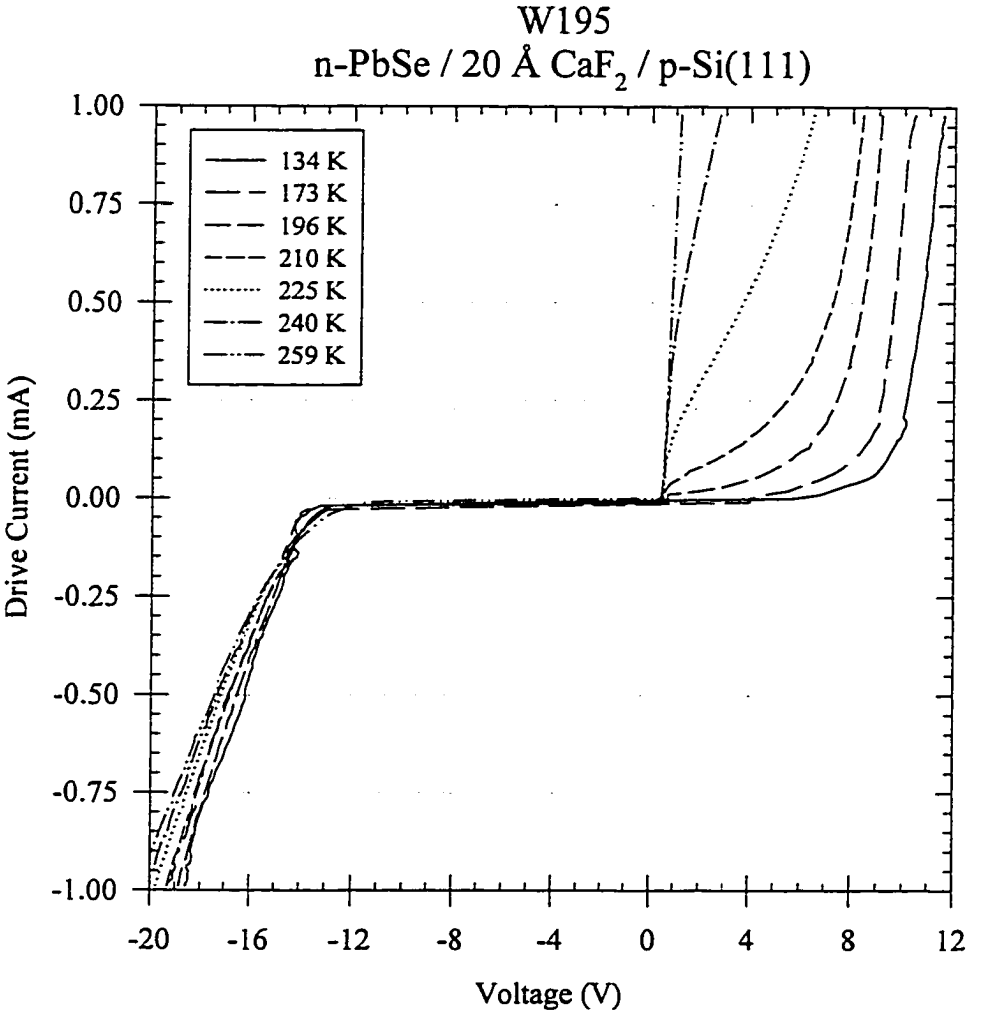

Figure 4.6: Current versus voltage curves for sample number W195, a "*p-n* heterojunction" containing an intervening layer of 20 Å thick CaF_2. Bias is expressed relative to the PbSe epilayer, so that positive bias in the figure corresponds to positive bias across the "*p-n* heterojunction". These forward and reverse bias curves were taken using the shielded configuration, but the electronics and control software had not yet been upgraded.

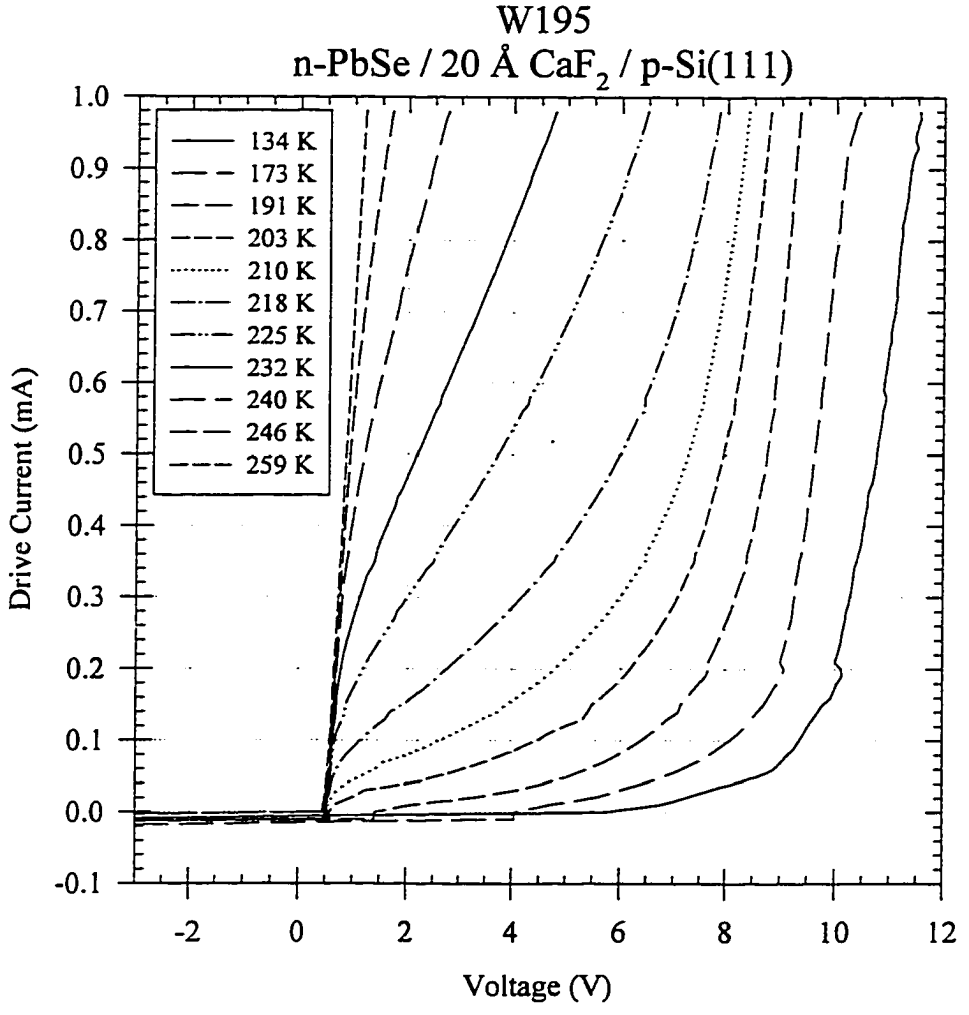

Figure 4.7: Current versus voltage curves for sample number W195, a "*p-n* heterojunction" containing an intervening layer of 20 Å thick CaF_2. Bias is expressed relative to the PbSe epilayer, so that positive bias in the figure corresponds to positive bias across the "*p-n* heterojunction". These forward bias curves were taken using the shielded configuration, but the electronics and control software had not yet been upgraded.

4.2.2 *Structures on conductive n^+-type silicon (111)*

Current-voltage curves obtained for samples W209 and W211 manifest fewer features. For these structures, voltage was applied relative to the substrate, resulting in positive bias across the "*p-n* heterojunction" of W209 and the *p-n* homojunction of W211. W209, which contained a 50 Å CaF_2 layer and a single *n*-type PbSe layer, produced the curves shown in Figure 4.8. A monotonic decrease in blocking voltage—in both the forward and reverse directions—occurred as the temperature was raised. The greatest shift in the curves takes place between the 170 K and 300 K measurements. This range roughly corresponds to the 173 K to 259 K range covering the majority of the much larger voltage shifts observed in Figure 4.6 of sample W195.

Measurement of W211 produced the curves shown in Figure 4.9. W211 also contained a 50 Å CaF_2 layer, but two PbSe layers were present: an *n*-type layer nearest the substrate and a *p*-type layer uppermost.

4.3 *Discussion*

4.3.1 *Structures on highly resistive p-type silicon (111)*

Examining the current-voltage curves of samples W189 and W195, shown in Figures 4.5 and 4.6, presents the difficulty of explaining the large shift in forward bias turn-on voltage with temperature. The current measured at low forward bias in W195 increases dramatically as the temperature increases. Schottky emission in the CaF_2 is consistent with this tendency. Other basic conduction processes in insulators have the opposite—or negligible—temperature dependence or a linear current-voltage response [4]. Attempts to model the forward conduction characteristic of W189 or W195 using an expression for voltage and temperature dependence of Schottky emission [4]

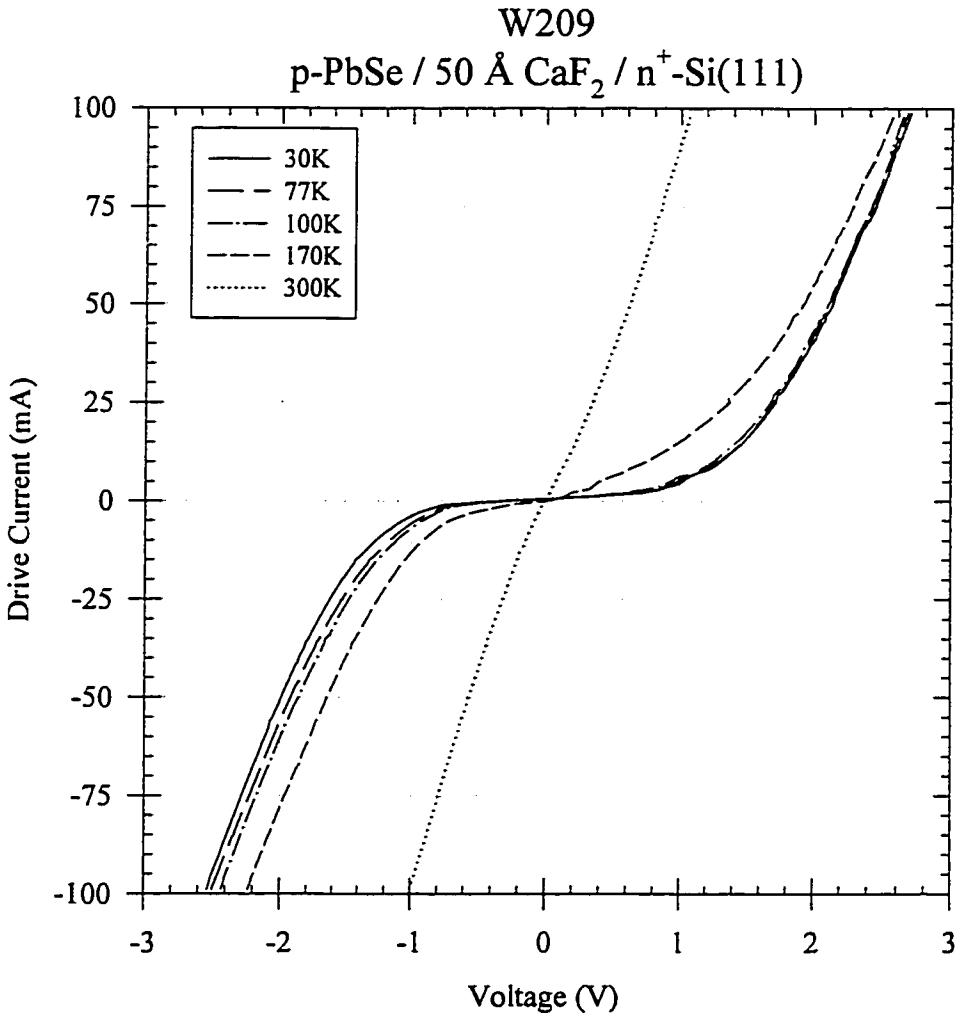

Figure 4.8: Current versus voltage curves for sample number W209, a single layer of PbSe grown on low resistivity Si(111) with a 50 Å thick CaF_2 buffer. Bias is expressed relative to the Si substrate. Full forward and reverse bias curves taken in the unshielded system are shown. The resistance of the sample at 300 K is approximately 10 Ω, corresponding to an expected resistance of 1.6 Ω for a 1 cm^2 injection area.

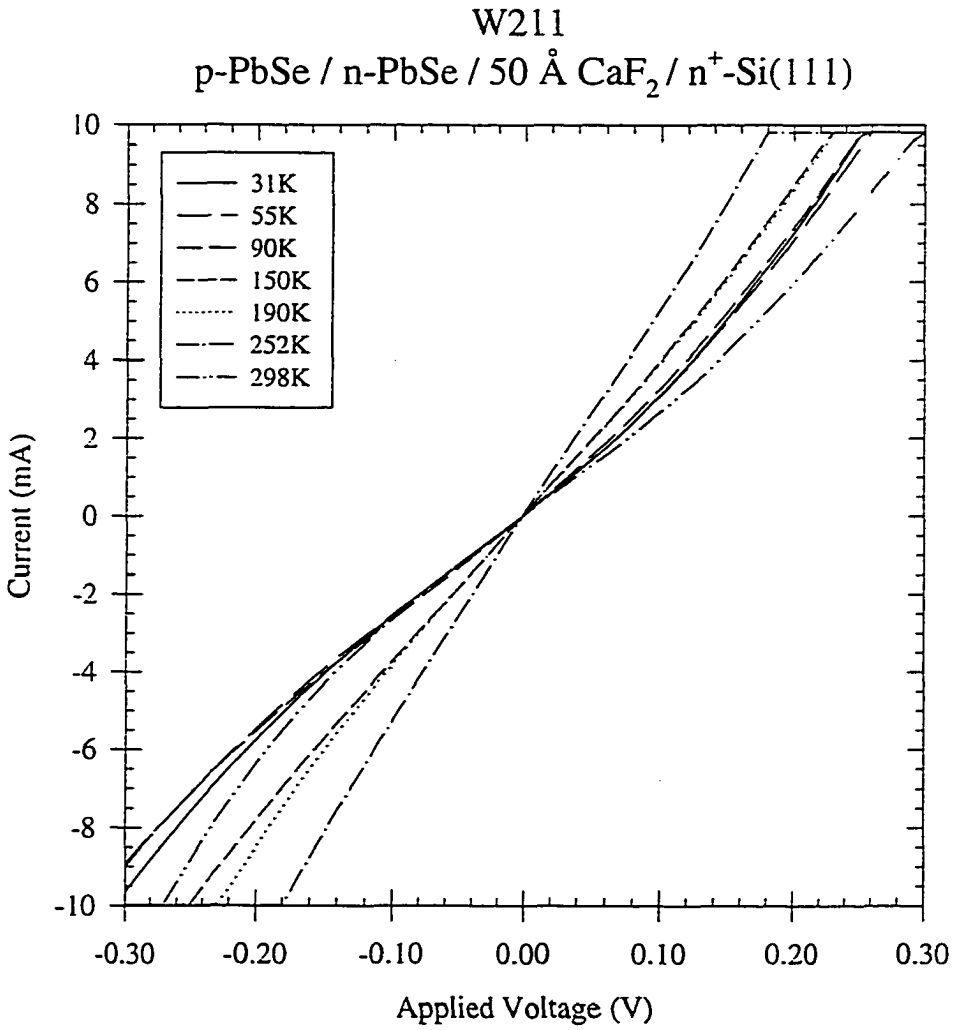

Figure 4.9: Current versus voltage curves for sample number W211, a double layer of PbSe grown on low resistivity Si(111) with a 50 Å thick CaF_2 buffer. Bias is expressed relative to the Si substrate. Full forward and reverse bias curves taken in the unshielded system are shown. The resistance of the sample at 300 K is approximately 18 Ω, corresponding to an expected resistance of 2.9 Ω for a 1 cm^2 injection area.

$$J \sim T^2 \exp\left[\frac{+a\sqrt{V}}{T}\right]$$

failed to account for the 0.5 V room temperature turn-on voltage in W195 and could not replicate the large curve shifts observed in either sample. In this equation, J is the current density and a is a positive constant dependent upon the dielectric constant and thickness of the insulator.

Current conduction must occur through the CaF_2 or—less intuitively—around it. It is interesting that the vapor pressure of H_2O drops from 1360 to 0.5 mT over this same temperature range [5]—a 2700-fold drop. At one time, it was thought that water-vapor-influenced air-breakdown around the perimeter of the device mesa might account for the observed shifts. However, repeated pumping and flushing of the system with dry N_2—to decrease the influence of water vapor upon the measurements—failed to produce any noticeable change in the observed temperature-induced shifts.

The role of tunneling upon conduction through the CaF_2 buffer was also investigated. Phonon-assisted tunneling probability for electrons in the PbSe layer is proportional to the population of electrons and available phonons meeting the energy and momentum conservation requirements for crossing the barrier. Since the PbSe layer is expected to be *n*-type degenerate, the population of available electrons near the PbSe conduction band edge should vary little with temperature. CaF_2's change in phonon population may be estimated from the Bose-Einstein equation [6],

$$F(\nu,T) = \frac{1}{\exp(h\nu/kT) - 1}.$$

Assuming a phonon energy of 0.042 eV—which is obtained from the separation between the zero-phonon and first Stokes-shifted absorption peaks seen in photoluminescence measurements performed on epitaxial CaF_2 grown on Si—the CaF_2 phonon poplation is calculated to increase 6.7-fold between 134 K and 259 K. The probability of phonon state occupancy, F, at 134 K is approximately 0.0265, indicating that phonons having an energy of 0.042 eV are readily available even at the lower temperture. Phonon availability is not expected to be a limiting factor to tunneling of electrons through the CaF_2 barrier. However, the tunneling probability is also proportional to the population of available states—holes at the appropriate energy—in the Si. From the measured resistivity of the Si substrate, the Fermi level may be placed 0.3 eV above the valence band. The population of holes in the valence band may then be calculated from [7]

$$p_o = \frac{\alpha T^{\frac{3}{2}}}{1+\exp\left(\frac{E_F - E_v}{kT}\right)},$$

where α is a constant incorporating the hole effective mass. A 10^5-fold increase in available state population is calculated for the Si substrate as its temperature changes from 134 K to 259 K. This increase in the number of Si valence band holes is a more likely candidate for explaining the majority of the temperature-related shift observed in the current-versus-voltage curves for W189 and W195.

Band diagrams for samples W189 and W195 are presented in Figures 4.10 and 4.11. Several assumptions were required in order to develop them. First, the effect of the CaF_2 buffer layer upon the band alignments was neglected. While the offset in the conduction band energy between CaF_2 and Si has been measured to be 2.2 eV [8], no similar study of the CaF_2 / PbSe interface has been performed. It was not possible to use the PbSe and Si

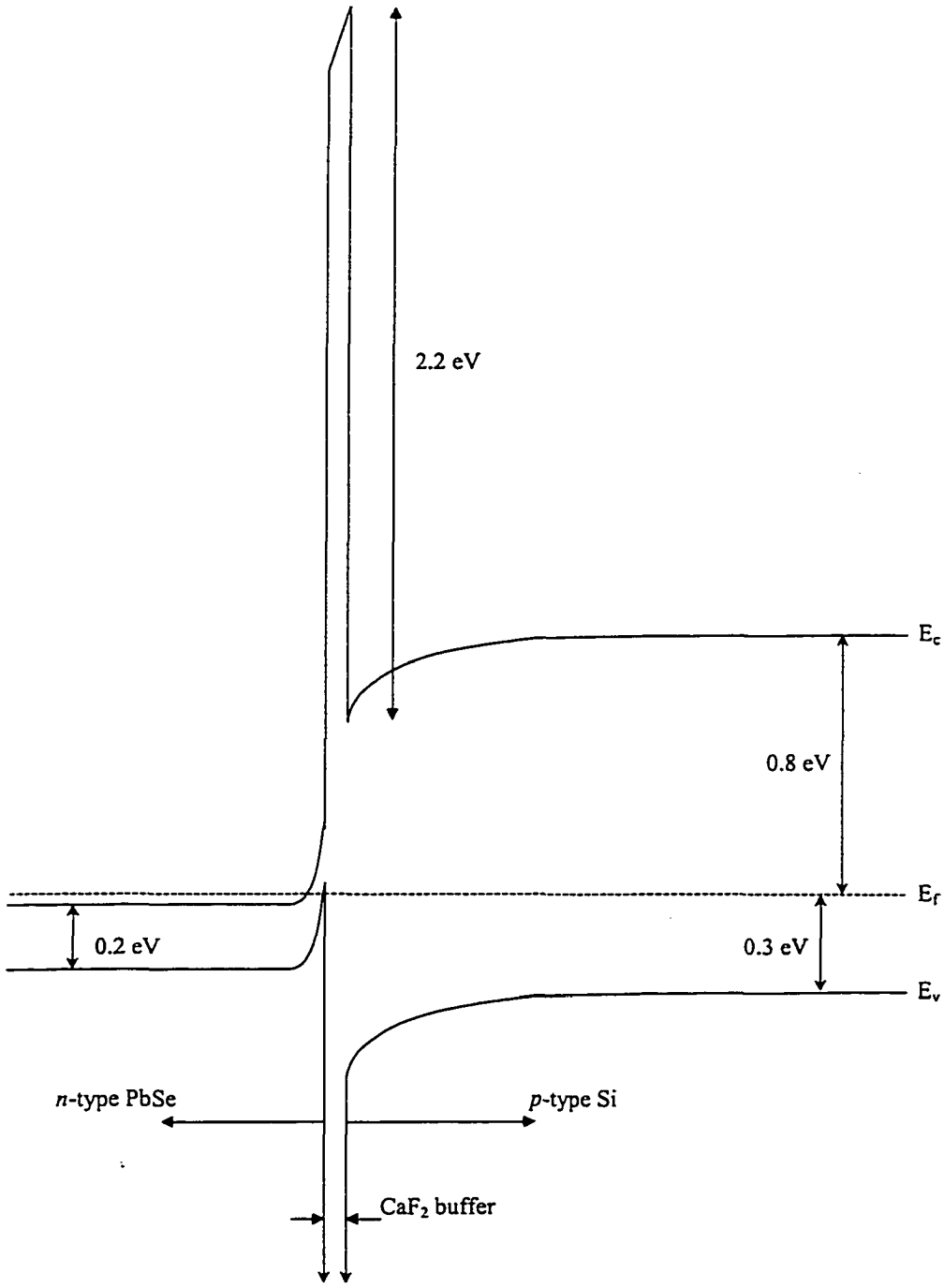

Figure 4.10: Proposed band diagram for sample W189, a "*p-n* heterojunction" containing a thick intervening layer of CaF_2. The suspected effect of the CaF_2 layer is seen in the conversion of the *n*-type PbSe to *p*-type near the PbSe/CaF_2 interface. Band alignment offsets due to differences in electron affinity have been ignored in this diagram.

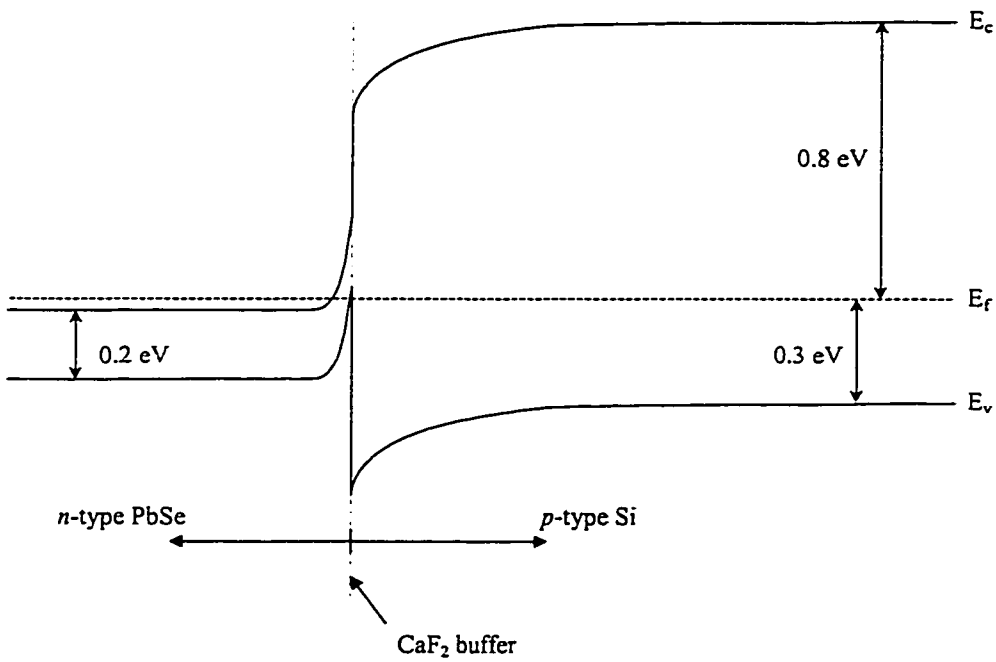

Figure 4.11: Proposed band diagram for sample W195, a "*p-n* heterojunction" containing a thin intervening layer of CaF_2. The CaF_2 layer is not shown in the diagram, but its suspected effect upon the PbSe layer is seen in the conversion of the *n*-type PbSe to *p*-type near the PbSe/CaF_2 interface. Band alignment offsets due to differences in electron affinity have been ignored in this diagram.

conduction band offsets, relative to CaF_2, to determine the band alignments for the system. For lack of a better estimate, the offset between the PbSe and Si conduction bands was taken to be equal to the offset between the PbSe and Si valence bands. Second, the PbSe bands were assumed to have been "pre-bent" by the influence of the CaF_2 interface. Studies of the growth of PbTe on BaF_2 [9] indicate that the resulting PbTe layer is always *p*-type. This was attributed to the existence of defects at the PbTe / BaF_2 interface which act as acceptors. For this reason, the PbSe was assumed to be *p*-type at the PbSe / CaF_2 interface and the band offsets between the PbSe and Si were split evenly based upon this placement. Third, the CaF_2 layer was assumed to be sufficiently thin that it did not affect current flow through the structure of W195—where it is 5 times thinner than in W189. It is represented as a dashed vertical line in Figure 4.10 as a reminder of its existence, but it is otherwise ignored.

It should be noted that the figures are not to-scale horizontally. An estimate of the extent of the depletion region into each layer of samples W189 and W195 may be obtained from [7]

$$E_o = -\frac{q}{\varepsilon_{no}} N_d x_{no} = -\frac{q}{\varepsilon_{po}} N_a x_{po}$$

$$W = x_n + x_p$$

$$V_o = -\tfrac{1}{2} E_o W$$

to give

$$E_o = \left[\frac{2qV_o}{\left[\frac{\varepsilon_n}{N_d} + \frac{\varepsilon_p}{N_a} \right]} \right]^{\frac{1}{2}}$$

or

$$E_o = 17.2 \times 10^3 V_0^{\frac{1}{2}} \text{ Vcm}^{-1} \tag{4.1}$$

$$x_{po} = 1.12 V_o^{\frac{1}{2}} \mu\text{m} \tag{4.2}$$

$$x_{no} = 393 V_o^{\frac{1}{2}} \text{ Å} \tag{4.3}$$

upon substitution of the appropriate values ($\varepsilon_n = \varepsilon_{PbSe} = 207\varepsilon_o$, $N_d = N_{PbSe} = 5 \times 10^{17}$ cm^{-3}, $\varepsilon_p = \varepsilon_{Si} = 11.8\varepsilon_o$, $N_a = N_{Si} = 1 \times 10^{15}$ cm^{-3}). V_o is the contact potential, E_o is the electric field at the interface, N is the ionized dopant concentration, ε is the dielectric constant, W is the total depletion width, and x is the depletion extent into each layer. If V_o is assumed to be about 0.5V, then the depletion region then extends 0.79 μm into the Si and 278 Å into the PbSe. (This calculation ignores the likely influence of acceptors generated in the PbSe by defects near the CaF_2 / PbSe interface [9], but still gives a feeling for the relative magnitudes.)

Comparison of the curves for W189 and W195 show that W189 lacks a sharp turn-on at room temperature. This is attributed to the greater thickness of the CaF_2 layer in W189. The temperature dependence of the turn-on is believed to arise primarily from the change in carrier concentration in the lightly-doped silicon substrate. As the temperature falls from 259 K to 134 K, the estimated hole concentration falls by a factor of 10^5 and the electron concentration falls by a factor of 10^{14}. This dramatically decreases the conductivity of the substrate and limits current flow through the device on its surface.

4.3.2 Structures on conductive n^+-type silicon (111)

Samples W209 and W211 were grown with identical CaF_2 layers, to allow the effects of including a *p-n* homojunction in W211 to be separated from the effects of CaF_2 layer

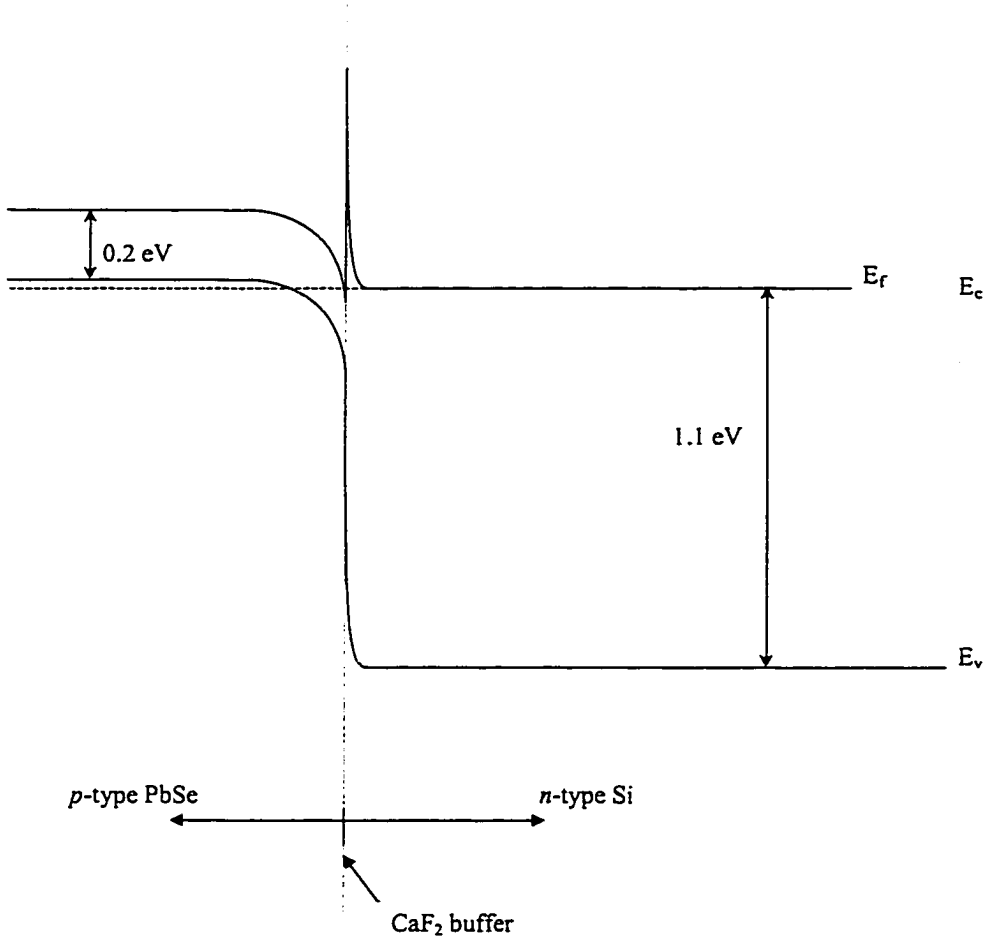

Figure 4.12: Proposed band diagram for sample W209, a "*p-n* heterojunction" containing an intervening layer of CaF_2. The CaF_2 layer is shown in the diagram as a dashed vertical line. Band alignment offsets due to differences in electron affinity have been ignored in this diagram.

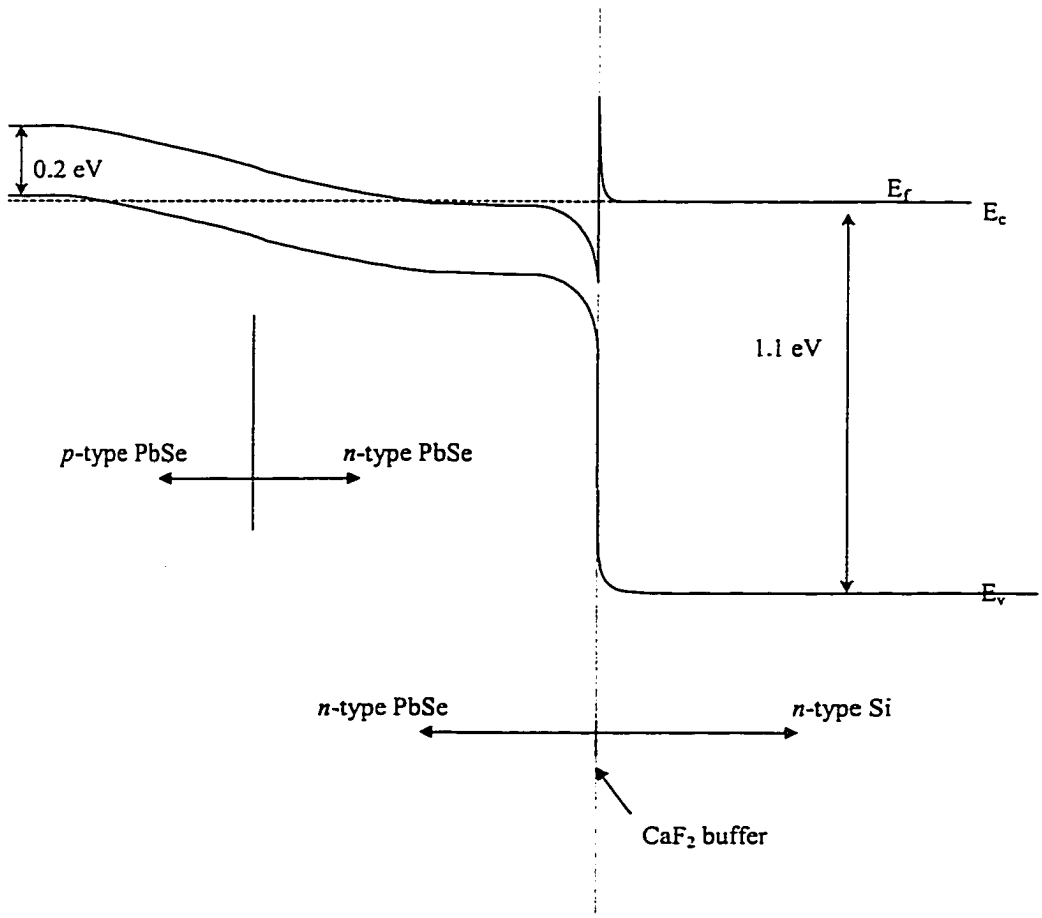

Figure 4.13: Proposed band diagram for sample W211, a *p-n* homojunction grown on n^{++} Si with an intervening buffer layer of CaF_2. The CaF_2 layer is shown in the diagram as a dashed vertical line. Band alignment offsets due to differences in electron affinity have been ignored in this diagram.

thickness. No evidence of a *p-n* homojunction is visible in the I-V plot in Figure 4.9, even at 31 K. However, a nearly ohmic response was obtained near room temperature for both samples. Making assumptions similar to those made for samples W189 and W195 produced the band diagrams shown in Figures 4.12 and 4.13. The placement of the PbSe bandgap in the middle of that for Si resulted in a thin *n*-type layer near the CaF_2 / PbSe interface of Figure 4.12, even with the acceptor doping expected from the CaF_2 induced defects [9]. In Figure 4.13, the additional doping is represented by the raising of the Fermi level higher into the PbSe conduction band near the PbSe / CaF_2 interface.

An estimate of the extent of the depletion regions into the PbSe and Si layers near the CaF_2 interface in samples W209 and W211 may be obtained by repeating the calculation in the previous section. In the case of W209, $\varepsilon_p = \varepsilon_{PbSe} = 207\varepsilon_o$, $N_a = N_{PbSe} = 5 \times 10^{17}$ cm^{-3}, $\varepsilon_n = \varepsilon_{Si} = 11.8\varepsilon_o$, and $N_d = N_{Si} = 3 \times 10^{19}$ cm^{-3}. These numbers result in equations parallel to (4.1)-(4.3):

$$E_o = 93.5 \times 10^3 V_o^{\frac{1}{2}} \text{ Vcm}^{-1} \tag{4.4}$$

$$x_{no} = 2.03 V_0^{\frac{1}{2}} \text{ Å} \tag{4.5}$$

$$x_{po} = 2140 V_0^{\frac{1}{2}} \text{ Å} \tag{4.6}$$

If one assumes that the difference in conduction band energy between the PbSe and Si away from the CaF_2 interface is representative of the contact potential, then depletion region extends 0.9 Å into the Si and 957 Å into the PbSe. Although the calculated values should not be interpreted to be the actual extent of the depletion regions in the two layers—the 0.9Å distance for Si is much too small to assume, as the derivation of the above equations does, that the electric field in the Si is continuous—they do indicate that

the majority of the depletion region extends into the PbSe and that the depletion region in the Si is extremely thin. This would allow carriers to easily pass through the Si conduction band barrier shown in Figures 4.12 and 4.13. The symmetry observed in the electrical measurements of W209 and W211 (Figures 4.8 and 4.9, respectively) is not easily explained in terms of the band diagrams in Figure 4.12 and 4.13. One would expect to observe a 0.2 V forward-bias turn-on for electron injection directed from the substrate into the epilayers and a much larger reverse bias hold-off, at least at lower temperatures. Possible reasons for the lack of correspondence between the band diagrams and electrical measurements include the omission of electron affinity effects in the band diagrams, uncertainty of the true carrier concentrations in the PbSe, and the effects of localized heating of the device during measurement.

4.4 Conclusion

There were two questions which this research attempted to answer: (1) Can current be injected through a thin CaF_2 buffer and into an overlying structure? and (2) Can a PbSe *p-n* homojunction be formed by varying chalcogenide concentration during MBE growth?

The answer to question (1) is yes. Measurements upon W209 and W211 both indicated ohmic conduction at room temperature for the structures shown in Figures 4.3 and 4.4. Similar structures may be suitable for current injection into epitaxially grown devices on silicon if these structures can be modified so that their resistance is also low below room temperature. Results from measurements on samples W189 and W195 indicate that a heavily doped n^+ substrate provides a greatly reduced barrier to current flow, especially at lower temperatures, compared to a lightly doped *p*-type substrate.

This effect was observed in spite of the thicker fluoride buffer layer employed in the samples grown on n^+ silicon.

The answer to question (2) is no—or at least, not in this attempt. The layers making up W211 were an early attempt to produce a PbSe *p-n* homojunction. The consistency of obtaining *p*-type PbSe has improved as materials experience has been accumulated. In addition, *p*- and *n*-type dopants have been introduced for MBE PbSe growth. Both *p*- and *n*-type doped layers are now routinely grown by MBE, avoiding problems of inter-layer Se diffusion and reducing the urgency for an answer to this question.

4.5 References

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Chapter 5: LPE-grown IV-VI Structures on Silicon

Many groups have fabricated IV-VI lasers using molecular beam epitaxy (MBE) [1-4] and liquid phase epitaxy (LPE) [5-11] grown structures. Such lasers are also commercially available from Laser Photonics in Andover, Massachusetts and Laser Components, GmbH in Olching, Germany. These commercial lasers consist of structures grown on IV-VI substrates which are unavailable in large dimensions and are thermally resistive. (Thermal conductivities of PbSe and PbTe are 0.018 W/cmK [12] and 0.020 W/cmK [12], respectively. These values compare poorly with Cu (4.01 W/cmK [13])). The ability to grow high quality, crack-free PbSe on Si(100) will provide larger, lower-cost substrates and is an important step towards the fabrication of thermoelectrically cooled devices [14].

The (100) orientation of Si provides certain advantages over either (111) or (110). First, Si(100) based technology is more developed; the silicon processing industry prefers this orientation due to its lower density of traps at the Si/SiO_2 interface [15]. Second, device fabrication requirements of IV-VI based lasers favor growth on (100)-oriented substrates. PbSe cleaves preferentially along its {100} planes [16], producing faces parallel and perpendicular to each other and perpendicular to the epilayer surface; for PbSe grown on Si(111), the {100} planes are angled with respect to the epilayer surface, preventing Fabry-Perot cavity formation by cleaving.

Island growth, misorientation, and thermal stress induced cracking have hampered growth of continuous epilayers of IV-VI materials on Si(100). Although MBE growth procedures overcoming the problems of island growth and misorientation in the BaF_2/CaF_2 buffer layers have been developed [17], there have been no reports of crack-

free PbSe growth on this surface. This chapter discusses experiments which demonstrate that addition of an LPE-grown PbSe layer on MBE-grown PbSe/BaF_2/CaF_2 suppresses thermally induced cracking and produces continuous (100)-oriented PbSe layers on Si(100).

Parallel experiments also investigated LPE growth of IV-VI material on similar MBE-grown structures on Si(111) and showed pyramidal morphology during initial LPE growth, similar to that observed in LPE-grown PbSe layers on BaF_2(111) substrates [18]. These triangular pyramids coalesce and their tops flatten upon further growth, forming a quasi-planar surface covered with melt-trapping depressions.

5.1 Experiment

5.1.1 Growth on Si(100)

Epitaxial growth of PbSe on Si(100) proceeded in two phases: MBE growth of a thin PbSe layer on Si(100) using BaF_2 and CaF_2 buffer layers followed by LPE growth of a thick PbSe layer on the MBE-grown structure.

5.1.1.1 Molecular Beam Epitaxy Growth

Growth was performed on *p*-type Si(100) in an Intevac Gen II MBE system. Wafers were cleaned by the Shiraki method [19] prior to loading and heated to 1000 °C for 30 minutes in the growth chamber to remove the Shiraki-grown oxide. After oxide desorption, a 200 Å CaF_2 layer was grown while the wafer temperature was held at 580 °C. This was followed by a 3200 Å layer of BaF_2 (substrate temperature 580 °C), annealing at 800 °C for 3 minutes [17], and growth of an additional 1500 Å of BaF_2 (substrate temperature 700 °C). The final MBE layer was 1000 Å of PbSe (substrate temperature 260 °C) grown from a single PbSe effusion cell.

5.1.1.2 Liquid Phase Epitaxy Growth

The Si(100) wafer, with the MBE-grown layers, was cleaved along <110> directions to form 1 x 1 cm^2 squares, which were then used as substrates for subsequent LPE growth with no further preparation. Melt constituents, Pb and PbSe, were placed in a graphite boat and heated to 650 °C in a hydrogen atmosphere for approximately 2 hours to homogenize the melt. The furnace and boat used for the LPE growth are described elsewhere [20,21]. Chalcogenide concentration was set to 0.20 wt% based upon previously published phase equilibria data for PbSe [22]. Nucleation and liquidus temperatures for the melt were measured by observing the temperature for the initial formation of nuclei during cooling and dissolution of the last nucleus during warming. The furnace was then cooled to room temperature before being opened to introduce the substrate. Furnace temperature was subsequently kept below 500 °C to minimize the thermal stress applied to the MBE-grown epilayers. Growth was initiated by pulling the substrate under the melt at 2 °C above the measured nucleation temperature (near 470 °C) as the melt was being cooled at 2 °C per minute. The epilayer grew for 40 minutes, at which time growth was terminated by pulling the substrate out from under the melt. The furnace was turned off and the system allowed to cool to room temperature before being flushed with Ar and opened to atmosphere. The resulting structure is shown schematically in Figure 5.1.

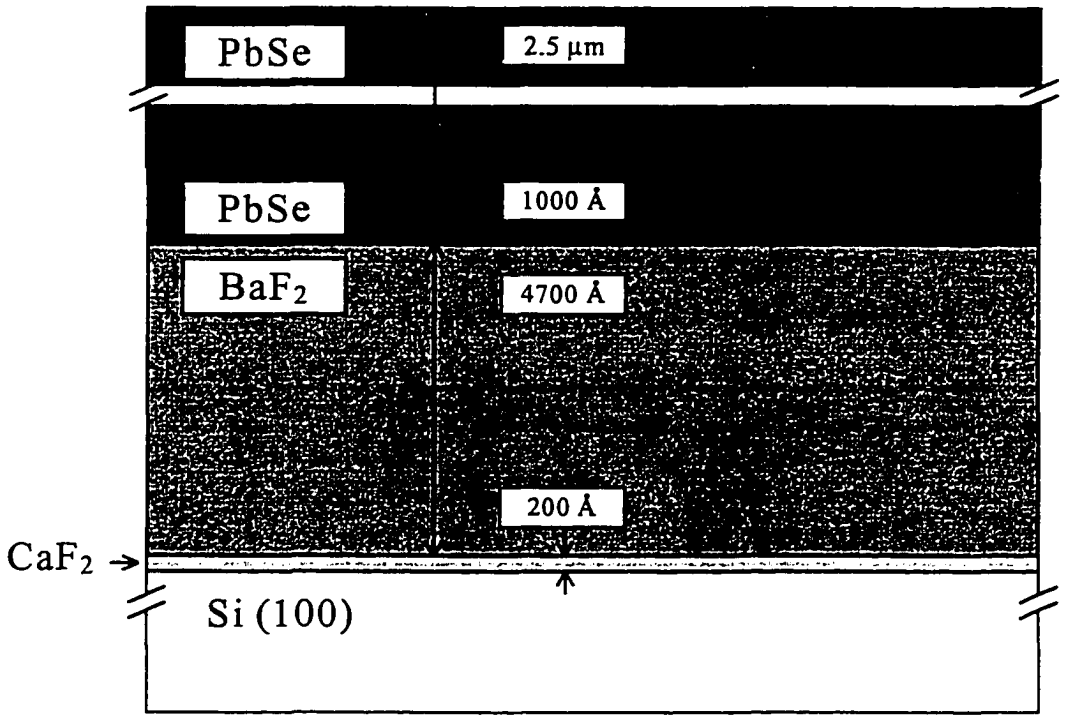

Figure 5.1: Schematic of a crack-free PbSe on Si(100) structure. 1000 Å of MBE-grown PbSe permits low temperature LPE growth of the uppermost 2.5 μm of PbSe.

5.1.2 Growth on Si(111)

Epitaxial growth of PbSe on Si(111) also proceeded in two phases: MBE growth of a thin PbSe layer on Si(111), using only a CaF_2 buffer, followed by LPE growth of a thick PbSe layer on the MBE-grown structure.

5.1.2.1 Molecular Beam Epitaxy Growth

Growth was performed on *p*-type Si(111) in an Intevac Gen II MBE system. Wafers were cleaned by the Shiraki method prior to loading and heated to 1000 °C for 30 minutes in the growth chamber to remove the Shiraki-grown oxide. After oxide desorption, a 100 Å CaF_2 layer was grown while the wafer temperature was held at 700 °C. CaF_2 growth rate was estimated to be 8.7 Å min^{-1} from a beam equivalent pressure (BEP) of 4.34 x 10^{-8} Torr. Deposition of 2.59 μm of PbSe followed at a substrate temperature of 310 °C and an estimated growth rate of 135 Å min^{-1}, obtained from a BEP of 1.34 x 10^{-6} Torr.

5.1.2.1 Liquid Phase Epitaxy Growth

The Si(111) wafer, with the MBE-grown layers, was cleaved along parallel {111} planes into 1 cm wide strips and then across the strips along parallel {110} planes to produce 1 x 1 cm^2 squares. These were used as substrates for subsequent LPE growth with no further preparation. Melt constituents, Pb and PbSe, were placed in a graphite boat, along with the substrate, and heated to 550 °C for approximately 2 hours to homogenize the melt. Chalcogenide concentration in the melt was set to 0.25 wt%. Growth was initiated by pulling the substrate under the melt at 2 °C above the measured nucleation temperature (near 480 °C) as the melt was being cooled at 2 °C per minute. The epilayer grew for 20 minutes, at which time growth was terminated by pulling the

substrate out from under the melt. The furnace was turned off and the system allowed to cool to room temperature before being flushed with Ar and opened to atmosphere. The resulting structure is shown schematically in Figure 5.2.

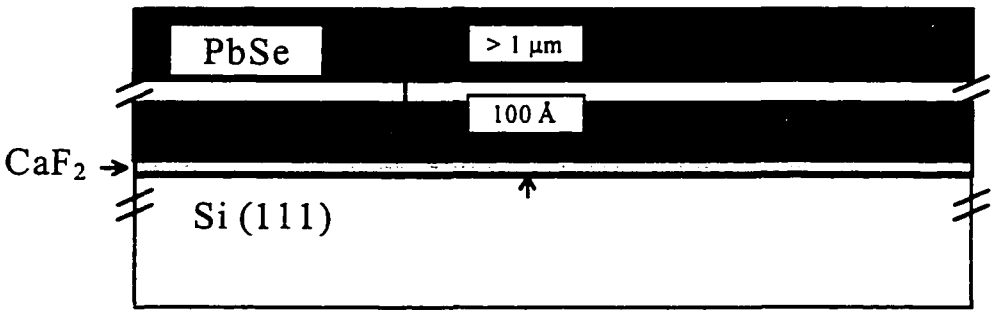

Figure 5.2: Schematic of a PbSe on Si(111) structure. 100 Å of MBE-grown PbSe permits low temperature LPE growth of the uppermost layer of PbSe.

5.2 Results

5.2.1 Growth on Si(100)

Optical Nomarski microscopy, scanning electron microscopy (SEM), contact mode atomic force microscopy (AFM), and high resolution x-ray diffraction (HRXRD) were used to examine the layers. Figure 5.3 shows a 80 x 80 μm^2 AFM scan of the surface of sample W113-1, an LPE-grown PbSe layer on (100)-oriented Si which was grown as described above. The image was obtained with a TopoMetrix Explorer AFM system operating in contact mode and shows the region to be crack-free. The scan indicated a peak-to-peak surface roughness of approximately 0.25 μm for the layer. Figure 5.4 is a similar scan of the sample after temperature cycling to 77 K. It shows (100)-oriented cracks spaced approximately 50 μm apart. An SEM cross-section of sample W113-1 after temperature cycling to 77 K, Figure 5.5, shows that cracks extend through the PbSe layer, perpendicular to its surface. The 2.5 μm layer thickness visible in the SEM micrograph was verified by a Tencor scan profiler.

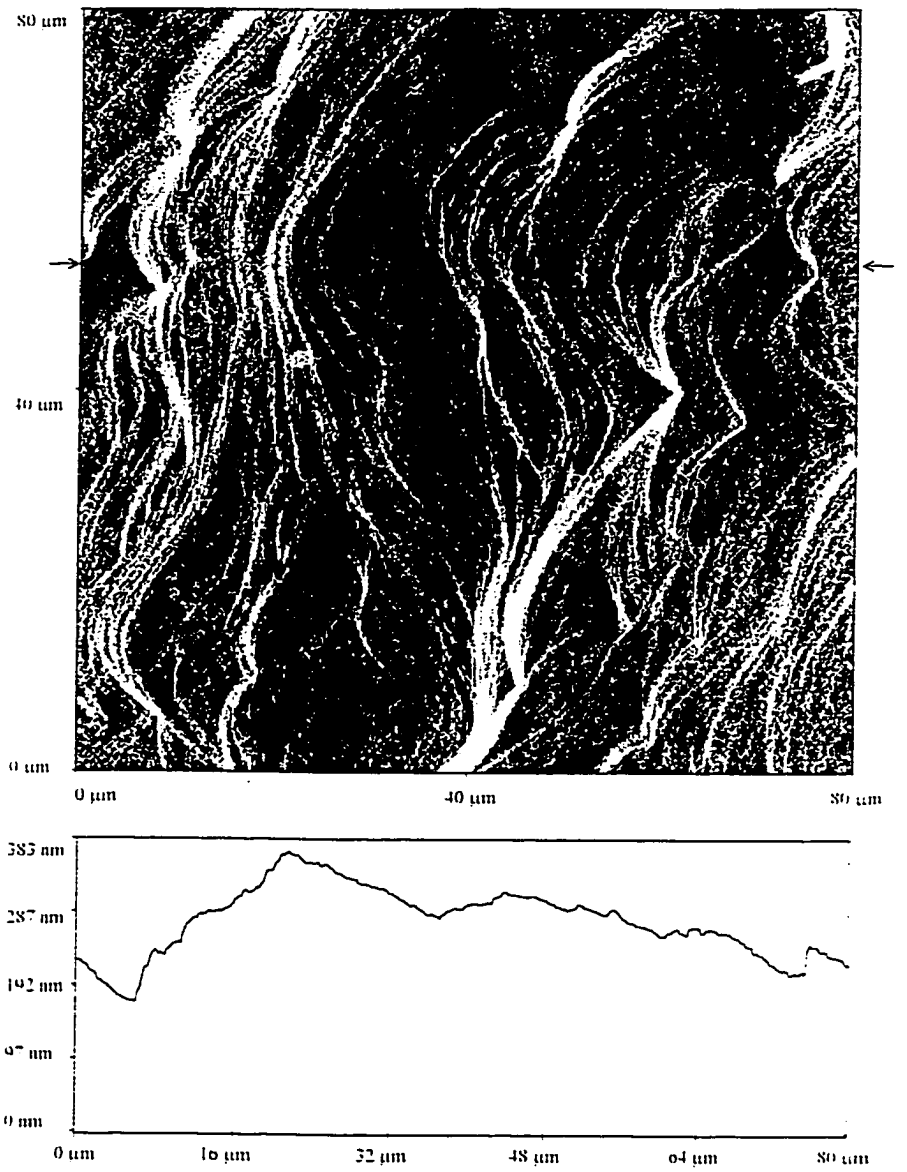

Figure 5.3: Contact-mode AFM scan of sample W113-1, an LPE-grown PbSe layer on Si(100) exposed to a minimum temperature of 300 K. To accentuate sample relief, the scan is displayed in a shadowing mode, simulating a light source on the left. A line scan, indicated by the arrows, shows a peak-to-peak roughness of about 200 nm and presents the true surface topography. The 80 x 80 μm^2 surface is free of cracks, inclusions, and melt adhesion.

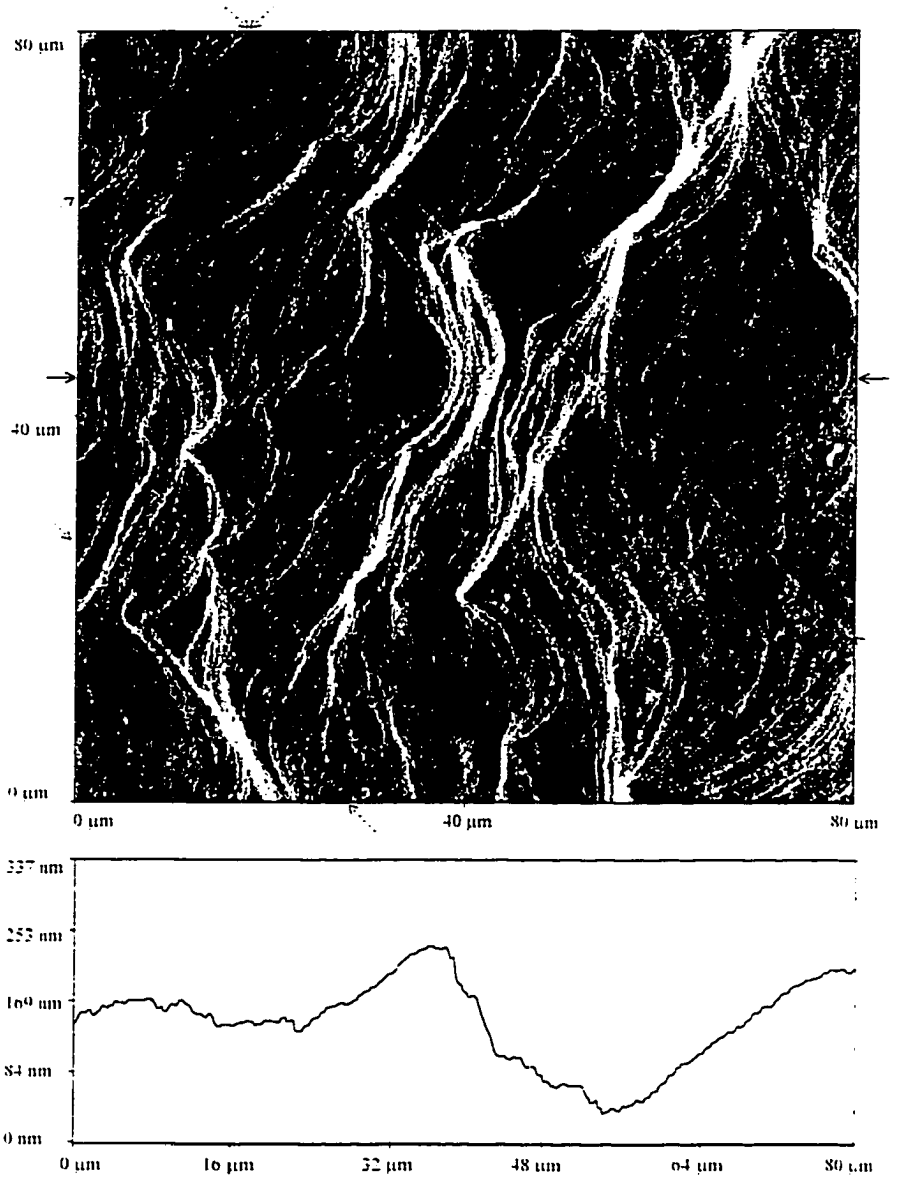

Figure 5.4: Contact-mode AFM scan of sample W113-1, an LPE-grown PbSe layer on Si(100), after cooling to 77 K and warming to 300 K. To accentuate sample relief, the scan is displayed in a shadowing mode, simulating a light source on the left. A line scan, indicated by the solid arrows, shows a peak-to-peak roughness of about 220 nm and presents the true surface topography. Two parallel (100)-oriented cracks, spaced by approximately 50 µm, and a (100)-oriented crack perpendicular to them are indicated by dotted arrows.

Figure 5.5: SEM micrograph of a cross-section of sample W113-1, an LPE-grown PbSe layer on Si(100) cleaved along one of its {111} planes, after cooling to 77 K and warming to 300 K. LPE-grown PbSe occupies the top side of the micrograph; the thin buffer layer structure is visible separating it from the Si substrate below. A crack having parallel (100)-oriented faces extends to the substrate surface.

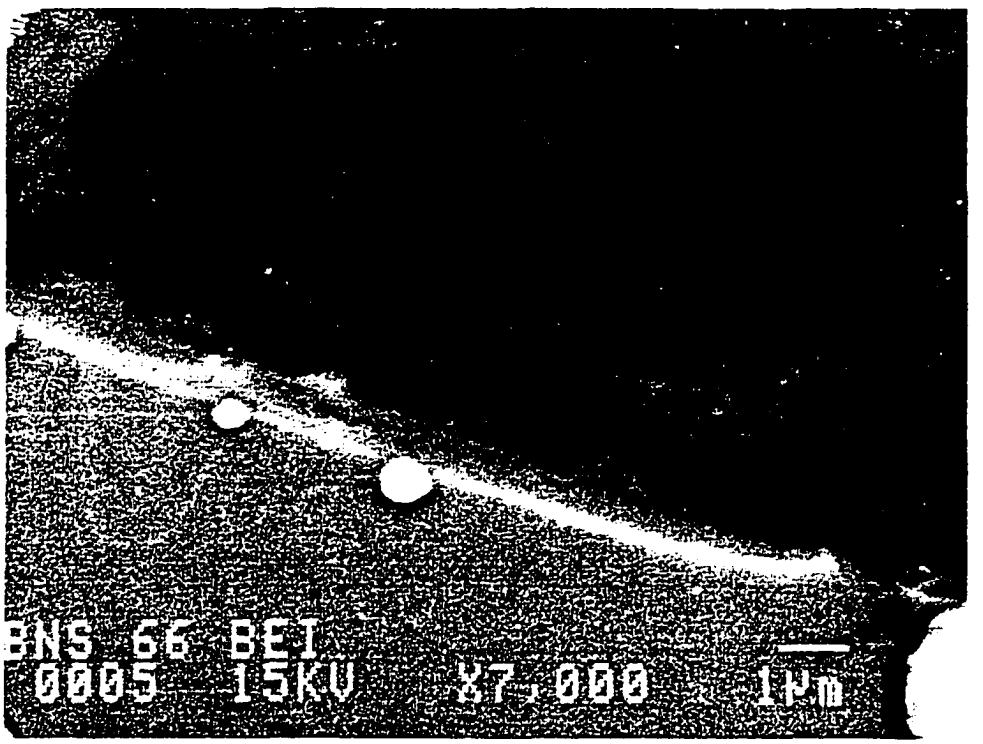

Figure 5.6: SEM micrograph of the LPE melt contact boundary of sample W113-B66. The surface of the cracked MBE-grown PbSe layer occupies the upper half of the micrograph. The surface of the uncracked LPE-grown PbSe layer is shown in the lower half. Small spheres of melt adhesion dot the boundary.

The SEM micrograph of sample W113-B66 in Figure 5.6 was taken at the boundary of the LPE melt contact and shows the surface morphologies of LPE-grown (lower half of photograph) and MBE-grown (upper half of photograph) layers. Since the horizontal well dimensions of the graphite boat are smaller than the substrate width, a portion of the substrate is left exposed, providing a comparison of the materials obtained by the two PbSe growth techniques. While approximately 10^6 cracks/cm^2 are visible in the MBE grown layer, no cracking is visible in the LPE-grown region. Optical Nomarski microscope observation of the cryogenically uncycled LPE-grown PbSe layer of this sample revealed three (100)-oriented cracks across the sample. It should be noted, however, that sample W113-B66 varied from the growth procedure described above by being inserted into the LPE furnace before homogenizing the melt. The cracking observed in this sample has been attributed to the higher temperature to which it was exposed prior to LPE layer growth. Sample W113-1 was not exposed to the high temperature homogenization step, and no cracks were observed by either optical Nomarski or AFM examination.

A Philips MRD four-bounce monochromator X-ray diffraction system was also used to investigate crystal quality. Both rocking curve and θ-2θ measurements about the symmetric (004) Bragg reflection were performed to separately assess PbSe epitaxial material quality with respect to mosaic tilt spread as well as inhomogeneous strain broadening (*d*-spacing variation) along the growth direction. Additionally, for selected samples, "reciprocal-space maps" (constant-diffracted-intensity contours in the reciprocal space diffraction plane) of the PbSe (004) peak were recorded. A representative reciprocal-space map is given in Figure 5.7. From the figure, it is evident (see inset) that

the diffraction peak is of considerably greater extent in reciprocal space along the in-plane directions than along the growth direction. The large in-plane peak width is most commonly attributed to mosaic spread while the growth direction peak broadening is, in general, a measure of both inhomogeneous strain and finite crystal coherence length effects along the growth direction, due to the presence of a high density of misfit-relieving threading dislocations, stacking faults, or other extended defects. In view of the large lattice mismatch (~1% for BaF_2 and PbSe, ~14% for Si and PbSe) between the PbSe layers and the substrate, this is not surprising, and, in fact, has been observed in other highly lattice-mismatched material system such as GaN on Al_2O_3 [22].

To better characterize these separate peak-broadening effects, a set of rocking curve scans, as well as θ-2θ scans (in both cases with a 0.45 mm receiving slit placed in front of the detector), were performed for each sample. The rocking-curve and θ-2θ scans correspond to profiling the PbSe (004) reciprocal-space feature of Figure 5.7 along its widest and narrowest aspects, respectively. In all cases, the θ-2θ scans yield narrow, Gaussian peaks with FWHM values ranging from 200-250 arcsec. On the other hand, rocking curve measurements of the same PbSe (004) reflections exhibit comparatively broader peaks with *exponential* tails. This latter observation suggests that the (004) planes of the PbSe layer are approximately exponentially distributed in angle over a small range of tilts (FWHM from ~ 600-1200 arcsec in our initial samples to as little as ~ 350 arcsec for W113-1 as epitaxial growth procedures became improved) about some mean value. As can be seen from Figure 5.7, the PbSe (004) peak is slightly displaced from the ordinate, indicating that the mean PbSe [004] (hence [001]) direction is *not* aligned

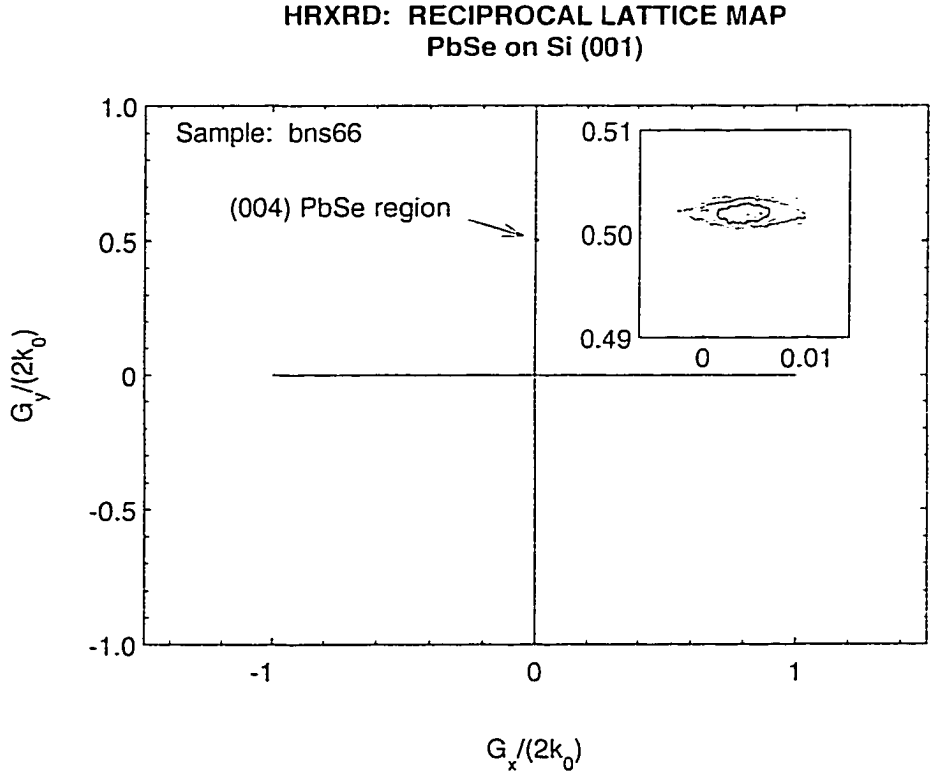

Figure 5.7: Reciprocal space plot of the (004) reflection of a PbSe(100) layer grown on Si(100) by LPE. The inset shows the shift of the PbSe (004) reflection to the right of the vertical axis, which has been aligned to the Si(100) substrate.

parallel to that of the substrate. In fact, HRXRD examination of the substrate shows that the nominally (001)-oriented Si substrates are actually slightly vicinal (off axis by ~ 0.85°), and that the mean PbSe [001] direction appears to be rotated by ~ 0.35° relative to that of the substrate in a direction toward the actual substrate normal. It is possible that this net rotation of the epitaxial structure occurs as an additional mechanism to (partially) accommodate the rather large epitaxial-substrate lattice mismatch; the origin of the rotation effect is still under investigation.

5.2.2 Growth on Si(111)

Optical Nomarski microscopy was used to examine two regions of sample Si111-2-480-n-1: the MBE-grown PbSe exposed to the LPE melt during substrate transfer and the LPE grown PbSe layer. No electrical measurements were performed due to the solidified melt, described below, that remained on the surface after growth. Figure 5.8 shows a 100 x 75 μm^2 region of MBE grown PbSe exposed to the melt after LPE growth. Small triangular pyramids decorate the MBE-grown PbSe surface. The pyramids all maintain the same orientation relative to the substrate. A few can be seen to have merged and all have rounded tops. Two lines, of what appears to be melt adhesion, run vertically across the micrograph.

Micrographs of the LPE-grown PbSe layer are shown in Figures 5.9 and 5.10. Figure 5.9 is a lower magnification picture showing a 1000 x 760 μm^2 area. The connected gray areas of the picture surround lighter and darker circular features. Magnification to 100 x 75 μm^2, in Figure 5.10, shows the flat connected areas more clearly. Focusing through the circular features indicated that they lie below the surface

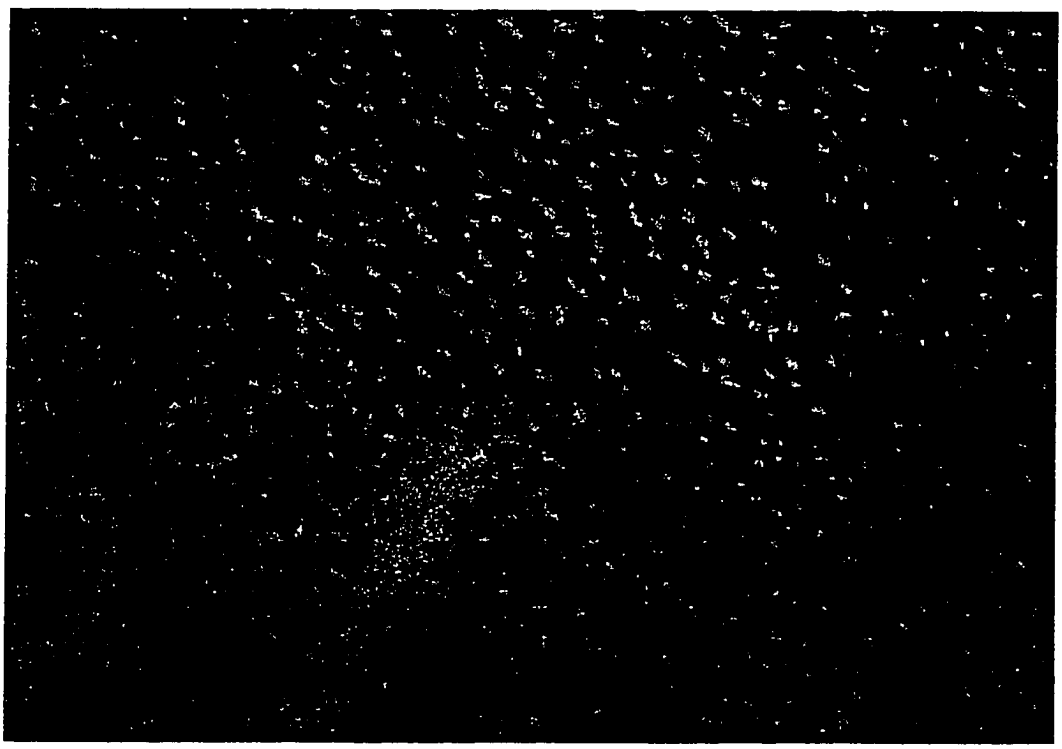

Figure 5.8: Optical Nomarski micrograph of the surface of sample Si111-2-480-n-1, an MBE-grown PbSe(111) surface exposed to an LPE melt during substrate transfer. The 100 x 75 μm^2 area contains triangular pyramids which are all oriented in the same direction. Rounding of the pyramid tops was observed through the microscope objective but is not easily visible in this reproduction. Two lines of probable melt adhesion run across the micrograph vertically.

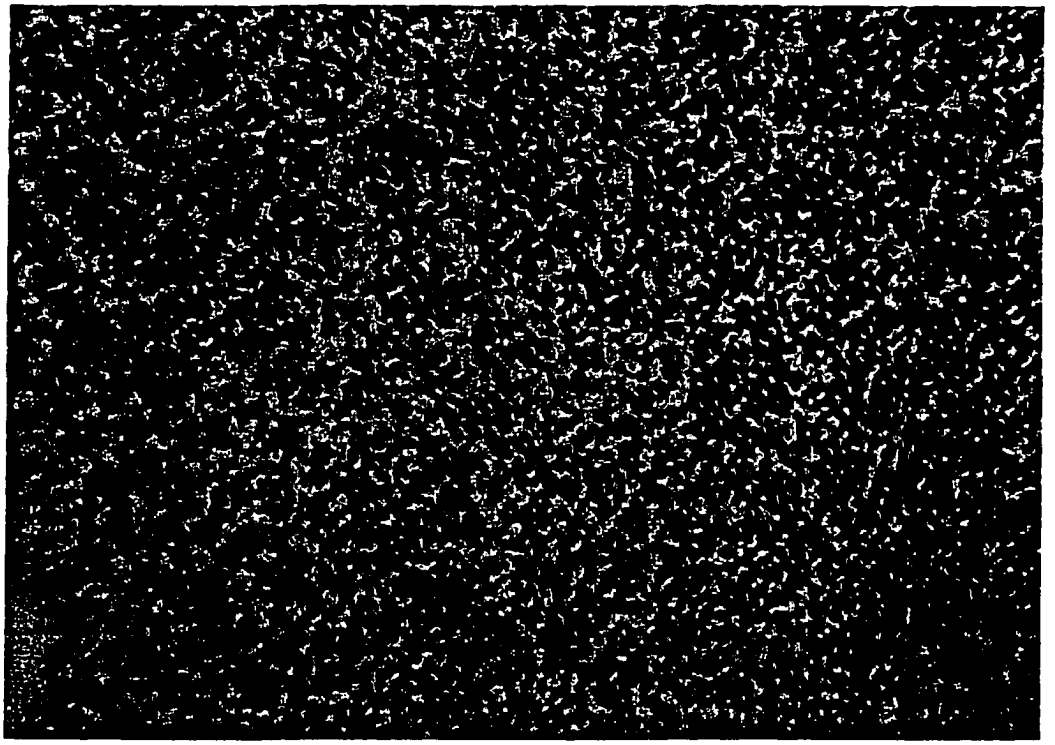

Figure 5.9: Optical Nomarski micrograph of 1000 x 750 μm^2 of sample Si111-2-480-n-1, an LPE-grown PbSe layer on Si(111). Gray regions surround lighter and darker circular features.

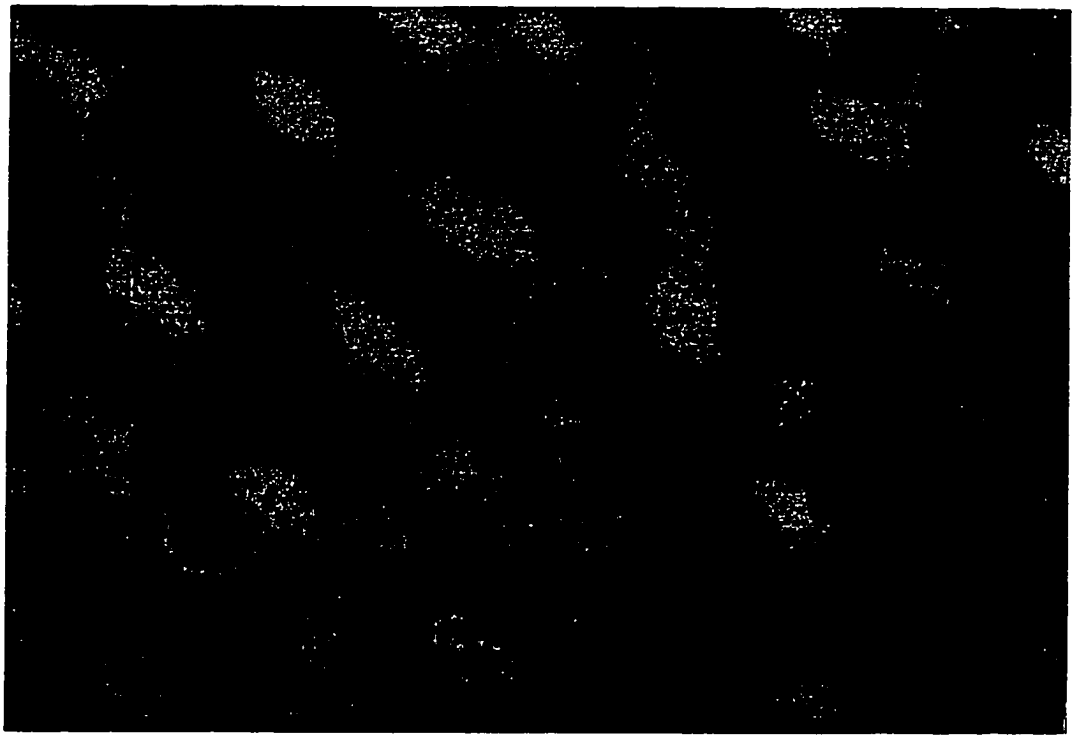

Figure 5.10: Optical Nomarski micrograph of 100 x 75 μm^2 of Si111-2-420-n-1, an LPE-grown PbSe layer on Si(111). The flat, connected gray regions surround depressions containing solidified melt. Three-fold symmetric arrays of lines were visible in the microscope objective but are not visible in this reproduction. These lines were oriented in the same directions as the intersection between the {100} faces of the triangular pyramids observe in Figure 5.8 and the MBE-grown PbSe(111) surface.

formed by the connected regions. The features are out of focus but many can be seen to contain droplets of solidified melt.

5.3 Discussion

Growth of CaF_2 (lattice parameter 5.46305 Å at 300 K [23]) on Si(100) using a two temperature process produces flat (100)-oriented CaF_2 layers in spite of CaF_2's tendency toward (111) faceting due to the lower surface energy of the (111) faces [24]. By following CaF_2 growth with BaF_2 (6.2001 Å [25]) growth, PbSe (6.1243 Å [26]) can be grown with much smaller lattice mismatch (1.2%) than growth directly on CaF_2. An additional benefit of this structure is that the incorporated BaF_2 layer is water soluble and can be used as a release layer, enabling epitaxial lift-off of structures from the silicon substrate [14].

The high density of cracks (approximately 10^6 cm^{-2}) in the MBE-grown PbSe is clearly caused by the large mismatch of thermal expansion coefficients between the Si substrate and the CaF_2, BaF_2, and PbSe layers. (The thermal expansion coefficients, at 300 K, are 2.6 x 10^{-6} K^{-1} for Si and 19.2-19.8 x 10^{-6} K^{-1} for the epilayers [27].) As the wafer cools from its final MBE growth temperature of 280 °C, the PbSe and fluoride buffer layers contract more rapidly than the silicon substrate, large tensile stress is generated in the layers, and cracks form. It is also possible that the MBE-grown PbSe is "cracked" when grown, due to pre-existing cracks in the BaF_2 surface caused by cooling from the BaF_2 growth temperature (700 °C) to the PbSe growth temperature (280 °C) and a failure of the PbSe to grow down the crack walls or bridge them.

The thermal expansion mismatch between the layers and substrate requires that the LPE growth temperature for the final PbSe layer be as close to room temperature as

possible. The MBE-grown PbSe allows this lower temperature LPE growth. Earlier studies of LPE growth of PbSe on BaF_2(100) substrates demonstrated that growth must begin near 625 °C [18], which corresponds to the formation of a BaSe reaction layer [28] that can catalyze PbSe nucleation [29]. Attempts to grow PbSe on BaF_2/CaF_2/Si(100) without the MBE-grown PbSe layer required such elevated temperatures and resulted in poor layer quality with inclusions, a large number of cracks, and melt adhesion. The limiting factor for low temperature LPE growth of PbSe is the chalcogenide concentration in the melt. Nucleation temperature of the melt decreases to the melting point of Pb (327 °C) as the concentration of Se is reduced. However, attempts to grow PbSe from melts with a chalcogenide concentration less than about 0.20 wt% resulted in discontinuous layers, probably due to Se solute depletion between growing nuclei on the substrate surface. At this concentration, the LPE growth initiation temperature is still 210 °C higher than the growth temperature for the MBE-grown PbSe. It is hypothesized that this provides a smooth, compressed surface of MBE-grown PbSe during LPE growth, as long as the temperature is not too high. In which case, the MBE-grown PbSe is damaged by the excessive compression and perhaps buckles.

The primary dislocation glide plane system in PbSe is along the {100} planes in the <110> directions [16]. For growth on (100)-oriented substrates, these planes are perpendicular to the surface, have zero valued Schmid factors and are incapable of relieving the thermally induced stress. However, higher order glide planes may exist which have non-zero Schmid factors and are able to relieve the stress. Previous work by Maissen [30] has detected slip lines in (100)-oriented MBE-grown PbSe on Si using STM. It is possible that the high concentration of Se vacancies (10^{18}-10^{19} cm^{-3}) [31] in

the LPE-grown PbSe provides a mechanism for dislocation climb [32], which relieves the stress or interacts with dislocations moving along the higher order glide planes, making them more mobile. This is a possible explanation for successful growth of crack-free PbSe layers on (100)-oriented Si.

For LPE growth of PbSe on Si(111), the resultant layer displayed a large concentration of melt trapping depressions. Rounding off of the pyramid peaks, seen in Figure 5.8, may be a precursor to planarization of the LPE grown layer. The depressions observed in Figures 5.9 and 5.10 are believed to result from failure to completely fill the areas between nucleated pyramids as the growth proceeds. The apparent flatness of the connected region seen in Figure 5.10 argues for a planarization mechanism, flattening out the pyramid peaks and preferentially filling the areas between them. It is possible that this is a consequence of the low starting temperature of the LPE growth, but no attempt was made to investigate this hypothesis. A slower cooling rate during LPE growth might assist in reducing the density of depressions observed. The three-fold symmetric arrays of parallel lines seen through the microscope objective when taking the micrograph of Figure 5.10 are produced by the mismatch in lattice expansion coefficient between the Si substrate and the PbSe epilayer. They correspond to the intersection of the {100} planes of the PbSe and the exposed (111) surface. These planes also form the sides of the triangular pyramids observed in Figure 5.8.

5.4 Conclusion

High quality (100)-oriented PbSe layers have been grown by LPE on Si(100) using an MBE-grown PbSe/BaF_2/CaF_2 buffer. The MBE-grown PbSe allows for lower temperature LPE growth and reduced stress in the system compared to that required for

growth without the PbSe. This results in crack-free (100)-oriented PbSe on Si(100) and a high quality substrate for subsequent growth of IV-VI laser structures. In addition, the MBE-grown BaF_2 layer incorporated into the buffer allows epitaxial lift off of such IV-VI laser structures. LPE growth on Si(111) substrates produced a PbSe layer containing a high density of melt-trapping depressions. The unexpected planarization of the (111) PbSe surface indicates that it may, however, be possible to grow (111)-oriented PbSe layers without these depressions.

5.5 References

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Chapter 6: Summary and Recommendations

Applications for thermoelectrically cooled IV-VI lasers are numerous and potentially lucrative. Their use in the pollution monitoring field could greatly impact both individual and corporate health. Thermal models have indicated that improvement in device operating temperature—made possible by growth on water soluble materials—should allow the manufacture of thermoelectrically cooled IV-VI lasers. The chief impediment to attaining this goal is immature IV-VI materials growth and processing technology. A summary of efforts to extend the boundaries of this technology are described below.

6.1 Summary of Results

Chapter 1 described the state-of-the-art for the materials system, growth methods used, and device structures employed. The double heterostructure (DH) was chosen for device fabrication due to the unavailability of in-house photolithography needed for buried heterostructure manufacture. Vertical cavity surface emitting laser (VCSEL) structures were also described as a prelude to basic design equations.

Chapter 2 described the proposed structures for DH lasers and VCSELs. Recombination centers produced by lattice mismatch imposed compositional constraints upon the epilayers, as did refractive index considerations. Upper and lower limits for active region thickness in the proposed DH lasers were obtained from a lossless, dielectric slab waveguide model and estimated minority carrier diffusion lengths in the chosen active materials. Equations relating layer composition and LPE melt constituents were provided along with recommended growth procedures. The design procedure was repeated for a proposed MBE-grown DH laser, but growth procedures could not be presented due to lack of recipes for MBE growth of the requisite materials. Basic design

equations were used to predict the behavior of CaF_2/PbEuSe Bragg reflector stacks for incorporation into an optically pumped VCSEL. Since the required reflectivities—and number of Bragg pairs—is dependent upon the unknown gain of the PbSe active region, a table of proposed Bragg reflector structures was presented.

Chapter 3 presented the result of growth experiments on (100)-oriented BaF_2 substrates. Preparation of the substrates was found to be critical to the production of acceptable epilayers. Mosaic patterns observed in the commercially procured BaF_2 samples cast doubt upon their suitability as substrates for laser production. Unreasonably high carrier concentrations—attributed to supposed inclusions caused by poor substrate quality—were obtained from Hall measurements. Contacting methods and epilayer oxidation are believed to contribute to Hall measurement error, but are not sufficient to explain the excessive carrier concentrations calculated. Improved BaF_2 preparation reduced epilayer surface roughness by a factor of 10 and lowered measured carrier concentrations. However, discrepancy remains between results obtained in this work and in previous efforts that used BaF_2 substrates purchased earlier.

Chapter 4 presented current-versus-voltage characterization of PbSe/CaF_2/Si(111) heterostructures grown by MBE to investigate the possibility of substrate-to-epilayer current injection for electrically pumping structures grown on Si(111). Ability to form MBE-grown IV-VI *p-n* junctions without doping was also investigated. Curves obtained for structures grown on high-resistivity *p*-type silicon—grown to investigate current injection through the CaF_2 buffer—indicate that high-resistivity silicon is unsuitable for use as a substrate when current injection into the epilayers is desired. Curves obtained for structures grown on conductive n^+-type silicon—grown to investigate *p-n* junctions in

PbSe—were consistent with current injection through a CaF_2 buffer interposed between the IV-VI epilayers and silicon substrate, but manifested no diode-like behavior. However, these structures demonstrated ohmic conduction near room temperature, indicating that similar structures on conductive silicon substrates may provide a mechanism for electrical pumping.

Chapter 5 presented the successful growth of crack-free PbSe layers on Si(100). The quality of the IV-VI epilayer was verified by HRXRD, SEM, AFM, and optical Nomarski inspection. The layers were grown by LPE on surfaces prepared by MBE pre-growth of CaF_2, BaF_2, and PbSe buffer layers. The LPE-grown PbSe layers lacked inclusions or melt adhesion and measured carrier concentrations were consistent with previously published data for similar layers grown on BaF_2(100) substrates by LPE. Surface roughness was as good as that obtained for the best layers on BaF_2 substrates and better than layers obtained using older BaF_2 preparation techniques. Minimization of the LPE growth temperature and substrate temperature exposure were critical to obtaining crack-free layers. Incorporation of an MBE-grown PbSe layer allowed lower LPE-growth temperatures and reduced the stresses arising from thermal expansion mismatch between the epilayers and the silicon substrate. MBE-grown IV-VI layers grown at even lower temperatures still displayed cracking—as did the MBE-grown PbSe upon which crack-free LPE growth occurred. A higher concentration of selenium vacancies in the LPE-grown material is believed to enhance dislocation movement through the layer and explain this difference in morphology. The LPE-grown layers have been successfully lifted off, are self-cleaving, and consistently form Fabry-Perot cavities suitable for optical pumping.

Appendices in this dissertation describe BaF_2 polishing procedures, LPE melt preparation and loading, cleaving jig design, construction, polishing, and electroplating, and the effects of oxygen adsorption upon IV-VI surfaces. Documented code listings are provided for the IV, HPIV, OPTICAL, CONVERT, RWT2SPW, and PLOT programs and their classes. It is hoped that individuals maintaining and improving these programs might find the consolidated listing useful.

6.2 Recommendations for Future Work

Demonstration of crack-free PbSe growth on Si(100) is a promising development, but extension to operational devices has been slow. Contacting and cleaving procedures suitable for electrically pumping lifted-off IV-VI structures are still underdeveloped. And a system for optical pumping and measurements is not yet operational. These two areas merit the greatest attention at this time. Techniques for lifting off LPE-grown PbSe layers and cleaving to produce samples suitable for optical pumping experiments have been developed and are proven. Characterization of such samples should be performed.

Growth on BaF_2 substrates should be continued if sufficient manpower is available. This ranks as a lower priority, however, due to the time intensive nature of substrate preparation. If a reliable vendor can be found for BaF_2 material and polishing can be automated, the sample-to-sample variability in epilayer quality should be greatly reduced. An advantage of growth on BaF_2 is the much closer match in thermal expansion between the BaF_2 and IV-VI epilayers than that found between the epilayers and Si. It is not unlikely that the crack-free layers grown on Si(100) contain a large number of defects generated by thermally induced stress. These could act as non-radiative recombination centers, raising pumping requirements unacceptably. This potential problem would be

greatly reduced for samples grown on BaF_2 substrates. By growing the initial PbSe layer onto the BaF_2 substrate by MBE, LPE growth temperatures on BaF_2 substrates could be reduced as observed in LPE growth on Si(100). The lower LPE growth temperature would improve LPE layer quality on BaF_2 substrates, reduce interdiffusion between epilayers during LPE growth, and produce more abrupt junctions. The feasibility of using Ar sputtering and annealing to prepare an atomically clean, highly crystalline BaF_2 surface prior to initial PbSe MBE growth should be investigated.

Growth of the proposed VCSEL structure of Chapter 2 will provide an optically pumpable laser structure as an intermediate step toward fabrication of electrically pumped VCSELs. However, the techniques for growing such structures on Si(111) have not yet been developed. Production and characterization of simple Bragg reflectors incorporating CaF_2 and PbSe epilayers on Si would seem a prudent first step. This would provide an opportunity to develop the requisite recipes for growth, verify the bandwidth and reflectivities of the mirror structures, and allow variance from expected behavior to be explained and corrected using a more easily modeled structure. Once mirror structures similar to those required for the proposed VCSEL have been grown and behave as expected, the PbSe epilayers should be replaced with PbEuSe and the mirror characteristics again verified: the estimates employed in Chapter 2's VCSEL design may be incorrect—this would be evident from the reflectivity and bandwidth obtained for the PbEuSe containing Bragg reflectors.

Current-versus-voltage measurements of simplified structures on Si(111) should be performed to extend the results of Chapter 4. Elimination of the PbSe epilayer or the CaF_2 buffer layer in the structure of Figure 4.2 would greatly simplify device modeling.

In the first case, the device could be modeled as a MIS structure—in which the metal, insulator, and semiconductor are all well defined. In the second, the band structure of the device could be simplified by growing the PbSe epilayer in direct contact with the conductive silicon substrate. For the first experiment, Au should be evaporated through a shadow mask onto the continuous CaF_2 epilayer in the growth chamber. This would avoid the wet chemical etching step used to pattern previously characterized samples.

Growth by MBE and LPE IV-VI structures on LPE-grown crack-free PbSe layers should also be investigated, but is a lower priority. Additional IV-VI layers have been grown on the crack-free layers by both methods. A small number of parallel cracks appear in the additional LPE-grown layers and a morphology reminiscent of the initial MBE-grown PbSe buffer layer of Chapter 5 appears in additional MBE-grown layers. These results are bothersome, but the density of cracks in the LPE-grown materials is sufficiently low to allow laser fabrication from the structures. LPE growth techniques presently outstrip the lab's ability to electrically pump, optically pump, or optically characterize the resulting structures. Until these facilities are developed, it is likely that efforts to improve growth procedures could be more profitably applied to the problems of contacting, cleaving, optically and electrically pumping, and optically characterizing available structures.

Appendix A: Development of a Chemical Mechanical Polish Technique for (100)-oriented BaF_2 substrates

The principal cleavage planes for BaF_2 are {111}. This allows preparation of (111)-oriented substrates by cleaving but requires that (100)-oriented substrates be cut from a block and polished. Since BaF_2 readily cleaves along its {111} planes, care and time must be spent—in large quantities—to slice commercially available crystal blocks into substrate blanks. These blanks are cut to a thickness of about 4 mm to reduce the occurrence of breakage observed in thinner-cut blanks. Once the blanks are prepared, they must be polished by hand on both sides—a process which requires approximately 8 to 10 hours and produces 4 substrates. Alternatively, the substrates may be purchased pre-cut and polished. However, the principal application of crystalline BaF_2 is for IR windows, not substrates for epitaxial growth. Surface quality of the supplied substrates is, therefore, inadequate and they must be polished as well. A one-to-two hour reduction in polishing time and a substantial decrease in lost product are obtained by employing pre-cut substrates. During substrate preparation, the surface of the substrate is abraded away by polishing with an alumina polishing grit. The size of this grit is changed as the polishing proceeds—beginning with a large grit (to remove the gross damage left by sawing the sample into thin wafers) and decreasing in size (to remove the damage left by the previously employed grit) to produce an increasingly smooth surface. The critical property of this surface is its crystallinity. Physical polishing damages this crystallinity. Incorporating chemical attack of the substrate surface provides a mechanism for material removal without the generation of dislocations.

The original procedure for preparing BaF_2 substrates for growth was divided into two processes: polishing and etching. Listed in Table A.1 is this original procedure. By altering a number of these steps, a process was developed which combined the etching and polishing throughout. This eliminated steps and greatly shortened the time needed to perform those remaining, while simultaneously improving the quality of the surfaces obtained. Since a supply of pre-cut blanks was established before development of this procedure, steps necessary for removal of saw marks were also deleted. The new procedure is listed in Table A.2.

By dissolving the BaF_2 pieces removed from the surface, the HCl solution used in the newer procedure postpones saturation of the polishing slurry. This extends the life of the slurry and the higher removal rates of the unsaturated solution. Shortened processing times and improved surface quality more than compensated for the caustic properties of the HCl-based slurries described in Table A.2.

Table A.1: Original procedure for polishing (100)-oriented BaF_2 substrates

1) Mount four substrate blanks onto a brass polishing plate using thermoplastic.
2) Attach this plate to a piston and place the piston in its sleeve—forming the "polishing jig".
3) Place approximately 2 cm^3 of 12 μm alumina grit on the center of a bare 8 inch circular quartz plate and mix with a small amount of de-ionized water to produce a thick slurry.
4) Place the polishing jig on the quartz plate.
5) While holding its sleeve, move the polishing jig across the quartz plate in a rotating "figure-eight" pattern until all saw grooves are removed. When the grit darkens during use, it must be replenished as described in step 3. (This step may be omitted if pre-cut blanks are employed.)

Due to embedded alumina grit, the surface of the soft BaF_2 will appear frosted and gray. It is important that the surface of the substrates not be touched after this point with anything other than the polishing materials.

6) After cleaning and drying the quartz plate, affix a polishing pad and repeat steps 3, 4, and 5—polishing until the embedded 12 μm grit has been removed.
7) Repeat step 6 using a clean polishing pad and 5 μm grit—polishing until the scratches left by the 12 μm grit have been removed.
8) Repeat step 6 using a clean polishing pad and 3 μm grit—polishing until the scratches left by the 5 μm grit have been removed.

The surface must be rinsed with de-ionized water and dried using dry nitrogen gas before inspection.

9) Repeat step 6 using a clean polishing pad and 0.5 μm grit—polishing until the scratches left by the 3 μm grit have been removed.
10) Remove the plate bearing the four substrates from the polishing jig.
11) Remove the substrates from the brass plate by melting the thermoplastic. After the samples have cooled, soak them in acetone to dissolve thermoplastic residues.
12) Remount the substrates, smooth side down, and repeat steps 2 through 10. Step 6 should be continued until the substrate thickness falls within acceptable limits.
13) Attach the substrate-bearing plate to a brass bar for immersion in a water bath.
14) Suspend the plate and bar assembly in a beaker of stirred de-ionized water at room temperature for 40 minutes. The water dissolves the BaF_2 surface, removing damaged exterior and exposing crystalline sub-surface.

The surface should now be covered with small hemispherical etch pits.

15) Remove the substrates from the brass plate by melting the thermoplastic. After the samples have cooled, soak them in acetone to dissolve thermoplastic residues.
16) Immediately prior to loading a substrate into the furnace for growth, rinse the surface with a 25 % HCl solution for 10 seconds. Immediately rinse with de-ionized water to remove HCl residues, then dry.

Table A.2: New procedure for polishing (100)-oriented BaF_2 substrates

1) Mix three squirt bottles containing 25 % HCl solution. In one place 12 μm grit, in another, 3 μm grit, and the last, 0.5 μm grit. The slurries produced should be moderately thick, but still exit the orifice of the squirt bottle—the 12 μm bottle's may need to be enlarged slightly.
2) Mount four substrate blanks onto a brass polishing plate using thermoplastic.
3) Attach this plate to a piston and place the piston in its sleeve—forming the "polishing jig".
4) Affix a polishing pad to the quartz plate.
5) Apply slurry sufficient to wet the surface of the polishing pad.
6) Place the polishing jig on the pad.
7) While holding its sleeve, move the polishing jig across the quartz plate in a rotating "figure-eight" pattern until the substrate surface is smooth and initial damage has been replaced by lines caused by the 12 μm grit.

When the grit darkens during use, it must be replenished by applying more slurry—approximately once per minute. Every five minutes, the pad, jig, and substrates should be thoroughly rinsed with de-ionized water. This helps to avoid cross contamination by other grit sizes and speeds the removal of material. (It also provides opportunity to stretch and replace one's outermost gloves.) It is important that the surface of the substrates not be touched after this point with anything other than the polishing materials.

8) Repeat step 7 using a clean polishing pad and 3 μm grit slurry—polishing until the scratches left by the 12 μm grit have been removed.

The surface should now appear optically flat to the naked eye. The best method developed for inspection is to look at the glancing reflection of an open set of backlit venetian blinds. The horizontal lines cast by the blinded window allow small dimples and non-uniformities to be easily detected. The surface must be rinsed with de-ionized water and dried using dry nitrogen gas before inspection.

9) Repeat step 7 using a clean polishing pad and 0.5 μm grit—polishing until the scratches left by the 3 μm grit have been removed.
10) Remove the plate bearing the four substrates from the polishing jig.
11) Remove the substrates from the brass plate by melting the thermoplastic. After the samples have cooled, soak them in acetone to dissolve thermoplastic residues.
12) Remount the substrates, smooth side down, and repeat steps 3 through 10. Step 7 should be continued until the substrate thickness falls within acceptable limits.
13) Remove the substrates from the brass plate by melting the thermoplastic. After the samples have cooled, soak them in acetone to dissolve thermoplastic residues.
14) Immediately prior to loading a substrate into the furnace for growth, rinse the surface with a 25 % HCl solution for 7 seconds. Immediately rinse with de-ionized water to remove HCl residues, then dry.

The surface should now be covered by small flat-bottomed pits, each having an apparent horizontal-to-vertical aspect ratio greater than 10:1.

Appendix B: Preparation and loading of LPE melts for IV-VI materials growth

Preparation of melts for growing IV-VI materials by LPE may be broken into three steps: determining constituent quantities, cleaning these materials, and measuring the required masses. Equations for calculating the desired melt constituents are presented in Chapter 2. This appendix contains procedures for cleaning, measuring, and loading the melts into an LPE furnace. Compositions considered are the quaternary $Pb_{1-x}Sn_xSe_{1-y}Te_y$, ternary $PbSe_{1-y}Te_y$, and binary PbTe or PbSe.

The IV-VI layers are grown from a Pb rich melt, producing a high concentrations ($>10^{18}$ cm^{-3} [1]) of Se and Te vacancies in the solid. Because chalcogenide vacancies act as donors in these materials, no *n*-type dopant is required. Adding Tl to the melt produces *p*-type layers with carrier concentrations between 10^{17} and 10^{18} cm^{-3}. It is therefore necessary to prepare Tl for inclusion in the melt as well, if *p*-type material is required. Description of material cleaning and measurement is presented in the order performed prior to loading. This order minimizes the exposure of oxidizable materials to atmosphere, so that a maximally pure melt is available for growth. Exposure to atmosphere generates an oxide layer on Tl and Pb. When these pieces are included in the melt, the oxides form a film on the surface of the melt, hindering observation of nucleation and liquidus temperatures and increasing variability of the melt constitution. They may also prevent intimate contact between the melt and the substrate surface.

All materials—save Tl, which is kept in an oil solution—are stored in a desiccator prior to use. Tl, Pb, and Sn are known to oxidize readily. As described in Appendix D, electrical and vacuum analytical techniques applied to Pb chalcogenide materials show that oxygen is adsorbed onto the surface of PbSe and PbTe as well. Adsorbed oxygen

will contaminate the resulting layers and should be minimized. Cleaning all materials prior to growth would be optimal but is performed only for Tl and Pb, since cleaning the other materials proves problematic, due to the small sizes of the pieces.

Because PbTe constitutes the smallest portion of the melt and is not amenable to division, it is measured first. Masses for the remaining constituents are then recalculated, so that the proper ratios of materials can be maintained. Measurement of PbSe follows. Any required division is made by cracking the hard crystal with a clean razor blade. Sn is next. This material is quite soft and lends itself readily to shaving, so that a nearly exact quantity of material may be obtained. Pb is cleaned by soaking in a 1:1 acetic acid:hydrogen peroxide solution. This dissolves the oxide layer that forms on the Pb surface. After soaking in the acetic acid / hydrogen peroxide solution, the Pb is agitated in two washes of de-ionized water and dipped in methanol. Methanol displaces the water and evaporates quickly in the nitrogen flow used to dry the Pb. The proper quantity of Pb is obtained as described for Sn and the materials are placed in a graphite boat—which is pre-loaded with a substrate and ready for insertion into the LPE furnace. If Tl is required for doping, a pellet is removed from its oil-filled storage bottle. The pellet is rinsed in acetone and methanol to remove the oil residue, and the surface shaved away with a razor. The requisite amount is measured and immediately placed in the boat with the other materials. The boat is then sealed in the furnace and flooded with oxygen-scavenging hydrogen gas. If a multiple layer structure is desired, the materials should be prepared and measured in parallel, so that minimal exposure to atmosphere occurs for the Pb and Tl.

References

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Appendix C: Construction and Preparation of a Cleaving Jig for Epitaxial Lift Off

Because epitaxial lift-off and cleaving is a pressing barrier to realization of high-temperature IV-VI double heterostructure tunable diode lasers, much effort was spent improving materials processing in this area. This appendix describes the cleaving jig, polishing techniques, and electroplating methods developed in cooperation with another member of the lab, whose parallel efforts are published elsewhere [1].

Inital versions of the cleaving jig were excessively large and complex.. As shown in Figure C.1 (a), the jig consisted of two thick copper plates and a number of thinner copper cleaving plates held together by steel screws. After assembly, the jig surface and cleaving plates were milled, sanded, and polished. The multi-body nature of the jig allowed the sandwiching plates to rotate and shift relative to one another. This made resurfacing the jig necessary after reloading cleaving plates. Jigs were quickly thinned beyond usefulness. Processing developments toward electroplating and hydrogen ambient bonding—discussed below—required reduced size and improved materials compatibility.

The second generation jig comprised a single-piece body and a solitary steel set screw providing compression of the inner cleaving plates, as shown in Figure C.1 (b). This model was slightly smaller than the previous generation, and was acceptable for atmospheric bonding. It did, however, tend to allow the cleaving plates to twist as they were milled flat. This complicated jig preparation. A smaller vesion of this design, small enough to fit in an available hydrogen furnace, is shown in Figure C.1 (c). This jig incorporated a brass pressure plate which fit over the sample during bonding and was constrained horizontally by two alignment pins. Replacement of the single set screw with two smaller screws and addition of ball bearing pivots at both ends allowed the jig

size to be reduced further and cleaving plate rotation to be eliminated. In the final design, the two steel screws were replaced with three smaller screws made of brass and the ball bearings and upper pressure plate were eliminated. Material for body of the jig was changed to brass, as well. This eliminated all materials other than copper and brass and improved compatibility with the developing electroplating and nitric acid based polishing procedures.

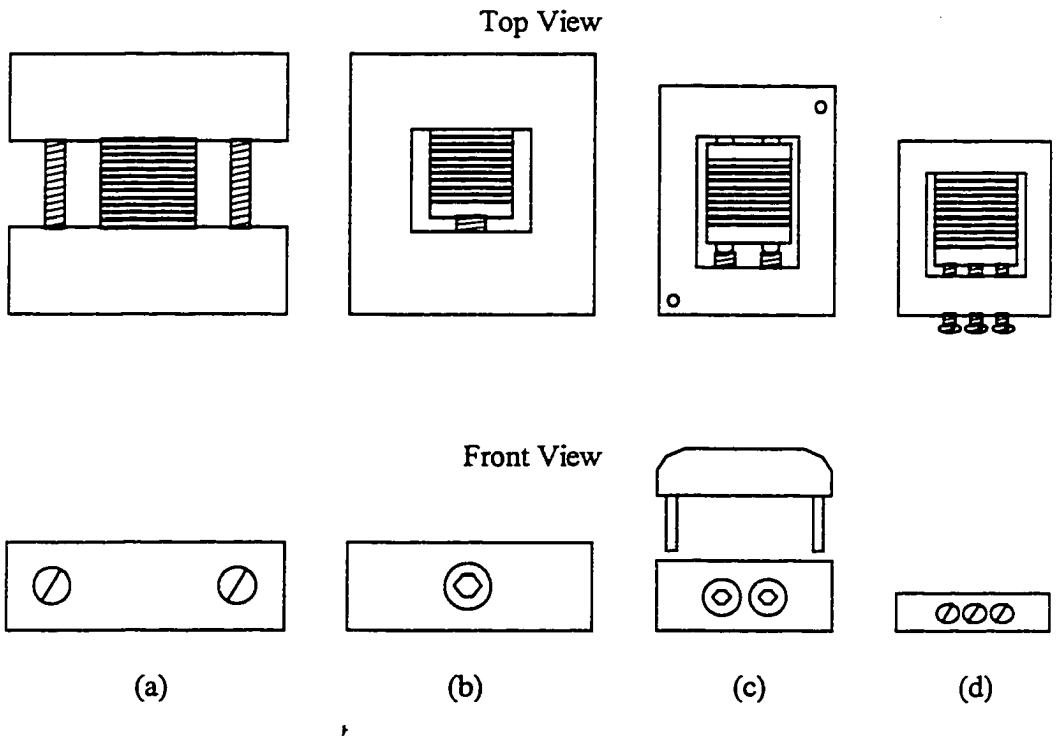

Figure C.1: Four generations of cleaving jigs. Jigs (a), (b), and (c) were made of copper and used steel screws. (c) included a vertically mobile plate for applying pressure during bonding. (d) was made entirely of brass—except for the cleaving plates, which were copper in all jigs.

By incorporating a larger number of screws, the stress on each screw was reduced so that a weaker material and smaller screws could be used and the jig could be thinned. An

additional benefit was the more uniform pressure applied to the cleaving plates. This final design is shown in Figure C.1 (d).

Preparation of the jig for electroplating required that the surface of the jig be smoothed. Initial milling removed the majority of the excess material. Sanding on 220, 400, and 600 grit sandpapers eliminated the scars from milling. The original polishing procedure after this point was identical to the original procedure for polishing BaF_2 substrates described in Appendix A, except for the water bath and final etch. As was the case for polishing BaF_2, the 12 μm grit used in the preliminary polish became embedded in the Cu surface. Removing this grit required extensive polishing on a pad and frequent replacement of the grit. Altering the procedure in a parallel fashion to the modification made to the BaF_2 precedure produced similar improvement. (It should be noted that modification of the Cu polishing procedure was actually made first. Improved results from the new Cu polishing suggested that acid slurry based polishing might work in the case of BaF_2 as well.) The new Cu polishing procedure is identical to the improved procedure described in Appendix A, except that a 10 % nitric acid solution was used as the liquid component of the polishing slurry. Copper polishing rates observed using HNO_3-based polishing slurries have been explained by a two step model [2]: the surface of the copper is mechanically removed by the abrasive and the abraded copper particles are chemically dissolved by the HNO_3. At high concentrations of acid, the surface removal rate of material is determined by the abrasive concentration (and applied pressure). At low concentrations of acid, the removal rate is determined by the acid concentration, which limits particle dissolution. When material is removed from the surface faster than it can be dissolved, the slurry saturates. Excess material is then

redeposited onto the surface. With a sufficient concentration of acid, the material removal rate will be abrasive concentration limited. This prevents rapid saturation of the slurry and copper redeposition onto the surface—and the concomitant trapping of alumina grit. Polishing with the series of abrasives listed in Appendix A produces a scratch-free surface for bonding. The cleanliness of this surface provides a high quality interface with the metals subsequently deposited.

Standard procedure for preparing copper for plating [3] is to preclean to remove organic residues, alkaline clean, and activate by short immersion in either sulfuric acid or hydrochloric acid solutions. Because of the high quality surface obtained from polishing, only a 15 second dip in 5 % sulfuric aid at room temperature is needed. For plating with Au, a nickel strike is also recommended, but was not used.

Two plating procedures were developed: immersion plating of Sn and electroplating of Au. These were later extended to allow the plating of a 60:40 Pb:Sn alloy. Immersion plating of Sn was first performed using a solution prepared in house. This recipe [4] is given in Table C.1.

Table C.1: Recipe for immersion plating Sn onto Cu. Solution should be held between 40 and 65 C.

Potassium stannate	45.0 g/L
Potassium cyanide	105.0 g/L
Potassium hydroxide	7.5 g/L

After demonstrating this procedure, a commercially prepared solution was obtained. Quality of the resulting layers was disappointing. Electroplating of Au from a commercial bath was tried next. High brightness layers were plated on copper, PbSe, and high conductivity Si under the conditions recommended by the bath manufacturer. However, the thickness of the plated layers varied across the surface of the sample. In

addition, areas of the sample would appear tarnished. Tarnishing was attributed to dissolution of the plated Au from the sample surface back into the plating bath and the drops of the bath which adhere to the sample after removal from the bath. Immediate removal of the sample from the plating bath upon cessation of plating and rinsing with deionized water eliminated the tarnishing problem. Variation of layer thickness across the sample can be explained by a combination of dissolution of the layer as just described and nonuniform current flow through the sample during plating.

References

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[3] E. C. Groshart, "Preparation of basis metals for plating", in Metal Finishing, vol. 60, edited by M. Murphy, Elsevier Science, New York, 1992.

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Appendix D: Effects of Oxygen upon IV-VI Layers

Work by several groups has demonstrated that exposure to oxygen can produce large changes in the electrical and physical properties of the surface of IV-VI layers. These effects are especially pronounced in thin layers, where the surface region can compose a large share of the layer thickness. The IV-VI compounds PbSe, PbTe, PbSnSe, and PbSSe have been examined by a number of methods, including Hall and thermoelectric power measurements, Auger electron spectroscopy (AES), x-ray photoelectron spectroscopy (XPS), and ultraviolet photoelectron spectroscopy (UPS). A cursory survey of some of these studies assists in understanding the dangers associated with oxygen exposure.

Bode and Levinstein [1] measured the electrical properties of thin vapor-grown *n*-type PbTe films in 1954. It had been noted that many IV-VI films required sensitization, by oxygen exposure, to achieve a photoconductive response. These experiments were an attempt to understand the process. They measured the *in situ* conductivity and thermoelectric power of the grown films, before and after exposures to increasing oxygen doses. The films demonstrated a decrease in conductivity as oxygen exposure increased—until the process reversed and conductivity began to increase again at high exposures. Thermoelectric power measurements indicated a coincidence between the conductivity minimum and conversion of the material from *n*- to *p*-type. This conversion took place at lower oxygen exposures for materials grown on lower temperature substrates, which produce more porous films. Their model proposed that oxygen adsorbed onto the PbTe surface and took electrons from the PbTe conduction band. Once the conduction band emptied, trapping state and the valence band electrons were

removed, converting the material. An investigation published in 1957 by Humphrey and Scanlon [2] found similar results for PbSe films.

Jensen and Schoolar [3] examined the effect of layer thickness upon the carrier concentration and mobility of oxygen-exposed (111)-oriented PbSnSe and PbSSe compounds and fit their measurements to a two-layer model [4] to extract estimates of these values for the surface and bulk regions. They concluded that carrier scattering at the semiconductor-air interface was specular for (111) PbSe, in agreement with reports by Brodsky and Zemel [5] for (100) PbSe. Calculated mobilities in the ternary compounds did not support a similar conclusion for these compositions.

Sun et al. have examined (111) surfaces of MBE-grown PbTe [6] and $Pb_{0.8}Sn_{0.2}Te$ [7] to describe the oxygen adsorption and bonding process using AES, XPS, and UPS. For *n*-type PbTe, they concluded that the oxygen uptake process proceeds in two stages—with the boundary at an exposure of 10^5 L. In the first stage (adsorption), oxygen adsorbs slowly—mostly at defect sites [8]—building up negative charge on the surface as electrons are transferred to the adsorbed oxygen. This induces a positive charge region just below the surface and bends the energy bands. The combination of electric field and surface strain from the adsorbed oxygen builds up until an exposure of about 10^5 L. In the second stage (oxidation), Pb-Te bonds across the surface are broken, oxygen uptake increases dramatically, and Pb-O and Te-O bonds are formed. Further exposure produces little change in the surface after this point, due to the oxide layer. Shift in the valence band maximum (relative to the Fermi level) is about 0.25 eV at an exposure just below 10^5 L, and changes only slightly during the oxidation stage. Comparison to the PbSe bandgap, 0.31 eV at 300 K, indicates that this produces a strongly *p*-type surface region.

Behavior of the *p*-type Sn containing compound is slightly different. Again there is a two stage process, and the process proceeds as before—except that the oxygen attaches at the Sn sites, producing Sn oxide, and an increase in Sn concentration is measured at the surface. The resulting valence band shift is somewhat smaller (only 0.15 eV) at the boundary exposure, but the bandgap of the material is smaller as well (0.2 eV at 300 K). Upon reaching the threshold exposure, Pb-Te bonds again break and form Pb-O and Te-O, accelerating adsorption. The main difference observed in this system is that oxygen adsorption does not saturate near 10^6 L—as was the case for PbTe—but continues beyond 10^9 L. This has been attributed to Sn diffusion from the bulk, providing additional Sn sites at the surface and producing diffusion channels which allow oxidation of Te and Pb deeper in the layer. This diffusion is accelerated by heating and is driven even in vacuum by residual oxygen adsorbed on the surface. Polycrystalline or amorphous Sn oxide, such as the layer formed during oxidation, is know to be *n*-type with a high conductivity [9], with possibly grave consequences for oxygen-exposed devices containing Sn, or attempts to measure the electrical properties of thin Sn containing lead chalcogenide layers.

Another problem arising from surface oxidation of lead chalcogenides is hinted at by observations of high carrier mobilities and specular scattering near the air-semiconductor interface. If an n-type PbSe layer is exposed to air, the energy band bending described above should increase non-radiative recombination due to surface states. This can be explained with the aid of Figure D.1. Electrons will be repelled from the surface—and the non-radiative recombination centers associated with it—by the negative surface charge of the adsorbed oxygen. This phenomenon can explain the specular reflection seen in Hall mobility measurements of *n*-type PbSe [3, 5]—and is apparently a helpful

thing. But Hall measurements provide and estimate of *majority* carrier mobility. The mobility of minority carriers injected into this region will be adversely effected by this band structure. For optically pumped laser structures this would be especially true, since carriers are produced near the exposed surface. Electrons produced by the optical excitation would migrate away from the surface. However, the corresponding holes will be pushed toward the surface and the non-radiative recombination centers it contains. Since it is the minority carrier concentration that is critical to lasing, oxidized optically pumped structures will prove more difficult to push to threshold.

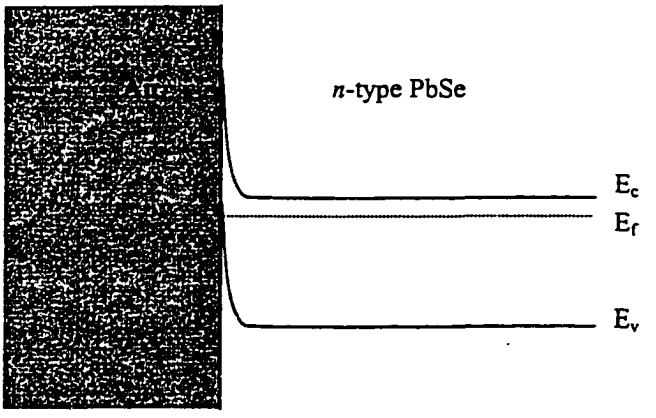

Figure D.1: Band alignment of *n*-type PbSe near an oxygen exposed surface

References

[1] D. E. Bode and H. Levinstein, "Effect of Oxygen on the Electrical Properties of Lead Telluride Films", *Phys. Rev.* **96**, 259 (1954)

[2] J. N. Humphrey and W. W. Scanlon, "Photoconductivity in Lead Selenide. Experimental", *Phys. Rev.* **105**, 469 (1957)

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[9] Z. M. Jarzebski and J. P. Marton, *J. Electrochem. Soc.* **123**, 299C (1976).

Appendix E: Code Lisitings of Various Utility Programs

Code lisitings of programs written during the course of this project are provided in this appendix. It is hoped that these will provide adequate documentation of the programs to allow those who continue this work to use and maintain them. The following programs are documented:

Convert.cpp	C++ source code for a DOS command to convert Bruker's JCAMP-DX format to MATLAB compatible or ASCII formatted output. This program is required to convert the output of the Aspect 2000 FTIR system to a useable form.
Hpiv.cpp	C++ source code for a program to automate the acquisition of current-versus-voltage and temperature data from a system comprised of an HP4140B voltage source and current meter and an LS805 temperature controller.
Hpiv.h	C++ classes used by Hpiv.cpp.
Plot.cpp	C++ source code for a DOS command to graphically display the first two columns of a whitespace delimited text file. The plotting routine is autoscaling. Plot.cpp was used to display the output produced by Hpiv.cpp.
Optical.cpp	C++ source code to control a Stanford Research SR510 lock-in amplifier and ILX Lightwave LDC3900 laser diode supply. Assumes that a square wave singal is connected to the ILX modulation line.
Optical.h	C++ classes used by Optical.cpp
Rwt2txt.cpp	C++ source code to convert output from a Tencor P-1 surface profiler into a SigmaPlot compatible file.
IV.bas	A Qbasic file used to acquire current-versus-voltage measurements with a Keithley 224 current supply and a Keithley 195A digital multimeter.

```
////////////////////////////////////////////////////////////////
//
//    Project CONVERT.CPP
//
//          Brian N. Strecker
//          Copyright 1995. All Rights Reserved.
//
//          FILE:                   CONVERT.CPP
//          AUTHOR:                 Brian N. Strecker
//          DATE BEGUN:             November 20, 1994
//          LAST EDIT:              June 1, 1995
//          VERSION:                1.2
//
//          OVERVIEW
//          ========
//          Source file for a DOS command to translate output
//          from Bruker's JCAMP-DX to two column, space delimited,
//          transmittance-versus-wavenumber format. (MATLAB
//          compatible output is also supported in this program
//          version.)  JCAMP-DX is used to translate FTIR spectrum
//          data taken on a Bruker Aspect 2000 system from the
//          Bruker system's native 24-bit ATS format to an ASCII
//          file with a header.  This allows the data to be
//          transmitted from the Aspect 2000 to a PC via a serial
//          port connection.  The code provided here extracts the
//          information needed to interpret the ASCII formatted
//          data from the header of the file produced by JCAMP-DX
//          and uses it to calculate the transmittance and
//          wavenumber of each point in the scan.
//
////////////////////////////////////////////////////////////////

#include <fstream.h>          // contains file input/output classes
#include <stdlib.h>
#include <cstring.h>          // contains string classes
#include <conio.h>
#include <iomanip.h>          // contains i/o manipulators
#include <classlib\arrays.h>  // contains array templates


//
// function definitions
//

//
//getText
// Locates Find_String in File, reads the line which contains it into
// CurrentLine, locates '=' in the string and extracts the text to the
// right of it.
//
//    Takes:      a copy of the string to be found
//                a reference to the file to search
//    Returns:    a pointer to the text after the equals sign
//                in the line containing the search string
```

```
//
string & getText(  string Find_String, fstream & InputFile)
{
      static string Work_String;
      char  CurrentLine[80];
      size_t Position;
      // Move stream pointer to beginning of file stream
      InputFile.seekg(0);

      // Read in lines from file until Find_String is located
      do {
            InputFile.getline( CurrentLine, 80, '\n');
            Work_String = string(CurrentLine);

            // Return error if Find_String not in Input File
            if (InputFile.ios::fail())
                  {
                  cout << "/n  Unable to locate string \""
                  << Find_String << "\" before end of file."
                        << endl << endl;
                  exit(EXIT_FAILURE);
                  };

      } while ( Work_String.find( Find_String) == NPOS);

      // find '=' position
      Position = Work_String.find( string('='));

      // get text to right of =
      Work_String = Work_String.substr( Position+1);

      return Work_String;
};

//
//getNumber
// Locates Find_String in File, reads the line which contains it into
// CurrentLine, locates '=' in the string and extracts the number to
// the right of it.
//
//          Takes:      a copy of the string to be found
//                      a reference to the file to search
//          Returns:    a copy of the number after the equals sign
//                      in the line containing the search string
//
float getNumber( const string Find_String, fstream & InputFile)
{
      string Work_String;
      char  CurrentLine[80];
      size_t Position;
      float Number;

      // Move stream pointer to beginning of file stream
      InputFile.seekg(0);

      // Read in lines from file until Find_String is located
```

```
      do {
            InputFile.getline( CurrentLine, 80, '\n');
            Work_String = string(CurrentLine);

            // Return error if Find_String not in Input File
            if (InputFile.ios::fail())
            {
                  cout << "/n  Unable to locate string \""
                        << Find_String << "\" before end of file."
                        << endl << endl;
                  exit(EXIT_FAILURE);
            };
      } while ( Work_String.find( Find_String) == NPOS);

      // find '=' position
      Position = Work_String.find( string('='));
      Work_String = Work_String.substr( Position+1);

      // get text to right of =
      Number = atof( Work_String.c_str());

      // convert text to number
      return Number;
}


//
//parseLine
// Calculates the transmittance and wavenumber values of FTIR data
// based upon the string containing the unconverted data and some
// parameters passed to the function.
//
//   Takes:       a reference to the output file
//                a pointer to the string containing the
//                unconverted data
//                a conversion factor for the transmittance
//                a conversion factor for the wavenumber
//                the wavenumber distance between consecutive
//                data points
//    Returns:    nothing - But sends converted data to output file.
//
//    Process:    The input line is in the form -
//                      XDATA1+YDATA1+YDATA2+YDATA3+YDATA4+...
//
//    Point 1     wavenumber:       WAVENUMBER = XDATA1 * X_Factor
//                transmittance:    TRANSMITTANCE = YDATA1 * Y_Factor
//    Point 2+    wavenumber:       WAVENUMBER = WAVENUMBER + Delta_X
//                transmittance: TRANSMITTANCE = YDATA2+ * Y_Factor
//
// Takes a full line of input
void parseLine( fstream & Output_File, const char * Current_Line,
                  float X_Factor, float Y_Factor, float Delta_X)
{
      string X_Data, Y_Data, Current_String;
      size_t Position;
      float X_Value, Y_Value;
```

```
        X_Data = Current_String = Current_Line;

        // locate +
        Position = Current_String.find( string('+'));

        // get text to left of +
        X_Data = X_Data.remove( Position);

        // convert text to X value
        X_Value = atof( X_Data.c_str()) * X_Factor;

        // remove text to left of + from input line
        Current_String =  Current_String.substr( Position+1);

        // locate 2nd +
        Position = Current_String.find( string('+'));

        // extract until last +
        while( Position != NPOS)
        {
              Y_Data = Current_String;

              // get text to left of +
              Y_Data = Y_Data.remove( Position);

              // remove text to left of + from input line
              Current_String = Current_String.substr( Position+1);

              // convert text to Y value
              Y_Value = atof( Y_Data.c_str()) * Y_Factor;

              // write X, Y to output file
              Output_File << setprecision(20) << X_Value
                          << ' ' << Y_Value << endl;

              // calculate next X value
              X_Value += Delta_X;

              // locate next +
              Position = Current_String.find( string('+'));
        };

        // calculate last Y value
        Y_Value = atof( Y_Data.c_str()) * Y_Factor;

        // write last X, Y to output file
        Output_File << X_Value << ' ' << Y_Value << endl;
};


//
// Main Program Function
//
void main( int argc, char * argv[])
        {
        //
        // Variable definitions
```

```
//

// read_all_data? Flag, error_with_file? Flag, and matlab?
// flags
int DoneFlag=0, EndFlag=0, matlab=0;

// temporary buffer to catch keypresses
char keyin='0';

// source filename, output filename, temporary string,
// units for the x data, and units for the y data
string Source, Output, CurrentString, XText, YText;

// buffer for reading in data
char CurrentLine[80];

// Xfactor * raw x data = X value,
// Yfactor * raw y data = Y value,
// and distance between x values in output

float XFactor=0.0, YFactor=0.0, DeltaX=0.0;


//
// Get source file and output file and verify conversion
//
cout << endl << endl;

// Explain the program's usage if it was started w/o a source
// file name
if( argc == 1)
{
      cout << endl << endl << "CONVERT.EXE version 1.2 - "
      << "last update May 31, 1995" << endl << endl;
      cout << "CONVERT translates FTIR spectrum data"
      << " produced by JCAMP-DX software" << endl
      << "        to a two column ASCII format.  It was"
      << " written by Brian Strecker" << endl
      << "        at the University of Oklahoma in 1994."
      << "  The JCAMP-DX file must" << endl
      << "        have the extension '.dx'.  The output"
      << " file is written to the" << endl
      << "        current directory.  MATLAB formatted"
      << " output is also supported." << endl
      << endl << endl << endl
      << "        Acceptable usage: CONVERT" << endl
      << "                          CONVERT 'source'    "
      << " -'source' has no extension" << endl
      << "                                              "
      << " since the program adds '.dx'" << endl
      << "                          CONVERT 'source' \\q"
      << " -the \\q switch disables the" << endl
      << "                                              "
      << " 'Is this acceptable?' prompt." << endl
      << "                                            \\m"
      << " -the \\m switch enables MATLAB" << endl
      << "                                              "
```

```
        << " output format (may be used as" << endl
        << "                                                    "
        << " \\qm or \\mq)" << endl;
        cout << endl << endl << endl;
        cout << "  Source filename w/o extension" << endl;
        cout << "     (.dx assumed): ";
        cin >> Source;
cout << endl << endl
     << "  MatLab output format? (Y for yes) ";
cin >> keyin;
if( (keyin=='y') | (keyin=='Y'))
{
        keyin=' ';
        matlab=1;
        };

} else
{
        // take source filename fromcommand line if possible
        if( argc > 1)
        {
              Source = string( argv[1]);
        };

        // skip source file input and verification if \q flag
        // and source filename are provided from the command
        // line
        if( (argc == 3) & ( (!strcmp( "\\qm", argv[2])) |
           (!strcmp( "\\mq", argv[2])) |
           (!strcmp( "\\q",  argv[2])) ) )
        {
              keyin = 'Y';
        };

        // skip source file input and verification if \m flag
        // and source filename are provided from the command
        // line
        if( (argc == 3) & ( (!strcmp( "\\qm", argv[2])) |
           (!strcmp( "\\mq", argv[2])) |
           (!strcmp( "\\m",  argv[2])) ) )
        {
              matlab = 1;
        };
};
if(!matlab)
{
        // set output filename
        Output = Source + ".cnv";
} else
{
        Output = Source + ".m";
};

// add .dx extension to source filename
Source += ".dx";

// convert names to upper case
```

```
Output.to_upper();
Source.to_upper();

// check source filename if not provided from command line
if( keyin != 'Y')
{
      cout << endl << endl;
      cout << "  Source filename:  " << Source << endl;
      cout << "  Output filename: " << Output << endl << endl;
      cout << "Correct? (Y to accept, any other terminates"
            << " program) ";
      keyin=getch();
      cout << endl << endl << endl;
};

//
// convert file if conversion approved
//
if( (keyin=='y') | (keyin=='Y'))
{

      //
      // read in data
      //

      // set up input file
      fstream InputFile( Source.c_str(), ios::in |
                        ios::nocreate);

      // set up output file
      fstream OutputFile( Output.c_str(), ios::out);

      // set flag and give message if input set up fails
      if( InputFile.fail())
      {
            cout << '\a' << "Unable to read from source"
                  << " file:  " << Source << endl;
            EndFlag = 1;
      };

      // set flag and give message if output set up fails
      if( OutputFile.fail())
      {
            cout << '\a' << "Unable to write to output"
                  << " file:  " << Output << endl;
            EndFlag = 1;
      };

      // if all is ok, read in data
      if( !EndFlag)
      {
            //
            // extract required data for conversion from Header
            //

            // get X conversion factor
            XFactor = getNumber( string("XFACTOR"), InputFile);
```

```
// get Y conversion factor
YFactor = getNumber( string("YFACTOR"), InputFile);
// get X step size
DeltaX = getNumber( string("DELTAX"), InputFile);

// get X units
XText = getText( string("XUNITS"), InputFile);

// get Y units
YText = getText( string("YUNITS"), InputFile);

// send matlab formatting if MATLAB format requested
if(matlab)
{
      OutputFile << "% Converted from " << Source
                 << endl << "% X is " << XText
                 << endl << "% Y is " << Ytext
                 << endl << endl << "xyDATA=["
                 << endl;
} else
{
      // send units to output file if ASCII
      // requested
      OutputFile << XText << ' ' << YText << endl;
};

//
// read in and convert X, Y data
//

// Set pointer to start of XY data
CurrentString = getText( string("XYDATA"),
                         InputFile);
DoneFlag = 0;

// read/write until data runs out
while( !DoneFlag)
{
      // read first data line
      InputFile.getline( CurrentLine, 80, '\n');

      // check to see if data is still available
      if( strncmp( CurrentLine, "##END", 5))
      {
            // extract, convert, and write X, Y
            // values to output file
            parseLine( OutputFile, CurrentLine,
                       XFactor, YFactor, DeltaX);
      } else
      {
            // set flag if no more data
            DoneFlag = 1;
      };
};

// send MATLAB formatting if requested
```

```
                    if(matlab)
                    {
                          OutputFile << "];" << endl;
                    };

                    // notify user of successful conversion
                    cout  << Source << " converted to " << Output << endl
                                << endl;
              };
        } else
        {
              //
              // end program if conversion not approved
              //
              // notify user of termination
              cout << "Program terminated" << endl;
        };
        cout << endl << endl;

        // exit program
        exit(EXIT_SUCCESS);
};
```

```
////////////////////////////////////////////////////////////////////////
//
//      HPIV.CPP
//
//
//      author:         Brian N. Strecker
//      date:           2 December, 1996
//      revision:       1.0
//
////////////////////////////////////////////////////////////////////////

#include <stdlib.h>
#include <conio.h>
#include <iostream.h>
#include <cstring.h>
#include <time.h>
#include "HPIV.h"
extern "C" {
        #include <ieeeio.h>
        };

//
// Main Program
//
int main( int argc, char * argv[])
{

//
// explain program usage unless -s switch sent
//
if( (argc!=2) || (strcmpi( argv[1],"-s")) )
{
      cerr << "\nHPIV.EXE reads data from an HP4140B and LS805."
           << "  The resulting\n"
           << "           current, voltage, and temperature"
           << " readings are sent\n"
           << "           to the console as white space separated"
           << " columns.  The\n"
           << "           HP4140B should be set up for the"
           << " measurement via its\n"
           << "           front panel.  HPIV.EXE triggers the"
           << " instrument and\n"
           << "           acquires the data.  The -s flag turns"
           << " off this\n"
           << "           message.\n\n"
           << "           Copyright Brian N. Strecker, 1996\n"
           << "           Freely distributable - not to be sold.\n\n"
           << "Usage:  HPIV -s > FILEOUT.TXT \n";
        exit(EXIT_FAILURE);
};

// establish Personal488 connection - the vaiable ieee holds the file
//      handle for accessing the GPIB card after calling ieeeinit()
if( ieeeinit()==-1 )
{
      cerr << "Unable to establish communication with"
           << " Personal488 card."  << endl;
```

```
        exit(EXIT_FAILURE);
}

HPIV    hpiv;

hpiv.start();
hpiv.get_data();
hpiv.set_local();

return 0;
}
```

```
////////////////////////////////////////////////////////////////////////
/
//
//      Class definitions for the HPIV class.  The HP4140B should have
//      address 14 and the LS805 should have address 12.
//
//      author:         Brian N. Strecker
//      date:           2 December, 1996
//      modified:       6 December, 1996      temperature reading added
//      revision:       1.0
//
////////////////////////////////////////////////////////////////////////

#if !defined(__HPIV_H)
#define __HPIV_H

extern "C" {
        #include <ieeeio.h>
        };
#include <cstring.h>


////////////////////////////////////////////////////////////////////////
//
//
// HPIV Class definition and member functions
//
class HPIV {
      private:
            char        input_string[256];
            string      manip_string,
                        temp_string;
            long double     voltage;
            long double     current;

      public:
            // constructor for class
            HPIV();

            // read actual current (in mA)
            void get_status();
            void start();
            void get_data();
            void set_local();
      };

HPIV::HPIV() { }

void HPIV::get_status()
        {
        ieeewt( "OUTPUT 14;K\n");
        ieeewt( "ENTER 14\n");
        ieeerd( input_string);
        cout << input_string << endl;
        ieeewt( "OUTPUT 12;W2\n");
        ieeewt( "ENTER 12\n");
        ieeerd( input_string);
```

```
        cout << input_string << endl;
        }

void HPIV::start()
        {
        ieeewt( "OUTPUT 14;W1\n");
        ieeewt( "OUTPUT 12;WS\n");
        }

void HPIV::set_local()
        {
        ieeewt( "LOCAL 14\n");
        ieeewt( "LOCAL 12\n");
        }

void HPIV::get_data()
        {
        do
            {
                ieeewt( "ENTER 14\n");
                ieeerd( input_string);
                manip_string = input_string;
                manip_string.strip( string::Leading);
                temp_string = manip_string( 3,10);
                current = _atold( temp_string.c_str() );
                temp_string = manip_string( 15,7);
                voltage = _atold( temp_string.c_str() );
                ieeewt( "ENTER 12\n");
                ieeerd( input_string);
                cout << current << " " << voltage << " "
                     << input_string << endl;
            } while (manip_string[1] != 'L');
        }


#endif  // __HPIV_H
```

```
////////////////////////////////////////////////////////////////////////
/

//

//      PLOT.CPP

//

//      Source code for a program to plot two-column data to a VGA

//      screen.  The program accepts the filename of the file holding
//      the whitespace-delimited two column data from te command line.

//      PLOT then scans the data file twice.  The first time to extract

//      the minimum and maximum values of the data in each column.  The
//      second time to plot the data to the screen.  Column 1 is taken
//      to be the vertical, y, axis and column 2 is the horizontal, x,
//      axis.  Data after the first two entries on each line--up to the
//      next linefeed--is ignored.  A key must be pressed
//      before the program returns to the text mode and the command

//      interpreter.

//

//      author:         Brian N. Strecker

//      date:           25 October, 1996

//      revision:       1.0
//
//      Copyright 1996 Brian N. Strecker.
//              Freely distributable.  Not to be sold.
//
////////////////////////////////////////////////////////////////////////



#include <graphics.h>
#include <conio.h>
#include <fstream.h>
#include <iostream.h>
#include <stdlib.h>
#include <string.h>

#define LINE_COLOR YELLOW
#define SPOT_COLOR WHITE
#define BORDER_COLOR GREEN
#define LABEL_COLOR LIGHTGREEN

//
// main program
//
void main( int argc, char *argv[])
```

```
{


      //

      // variable declarations
      //

      // min and max values in file - used for setting borders

      double  min_x=0, max_x=0, min_y=0, max_y=0, x, y;

      float   scrn_width, scrn_height;

      // use VGA or EGA display if avail

      int     gd=DETECT, gm=0;

      char    buffer[512];


      //

      // explain program usage unless -s switch sent

      //

      if( (argc!=2))
      {

            cerr << "\nPLOT.EXE plots two column data from a file. "
            << " The first\n"

            << "           is used as the vertical data and the"
            << " second is\n"

            << "           used as the horizontal data.  The"
            << " minimum and\n"

            << "           maximum or each column are found"
            << " and used as the\n"

            << "           limits of the display.  Requires "
            << "VGA or EGA\n"

            << "           display.  The file EGAVGA.BGI must"
            << " be available\n"
            << "           to PLOT.EXE\n\n"
            << "           Copyright Brian N. Strecker, 1996\n"
            << "           Freely distributable - not to be sold.\n\n"
            << "Usage:  PLOT.EXE FILEIN.TXT \n";
            exit(EXIT_FAILURE);
      };

      //
      // initialize file input stream
```

```
//
ifstream        fin(argv[1]);

if( fin.fail() )
{

      cout << "unable to open file" << endl;

      exit(EXIT_FAILURE);

};



//

// get min_x, max_x, min_y, and max_y from file

//

fin >> y;

min_y = y;

max_y = y;

fin >> x;

min_x = x;

max_x = x;
fin.getline( buffer, 511);
while( !fin.eof() )
{

      fin >> y;

      if( y<=min_y) { min_y = y; };

      if( y>=max_y) { max_y = y; };

      fin >> x;

      if( x<=min_x) { min_x = x; };

      if( x>=max_x) { max_x = x; };

      fin.getline( buffer, 511);

};

//
// draw screen
//
initgraph( &gd, &gm, "");
scrn_width=getmaxx();
scrn_height=getmaxy();
```

```
        setbkcolor( BLACK);
        setcolor(BORDER_COLOR);
        rectangle(0,0, scrn_width, scrn_height);
        setcolor(LABEL_COLOR);
        settextjustify( 1, 2);
        outtextxy( scrn_width/2, 2, gcvt( max_y, 3, buffer));
        settextjustify( 1, 0);
        outtextxy( scrn_width/2, scrn_height-2, gcvt( min_y, 3, buffer));
        settextjustify( 2, 1);
        outtextxy( scrn_width-2, scrn_height/2, gcvt( max_x, 3, buffer));
        settextjustify( 0, 1);
        outtextxy( 2, scrn_height/2, gcvt( min_x, 3, buffer));

        //
        // get x, y and plot
        //
        fin.close();
        fin.open(argv[1]);
        fin >> y;
        fin >> x;
        fin.getline(buffer,512);
        moveto( (x-min_x)/(max_x-min_x)*(scrn_width),
              scrn_height - (y-min_y)/(max_y-min_y)*(scrn_height) );
        setcolor(SPOT_COLOR);
        circle( getx(), gety(), 2);
        setcolor(LINE_COLOR);
        while( !fin.eof() )
        {

              fin >> y;

              fin >> x;
              lineto( (x-min_x)/(max_x-min_x)*(scrn_width),
               crn_height - (y-min_y)/(max_y-
              setcolor(SPOT_COLOR);

              circle( getx(), gety(), 2);
              setcolor(LINE_COLOR);
              fin.getline(buffer,512);
        };

        //
        // pause before clearing screen
        //
        getch();

        //
        // clear screen and return to text mode
        //
        closegraph();

};
```

```
////////////////////////////////////////////////////////////////////////
//
//      OPTICAL.CPP
//
//      Source code for a program to control a Stanford Research SR510
//      Lock-in amplifier and an ILX Lightwave LDC3900 Laser Diode
//      Controller.  The program prompts the user for the minimum and
//      maximum desired drive current and the number of steps between
//      these values.  It then sets the output current of the LDC3900
//      to the 1st value, adjusts for the modulation applied to the
//      output (assumes square wave modulation with a 50% duty cycle),
//      waits for the output to settle, and reads the detector signal
//      strength from the SR510.  These values are printed to a file
//      (OPTICAL.OUT) having the following output:
//
//              first line:         ILX[mA] SR[mV]
//             second line:         xxxxxx1 yyyyyy1
//                   etc :          xxxxxx2 yyyyyy2
//
//      where xxxxxxn and yyyyyyn are the output of the LDC3900 and the
//      input from the SR510 for data point n.
//
//      The file OPTICAL.H contains class definitions for the ILX and
//      SR objects.
//
//      author:         Brian N. Strecker
//      date:           14 October, 1996
//      revision:       1.0
//
////////////////////////////////////////////////////////////////////////

#include <stdlib.h>
#include <conio.h>
#include <iostream.h>
#include <fstream.h>
#include <cstring.h>
#include <time.h>
#include "optical.h"
extern "C" {
#include <ieeeio.h>
};

//
// Main Program
//
int main()
{
      int           i,
                    current_minimum,
                    current_maximum,
                    samples;
      float         drive_current,
                    step_size,
                    signal;
      ofstream      fout("optical.out");

      // establish Personal488 connection - the variable ieee holds
```

```
        // the file handle for accessing the GPIB card after calling
        // ieeeinit()
        if( ieeeinit()==-1 )
        {
              cerr << "Unable to establish communication with"
                    << " Personal488 card."
                    << endl;
              exit(EXIT_FAILURE);
        }
        ILX     LDC_3900(ieee);
        SR      SR_510(ieee);

        // get current drive range and number of data points
        // desired from the user
        cout << "ILX  Lower current limit [mA]: ";
        cin >> current_minimum;
        cout << "     Upper current limit [mA]: ";
        cin >> current_maximum;
        cout << endl << "Number of samples: ";
        cin >> samples;
        cout << endl << endl << endl;

        // take data
        fout << "ILX[mA] SR[mV]" << endl;
        cout << "ILX[mA] SR[mV]" << endl;
        step_size = ( current_maximum - current_minimum ) / (samples-1);
        for( i = 0, drive_current=current_minimum; i < samples;
                    i++, drive_current += step_size)
        {
              LDC_3900.setpeak(drive_current);
              pause(3);
              signal = 1000 * SR_510.getsignal();
              fout << drive_current << " " << signal << endl;
              cout << drive_current << " " << signal << endl;
        }
        return 0;
}
```

```
////////////////////////////////////////////////////////////////////////
/
//
//      Class definitions for the ILX and SR classes.
//      A pause function is also included for
//      allowing GPIB access to be slowed
//
//      author:         Brian N. Strecker
//      date:           14 October, 1996
//      revision:       1.0
//
////////////////////////////////////////////////////////////////////////

#if !defined(__OPTICAL_H)
#define __OPTICAL_H

const float     SHORT_TIME=0.2;         // Pause time after a GPIB
command


////////////////////////////////////////////////////////////////////////
//
//
// Pauses for pause_time given in seconds
//
void pause( double pause_time)
{
  time_t          start, current;

  time(&start);
  do time(&current);
  while( difftime(current, start)<pause_time);
};
//
////////////////////////////////////////////////////////////////////////
//



////////////////////////////////////////////////////////////////////////
//
//
// ILX Lightwave Class definition and member functions
//
class ILX {
private:
  fstream         IEEE488;
  float           setpoint;
  float           current_output;

public:
  ILX( int);                    // constructor for class
  int reset();                  // n/a
  int on();                     // n/a
  int off();                    // n/a
  int setcurrent( float);       // change the setpoint (in mA)
  float getcurrent();           // read actual current (in mA)
```

```
  int setpeak( float);            // calculate and set the
  //   setpoint so that the
  //   peak current for a 50%
  //   duty cycle square wave
  //   modulated drive current
  //   is the the same as the
  //   value passed (in mA)
};

ILX::ILX( int file_handle)
  : IEEE488(file_handle) { }

int ILX::setcurrent( float desired_setpoint)
{
  setpoint = desired_setpoint;
  IEEE488 << "OUTPUT 10;LAS:LDI " << setpoint << endl;
  pause(SHORT_TIME);
  IEEE488 << "LOCAL 10" << endl;
  pause(SHORT_TIME);
  return 0;
}

float ILX::getcurrent()
{
  IEEE488 << "OUTPUT 10;LAS:LDI?" << endl;
  pause(SHORT_TIME);
  IEEE488 <<  "ENTER 10" << endl;
  pause(SHORT_TIME);
  IEEE488 >> current_output;
  pause(SHORT_TIME);
  IEEE488 << "LOCAL 10" << endl;
  pause(SHORT_TIME);
  return current_output;
}

int ILX::setpeak( float desired_current)
{
  float   real_current;

  setcurrent( desired_current);
  real_current = getcurrent();
  setpoint = 2 * ( desired_current - real_current );
  setcurrent( setpoint);
  return 0;
}

int ILX::reset() { return 0;}           // not implemented;
int ILX::on() { return 0;}              // not implemented;
int ILX::off() { return 0;}             // not implemented;
//
////////////////////////////////////////////////////////////////////////



////////////////////////////////////////////////////////////////////////
//
// Stanford Research Lock-In Class definition and member functions
```

```
//
class SR {
private:
  fstream          IEEE488;
  float            signal_strength;

public:
  SR( int);
  float getsignal();                // read the signal strength
  //    (in V)
};

SR::SR( int file_handle)
  : IEEE488(file_handle) { }

float SR::getsignal()
{
  IEEE488 << "OUTPUT 23;Q" << endl;
  pause(SHORT_TIME);
  IEEE488 <<  "ENTER 23" << endl;
  pause(SHORT_TIME);
  IEEE488 >> signal_strength;
  pause(SHORT_TIME);
  IEEE488 << "LOCAL 23" << endl;
  pause(SHORT_TIME);
  return signal_strength;
}
//
////////////////////////////////////////////////////////////////////////////
/

#endif  // __OPTICAL_H
```

```
////////////////////////////////////////////////////////////////
//      RWT2TXT.cpp

//

// Source code for a command which converts TENDOR P-1 *.rwt data files

// into 2 column ASCII.  Column 1 is the scan distance.  Column 2 is

// sample height.  Both values are given in microns.  The columns are

// separated by a space and each line is terminated by an endline.
//
//      Author:         Brian N. Strecker
//      Created:        22 October, 1996
//      Revision:       1.0
//
////////////////////////////////////////////////////////////////

#include <iostream.h>
#include <conio.h>
#include <stdlib.h>
#include <string.h>

//
// main program
//
int main( int argc, char * argv[])
{



      //

      // variable declarations

      //

      char            buffer[512];

      int             data_point = 0,

                      int_junk = 0;
      double          gain = 0.0,
                      horizontal_resolution = 0.0,
                      distance = 0.0,
                      height = 0.0;

      //
      // explain program usage unless -s switch sent
      //
      if( (argc!=2) || (strcmpi( argv[1],"-s")) )
      {

            cerr << "\nRWT2TXT.EXE is a file conversion program which"
                  << " accepts TENCOR P-1 profiler\n"
```

```
                << "            data in the form of a *.RWT file"
                << " and converts it to two column\n"

                << "            ASCII of scan-distance vs height"
                << " (both in microns) separated by a\n"

                << "            space and terminated by an endline."
                << "  The program takes input from\n"

                << "            the console and sends output to"
                << " the console.  Use -s to turn off\n"
                << "            this message.\n\n"
                << "Usage:  TYPE FILEIN.RWT | RWT2TXT.EXE -s >"
                << " FILEOUT.TXT\n";

        exit(EXIT_FAILURE);

};



//

// read and throw away the first 9 lines of the input

//

for( int i=1; i<10 ; i++) { cin.getline( buffer,256); };

//
// get setup data for the file to allow the data point values
// to be converted to height and horizotal distance values.

//

cin >> int_junk;

cin >> int_junk;

cin >> gain;

cin >> horizontal_resolution;

//
// read in lines, process, and send to cout
//

// end program on eof

while( !cin.eof())
{
        // clear up previous line

        cin.getline( buffer, 512);

        cin >> int_junk;
```

```
            // end conversion on endl or eof

            while( (cin.peek()!='\n') && (!cin.eof()) )
            {

                  // height = data_point *  gain / 10000.0;

                  cin >> data_point;
                  cout << distance << ' ' << height << endl;

                      distance += horizontal_resolution;

             };
      };


      return 0;

};
```

```
' Original Source code:          IV.bas
' Creation Date:                 ?/?/92
' Original Author:               John Hassel
' Editors:                       Roy, Rob, Derrick
' Last Editor:                   Brian Strecker
' Last Edit Date:                8/22/96
' Executable Code:               IV.exe
'
' Description:  Quick Basic source code for a Keithley 224 current
'     source with an optional 2243 IEEE Interface and a Keithley 195A
'     digital multimeter via a microchannel bus IOTech Personal488
'     GPIB card.   Program varies the ouput current of the 224
'     source from the minimum to the maximum current specified by the
'     user.  The current is stepped linearly form min to max by an
'     an increment determined by the number of data points requested
'     by the user.  The voltage at each point is read from the 195A
'     multimeter and displayed graphically.  Voltage scale for the
'     display is set by the user.  The current and voltage points are
'     stored in a temporary file.  A copy of this file is made by the
'     program if the user provides a filename when prompted.
'
' Editor Info:  The filenames in the source code are set up to
'     read/write from/to the default drive.  When compiling to
'     create an executable, set the radio button in the Make EXE
'     window to "Stand Alone EXE" (See the QuickBasic manual for
'     details.)  No error checking is provided by this program.
'     If you enter voltage/current parameters which are not
'     acheivable by the meter/current supply, the program
'     will NOT trap them.
'
' User Info:    1) The program runs from the default directory.  If you
'                  start it from C:\, it will store all its data in C:\.
'                  Running it from a hrad drive will result in slightly
'                  faster run times but will clutter the directory with
'                  temporary files.  I recommend running it from a sub-
'                  directory to avoid this.
'               2) The program expects to find a file named IV.IN
'                  in the default directory.  If you want to run the
'                  program from C:\MYDIRECT, make sure that a copy of
'                  IV.IN is in C:\MYDIRECT.  IV.IN holds the
'                  range settings for the previous run.  This leads to
'               3) Please keep the source code, the executable file,
'                  and the IV.IN files together when you transfer
'                  the program from place to place.  The source file
'                  will be needed by the next guy to use the system,
'                  since you will most likely be too busy to show him/
'                  her how to use it or you will have forgotten how.
'                  The program will also need to be changed in future
'                  the source code will speed this up.
'               4) Since the program must run on a PS/2 system and the
'                  hard drives in these systems are notoriously short
'                  lived, I recommend keeping a couple copies of the
'                  three files mentioned above on floppies in different
'                  places.  The executable, source code, and data file
'                  are small enough to fit (along with the system files
'                  needed to boot the computer) on a single 720 KB disk.
'                  The computer can be booted from the A: drive and the
```

```
'                 program run from it.
'
'

'PROGRAM BEGINS HERE
'
' Subroutines
'
DECLARE SUB PlotRootLocus (StartGain!, MaxGain!, MaxX!, RLMFile$,
status$, zeros!(), zerocount!, poles!(), polecount!, gain!,
Characteristic!, characteristicorder!, Volt, I, rzero!(), szero!(),
done!, RlmFileNum)
DECLARE SUB WaitForKey (stroke$)
DECLARE SUB MakeWorld (XMax, XMin, YMax, YMin)
DECLARE SUB DrawWindowAndScales (XMax, XMin, YMax, YMin)

'
' variable declarations
'
DIM rzero(30), szero(30), Volt(30), I(30)
DIM Characteristic(30), ZBackHue(11)
DIM poles(30, 30), zeros(30, 30)
DIM oldreal(30), oldimag(30)

'
' load user inputs from previous run
'
CLS
OPEN "IV.IN" FOR INPUT AS #4
INPUT #4, MinX, MaxX, MinY, MaxY, NumberofSteps
CLOSE #4

'
' get user values for this run for setting up the I-V display
'
PRINT "IV.EXE controls a current source and multimeter to produce a
plot of"
PRINT "the I-V characteristics of a device.  I-V data is tab-separated
and"
PRINT "stored as IV.OUT.  The graph image is stored as IV.CGA.  For
more"
PRINT "information, please examine the source code file IV.BAS"
PRINT
PRINT
PRINT "MIN display voltage [default = "; MinX; " V] ";
INPUT ""; a$
IF a$ <> "" THEN MinX = VAL(a$)

PRINT "MAX display voltage [default = "; MaxX; " V] ";
INPUT ""; a$
IF a$ <> "" THEN MaxX = VAL(a$)

PRINT "MIN applied current [default = "; MinY; " uA] ";
INPUT ""; a$
IF a$ <> "" THEN MinY = VAL(a$)

PRINT "MAX applied current [default = "; MaxY; " uA] ";
```

```
INPUT ""; a$
IF a$ <> "" THEN MaxY = VAL(a$)

PRINT "Number of y-axis steps [default = "; NumberofSteps; "] ";
INPUT ""; a$
IF a$ <> "" THEN NumberofSteps = VAL(a$)

'
' store user inputs for next run
'
OPEN "IV.in" FOR OUTPUT AS #4
PRINT #4, MinX, MaxX, MinY, MaxY, NumberofSteps
CLOSE #4

'
' draw I-V display grid
'
SCREEN 2
status$ = "Waiting For Key"
CALL DrawWindowAndScales(MaxX, MinX, MaxY, MinY)

'
' establish communications with Personal488
'
OPEN "\DEV\IEEEOUT" FOR OUTPUT AS #1
IOCTL #1, "BREAK"
PRINT #1, "RESET"
OPEN "\DEV\IEEEIN" FOR INPUT AS #2
PRINT #1, "FILL ERROR"

'
' disable SRQs
'
PRINT #1, "OUTPUT 16;M0X"
PRINT #1, "OUTPUT 02;M0X"

'
' main loop
'
again:
a$ = ""
I = MinY * .000001
CountSize = (MaxY - MinY) / NumberofSteps
OPEN "IV.out" FOR OUTPUT AS #4

'
' step the current from it's minimum value to it's maximum value
'   but stop if a key is pressed
'
WHILE (I <= MaxY * .000001 AND a$ = "")
    FOR I = MinY * .000001 TO MaxY * .000001 STEP CountSize * .000001
      a$ = INKEY$
      PRINT #1, "OUTPUT 02"
      PRINT #1, "I" + STR$(I) + "X"
      PRINT #1, "ENTER 16"
      INPUT #2, R$
      Volt = VAL(MID$(R$, 5))
```

```
        LOCATE 2, 3
        PRINT USING "+#.###^^^^"; I * 1000000;
        PRINT " " + CHR$(230) + "A  ";
        LOCATE 3, 3
        PRINT USING "+#.###^^^^"; Volt;
        PRINT " Volts"
        PRINT #4, I * 1000; "    ", Volt
        CALL PlotRootLocus(StartGain, MaxGain, MaxX, RLMFile$, status$,
zeros(), zerocount, poles(), polecount, gain, Characteristic,
characteristicorder, Volt, I * 1000000, rzero(), szero(), done,
RlmFileNum)
     NEXT
WEND

'
' reset the current source
'
PRINT #1, "OUTPUT 02"
PRINT #1, "I0X"
'***************'
CLOSE #4

'
' blank out the current and voltage display on the graph
'
LOCATE 2, 3
PRINT "                        "
LOCATE 3, 3
PRINT "                        "

'
' store the graphic page
'
DEF SEG = &HB800
BSAVE "IV.cga", 0, &H4000

'
' wait for keypress to end
'
WHILE INKEY$ = "": WEND
CLS

SUB DrawWindowAndScales (XMax, XMin, YMax, YMin)
'This SubProgram will draw and configure the plotting portion of the
'graphical screen.  Input XNegBorder is the maximum negative value of x
that
'can be displayed on the viewscreen.  Likewise with the other input
'parameters.  Output is the displayed window with axes and hash marks
'drawn.

CALL MakeWorld(XMax, XMin, YMax, YMin)


XNegBorder = XMin
XPosBorder = XMax
YNegBorder = YMin
YPosBorder = YMax
```

```
' This Group of Statements Moves the printing of the Y axis values so
they will print next to the Y axis

Vdrop = (XMax - XMin) / 80          'Vdrop is set to equal the voltage
drop per space
countx% = 0                           'Y is the counting variable that
tells the computer how many spaces to move before drawing the Y-Axis
X = XMin                         'X is the counting variable that
determines when the X values are zero
DO WHILE X < 0
      countx% = countx% + 1
      X = X + Vdrop
LOOP
countx% = countx% + 1

' This group of statements moves the printing of the X axis values so
they will print next to the X Axis

Vdrop = (YMax - YMin) / 23
county% = 0
Y = YMin
DO WHILE Y < 0
      county% = county% + 1
      Y = Y + Vdrop
LOOP
county% = 25 - county%

LINE (XNegBorder, 0)-(XPosBorder, 0)   'Draw X-Axis
LINE (0, YNegBorder)-(0, YPosBorder)   'Draw Y-Axis

LOCATE 6, countx%
PRINT YPosBorder / 2;
PRINT "uA"

LOCATE 18, countx%
PRINT YNegBorder / 2;
PRINT "uA"

LOCATE county%, 69
PRINT USING "#.##"; XMin + 70 * (XMax - XMin) / 80;
PRINT "V"

LOCATE county%, 47.5
PRINT USING "###.##"; XMin + 50 * (XMax - XMin) / 80;
PRINT "V"

LOCATE county%, 28.5
PRINT USING "###.##"; XMin + 30 * (XMax - XMin) / 80;
PRINT "V"

LOCATE county%, 7.5
PRINT USING "###.##"; XMin + 10 * (XMax - XMin) / 80;
PRINT "V"


LOCATE 2, 39
```

```
PRINT "I";
LOCATE 2, 41
IF YMax > 1000 THEN
      PRINT USING "###.#"; YMax / 1000;
      PRINT "mA"
ELSE
      PRINT USING "####.#"; YMax;
      PRINT CHR$(230) + "A"
END IF

'span = (XPosBorder - XNegBorder) / 100
'FOR c = YNegBorder TO YPosBorder STEP ((YPosBorder - YNegBorder) / 4)
'Draw Y-Axis hash lines
'   LINE (0, c)-(span, c)
'NEXT c


END SUB

SUB MakeWorld (XMax, XMin, YMax, YMin)
VIEW (2, 1)-(635, 180), , 2  'put view window in the lower left corner
of EGA screen

XNegBorder = XMin
XPosBorder = XMax

YNegBorder = YMin
YPosBorder = YMax

WINDOW (XNegBorder, YNegBorder)-(XPosBorder, YPosBorder) ' "Normalize"
the view screen

END SUB

SUB PlotRootLocus (StartGain, MaxGain, MaxX, RLMFile$, status$,
zeros(), zerocount, poles(), polecount, gain, Characteristic,
characteristicorder, Volt, I, rzero(), szero(), done, RlmFileNum)
          PSET (Volt, I)
END SUB

SUB WaitForKey (stroke$)

stroke$ = ""

WHILE stroke$ = ""
    stroke$ = UCASE$(RIGHT$(INKEY$, 1))
WEND

END SUB
```

IMAGE EVALUATION TEST TARGET (QA-3)

150mm

6"

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