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YEONG-WEN HWANG

Norman, Oklahoma

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A THIN-FILM DISTRIBUTED AMPLIFIER USING TRANSMISSION LINES

AND MOS TRANSISTORS

APPROVED BY

Stanley E. Babb, Jr.

DISSERTATION COMMITTEE

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CHAPTER I

INTRODUCTION

There are increasing demands for extremely broadband amplifiers. Conventional amplifiers have been shown to have a maximum gain-band width product for a given tube or transistor type, no matter how complex the coupling system between stages. Aside from this limitation, any attempt to exceed much more than 50% of the theoretically obtainable maximum will meet practical difficulties. The traveling-wave technique has provided a means for wide-band amplification at microwave frequencies. The traveling-wave tube must be electrically long, and practical limitations make it improbable that such tubes will be available for frequencies much below 1 GC.

The gain-band width product for conventional amplifiers can be expressed as

$$G \cdot BW = \frac{g_m}{2\pi(C_g + C_p)} \tag{1}$$

where g_m is the transconductance of the device, C_g and C_p are its input

and output capacitances. Parallel connection of the active devices does not help the gain-band-width product since as g_m is increased, capacitances are also increased by the same parallel connection.

A distributed amplifier utilizes sections of inductors and capacitors in both its input and output circuits. These sections serve as filters and artificial delay lines. As the signal flows to the load, g_m's add but C_g's and C_p's are separated by these sections. The conventional restrictions on gain-band-width are completely removed, thus the high frequency limit being determined entirely by effects within the device proper.

Distributed amplification has been employed in video and broadband amplifiers using vacuum tubes,[1-9] and it has also been used with transistors.[10,11] A problem encountered in the use of transistors with distributed amplifiers is the difficulty in designing fixed input impedance over the very broad frequency range of these amplifiers.[10] This together with the low input impedance of transistors requires special networks for compensation, limits the impedance of input filters to low values and reduces the gain in cascaded amplification.

This paper describes the development of the characteristics and design equations for distributed amplification using transmission lines and field-effect transistors. In Chapter III, the design of a thin-film distributed amplifier using strip lines and metal-oxide-semiconductor (MOS) transistors is discussed in detail.

Since the distributed amplification is actually accomplished by applying traveling-wave concepts to the lower frequency region, it is proposed to use a transmission line for distributed amplification

instead of traditional lumped inductors and capacitors. When the line is loaded by transistor capacitances, it then behaves partly like π-filter sections.

A transmission line section can be approximated by a π-network having series inductance and shunt capacitance elements, the latter combining with the loading capacitances to form a filter. This result is used in the first step of the design, but this is true only when the line is very short or the frequency is very low. At cutoff frequency, the phase shift per section is as high as 180 degrees, although this should be attributed to both the transmission line and the loading capacitances. On the high frequency side of the amplified band, the line is usually not very short. More exact formulas are calculated and compared with the lumped filter amplifier. Differences in characteristics between the distributed line type and the lumped type are discussed, with the former showing better performance.

The relation between phase shift and frequency is non-linear for the lumped filter as indicated in equation (5), of Chapter II. As a lossless transmission line gives no phase shift distortion, the behavior of the transmission line distributed amplifier is somewhat modified. It will be shown that the filter made of a transmission line and the loading capacitances has better phase shift characteristics than the lumped filter sections. This then is a method of improving the frequency response, the use of which is not limited to the thin-film case. A more linear phase shift is particularly important in case a large number of stages are to be cascaded.

The impedance of the lumped filter increases appreciably with frequency and near cutoff, a large undesired peak is produced. The transmission line filter has smaller impedance variation over the pass band, therefore a smoother amplitude response can be expected. The cutoff frequency of the transmission line filter is higher than that calculated from its lumped model, the peak is shifted to the right and its frequency coverage is narrowed. By choosing slightly different lengths of transmission line sections for the input and output circuits, it is possible to reduce the peaking effect by the phase shift difference between them near cutoff.

A transmission line is more readily realized than an inductor in a thin-film circuit since the amount of inductance that can be conveniently put into thin-film circuit is quite limited. It is difficult to make a pure inductor without introducing an appreciable amount of stray and distributed capacitance.

The length of the transmission line to be used is important. Unloaded smooth lines will be rather long for the substrate at the frequency of interest, however the loading capacitances of MOS transistors will reduce the length of line required. It is convenient to use silicon monoxide as the dielectric medium which further reduces the line length. Strip sandwich line will be used here because of its adaptation for deposition processes and high isolation characteristic between lines. The almost perfect shield of the sandwich line eliminates the isolation problem between input and output circuits which must otherwise be given careful consideration.

The field-effect transistor has high input impedance and

vacuum-tube-like characteristics. For MOS transistors, the input resistance is normally 10^9 to 10^{15} ohms, much higher than junction gate field-effect transistors. The MOS transistors are most easily fabricated by thin-film techniques.

Through microelectronic miniaturization, the proposed amplifier will not have those annoying problems encountered by ordinary distributed amplifiers. At frequencies near cutoff, the distributed amplifier is very sensitive to stray capacitances, lead wire inductances, oscillation, etc. This leads to an almost unpredictable behavior of the amplifier near cutoff. By miniaturization stray capacitances are reduced to a minimum and are fixed.

Lead inductance (inside and outside the tubes) in the grid and plate circuits of vacuum tubes has the effect of reducing the cutoff frequency and producing a peak near cutoff. The effect of the cathode lead inductance is even more serious.[1] This inductance, in conjunction with the grid-to-cathode capacitance, produces an input grid conductance which causes a grid loading effect. Self resonance of the lumped coils, attributable to capacitance between coil windings, yields limited amplifier performance at high frequencies.[6]

The thin-film amplifier eliminates all these effects by having the shortest leads possible. The highest frequency of the present amplifier is designed to be 100MC. This is a result of considerations of the transconductance fall off of the MOS transistors. Modifications for application in the UHF range can be readily verified. Detailed circuit and layout are designed with performance predicted.

CHAPTER II

THEORY

AMPLIFIER

The distributed amplifier principle, first disclosed by Percival,[12] was extensively discussed by Ginzton et. al. in 1948. In the following few years, there was active interest in this principle and numerous accounts of the design and performance were written. Since that time there has been little reference to this method of broadbanding, presumably due to the attention focused upon the then newly developing transistor, which does not seem to be as suitable for distributed amplification as the vacuum tube. As noted in the introduction, there is difficulty in designing a fixed input impedance over the broad frequency range for the transistor. Enloe and Rogers[11] have considered the problem and have succeeded in treating the transistor impedance as one similar to that of a tube for the tube formulas to hold. Beneteau and Blaser[10] have made an elaborate analysis of transistor input impedances and have designed a special network for emitter compensation of each transistor. The MOS transistor, however, can be readily adopted in the design of distributed amplifiers.

A single stage distributed amplifier using vacuum tubes is shown in Fig. 1. Two artificial lines made of filter sections are in

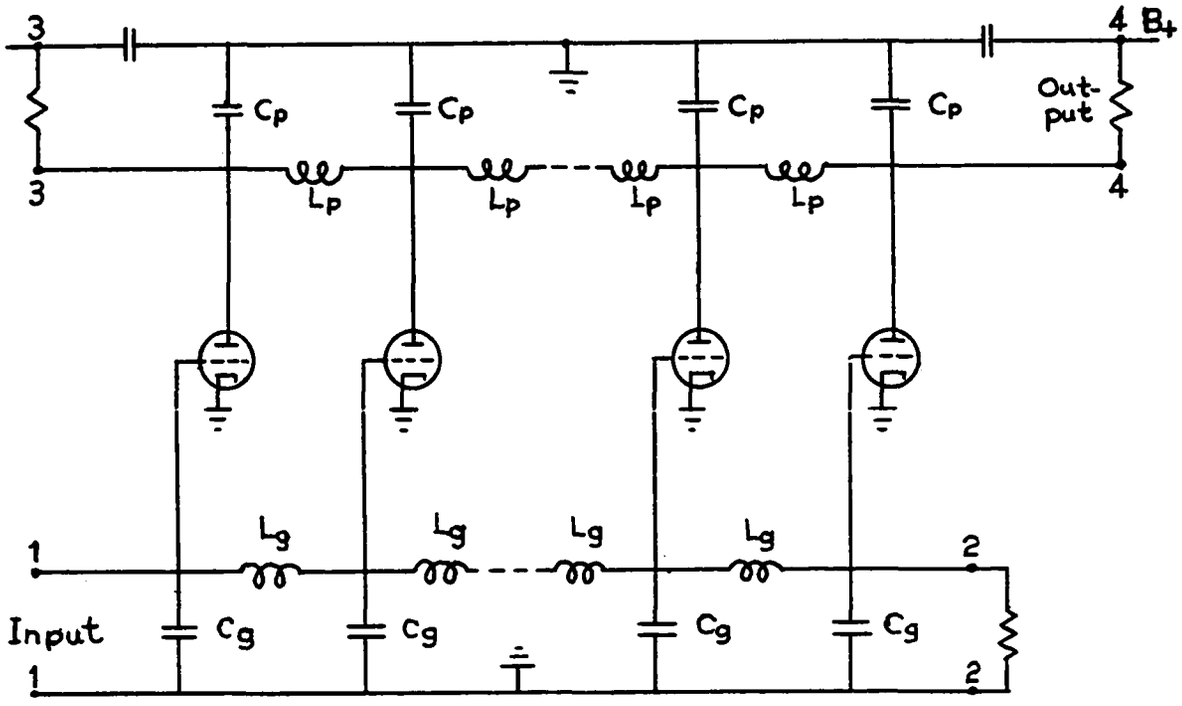


Fig. 1. Basic distributed amplifier using vacuum tubes

the grid and plate circuits. The input signal passes through filter sections in the grid line to reach a grid. The amplified output signal also passes filter sections in the plate line to reach the load. No matter what path the signal may take from input to output, the same number of sections, equal to the number of active elements in the stage, is always passed. If the phase shift per section is the same, the signal will reach the load in phase, having an additive effect. The output voltage is therefore directly proportional to the number of tubes.

The artificial line shown is formed by π-section constant k filters with coil L_g (or L_p) as series element and $\frac{1}{2}C_g$ (or $\frac{1}{2}C_p$) at both ends as shunt elements. The image impedance of the π-network is

$$Z_\pi = \frac{\sqrt{Z_1 Z_2}}{\sqrt{1 + \frac{Z_1}{4Z_2}}}, \qquad (2)$$

where Z_1 and Z_2 are series and shunt impedances respectively. The

cutoff frequency, occurring when Z_π is infinite, is

$$f_c = \frac{1}{\pi\sqrt{LC}} \qquad (3)$$

where L, C are the total series inductance and shunt capacitance. The image phase shift per filter section θ at frequency f (angular frequency ω) of the lossless π-network in the pass band is given by

$$\cos\theta = 1 + \frac{Z_1}{2Z_2} \quad , \qquad (4)$$

or for the present case,

$$\cos\theta = 1 - \tfrac{1}{2}\omega^2 LC = 1 - 2\left(\frac{f}{f_c}\right)^2 \quad . \qquad (5)$$

It should be noted that the phase shift at the cutoff frequency is 180 degrees. For equal phase shift per section the cutoff frequency of the two artificial lines should be the same. Thus, from (3):

$$L_g C_g = L_p C_p \qquad (6)$$

and

$$f_c = \frac{1}{\pi\sqrt{L_g C_g}} = \frac{1}{\pi\sqrt{L_p C_p}} \quad . \qquad (7)$$

Formula (2) is then

$$Z_1 = \frac{\sqrt{\frac{L_g}{C_g}}}{\sqrt{1-\left(\frac{f}{f_c}\right)^2}} \quad , \qquad (8)$$

$$Z_2 = \frac{\sqrt{\frac{L_p}{C_p}}}{\sqrt{1-(\frac{f}{f_c})^2}} \qquad (9)$$

where Z_1 and Z_2 as before are image impedances of the input and output filter lines respectively. At low frequencies, these image impedances reduce, using (8) and (9), to:

$$R_1 = \sqrt{\frac{L_g}{C_g}} \ , \qquad (10)$$

$$R_2 = \sqrt{\frac{L_p}{C_p}} \ . \qquad (11)$$

If the grid filter chain is terminated at this image impedance, and if the line is dissipationless and without grid loading, the driving-point impedance at terminals 1-1 is independent of the number of tubes so connected. In a like fashion, the impedance which the tube plate sees is independent of the number of tubes. The plate filter sections are terminated at both ends with resistances equal to R_2. The amplified signal in the plate circuit will flow in both directions, being divided equally and absorbed. The impedance connected to terminals 2-2 is called the grid termination. That connected to terminals 3-3 and 4-4 are called the reverse termination and output termination (or load) respectively. Practically, the reverse termination can be removed without deteriorating effect and doubles the gain.[3]

The effective g_m of this distributed stage may be increased to any desired limit theoretically. Thus, no matter how low the gain of each section is (even if it is less than unity), the output will increase as one desires by merely using a sufficient number of sections. The distributed amplifier stage can be used alone or when sufficient gain has been accumulated in one stage, such stages can be cascaded. For different plate and grid image impedances, matching networks can be utilized between stages. Fig. 2. shows a way of direct coupling. The series inductor combines with shunt capacitance to form a matching network. The series capacitor serves to block the direct current.

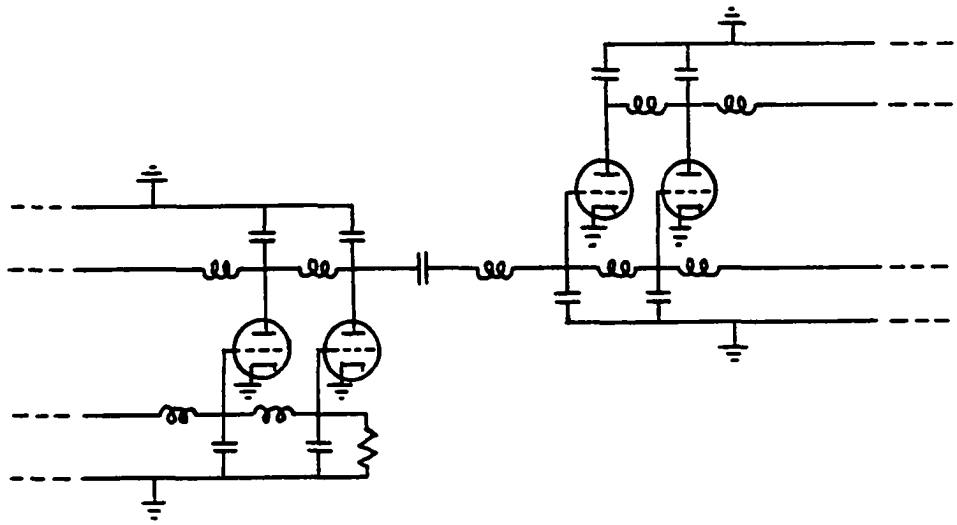


Fig. 2. Two stage distributed amplifier showing direct coupling

The distributed amplifier is the only means available for amplification when the maximum frequency desired is greater than the band width index frequency (where gain is unity) of the active device being used. With conventional circuits, it is usually found to be impractical to achieve much more than 50% of the theoretically available band width.

This is because the theoretical limit requires the use of extremely complex coupling circuits, which can hardly be considered practical and which increase the stray capacitance to ground. This is not the case in the distributed amplifier.

The basic filter sections shown in Fig. 1. and Fig. 2. are low-pass structures. The theoretical band is from the cutoff frequency down to zero frequency. In practical circuits, the response at the low frequency end is limited by the decoupling capacitors inserted for d-c biasing purpose. The distributed amplifier can be made to operate at frequencies down to d-c by using standard d-c amplifier techniques. It is obvious that the principle is equally applicable to band-pass filters since they also have capacitors as their shunt elements as shown in Fig. 3. The grid bias supply for the active device in band-pass applications must go through a separate choke.

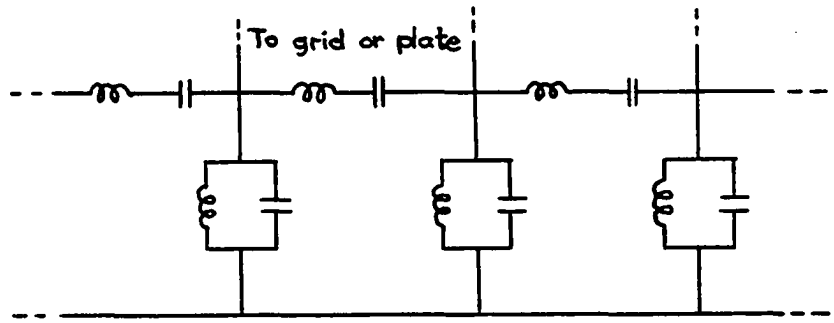


Fig. 3. Band-pass filter chains

The voltage gain A for a single distributed amplifier stage is

$$A = \frac{ng_mZ_2}{2} \tag{12}$$

where n is the number of sections in the stage and the output filter impedance Z_2 is much less than the plate resistance of the tube.

When the stage is cascaded, a transmission coefficient enters if the impedances of input and output circuits are different. It is proportional to the square root of the impedance ratio. When this is included, the gain of the amplifier consisting of n sections per stage and m cascaded stages can be expressed as

$$A = \left[\frac{ng_m}{2}\sqrt{Z_1 Z_2}\right]^m . \tag{13}$$

If the two impedances are equal, then for a low-pass amplifier,

$$Z_1 = Z_2 = \frac{R_o}{\sqrt{1-x_k^2}} \tag{14}$$

where

$$x_k = \frac{f}{f_c} \tag{15}$$

$$R_o = R_1 = R_2 = \sqrt{\frac{L}{C}} = \frac{1}{\pi f_c C} . \tag{16}$$

C is the total shunt capacitance per section. Under this condition, the gain equation becomes

$$A = \left[\frac{ng_m R_o}{2}\right]^m (1-x_k^2)^{-\frac{m}{2}} \tag{17}$$

and the gain of a single stage is

$$A = \frac{ng_m}{2} \frac{R_o}{\sqrt{1-x_k^2}} . \tag{18}$$

It is well known that the series resistance and shunt conductance

will produce attenuation in a filter. A good approximate equation is[13]

$$\alpha = \frac{x_k}{2}\left(\frac{1}{Q_C} + \frac{1}{Q_L}\right)\frac{d\theta}{dx_k} \tag{19}$$

$$\alpha = \frac{1}{4\pi f_c}\left(\frac{G}{C} + \frac{R}{L}\right)\frac{d\theta}{dx_k} \tag{20}$$

where

α = attenuation in nepers per section

x_k = the normalized frequency function

Q_C = the Q of the capacitors

Q_L = the Q of the coils

θ = the phase shift per section in radians

G = the shunt conductance across the capacitance C

R = the series resistance with inductance L

f_c = the cutoff frequency.

The first and second terms are obviously due to shunt and series losses respectively. The attenuation increases rapidly near cutoff as $d\theta/dx_k$ increases. The value of $d\theta/dx_k$ can be obtained from equation (5) and (15) for the low-pass filter case

$$\frac{d\theta}{dx_k} = \frac{2}{\sqrt{1-x_k^2}} \tag{21}$$

and is approximately equal to 2 for the low frequency case.

The delay time, τ, per section is given by

$$\tau = \frac{d\theta}{d\omega} = \frac{1}{\omega_c}\frac{d\theta}{dx_k} = \frac{2}{\omega_c\sqrt{1-x_k^2}} . \tag{22}$$

An important cause of grid loading is the effect of the cathode lead inductance L_c in conjunction with the grid-to-cathode capacitance C_{gc}. This grid (input) conductance is given by[14]

$$G = g_m \omega^2 L_c C_{gc}. \tag{23}$$

The ratio of output voltages with and without this input conductance loss can be expressed as[1]

$$\frac{E_{out} \text{ with input loss}}{E_{out} \text{ without input loss}} = 1 - \frac{A}{4} \frac{G}{g_m} \frac{d\theta}{dx_k} \tag{24}$$

where A is gain of the stage and G is the total grid (input) loading conductance.

Let us now consider a distributed amplifier using transmission line sections and MOS transistors as shown in Fig. 4. C_G and C_D are the gate and drain line loading capacitances.

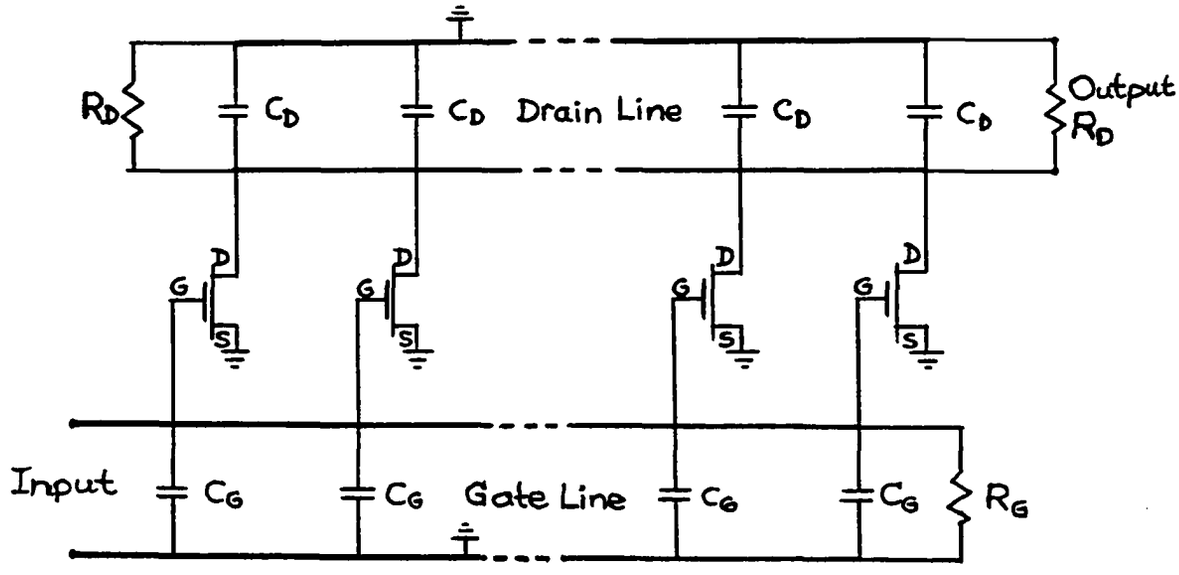


Fig. 4. Basic distributed amplifier using transmission line and the MOS transistors

A section of transmission line can be represented by an equivalent π-network as shown in Fig. 5.,

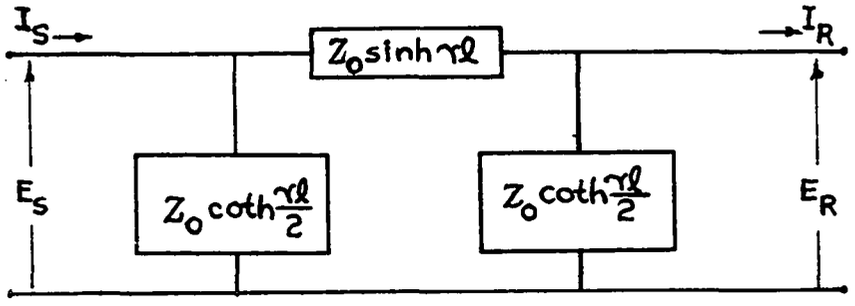


Fig. 5. Equivalent π-network for the transmission line

where Z_o, γ, ℓ, are the characteristic impedance, propagation constant and sectional length of the transmission line respectively. The equivalent circuit will yield the same phase shift, attenuation and terminal voltage current relations for the steady-state condition. The values of the elements in the equivalent circuit are functions of frequency. Thus, Z_0 and γ will generally change with frequency. For a lossless line, Z_0 is fixed and γ is equal to $j\beta$:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{25}$$

$$\gamma = j\beta = j\omega\sqrt{LC}. \tag{26}$$

Here L, C are the inductance and capacitance per unit length of the line. The equivalent network for the lossless line section is then as shown in Fig. 6.

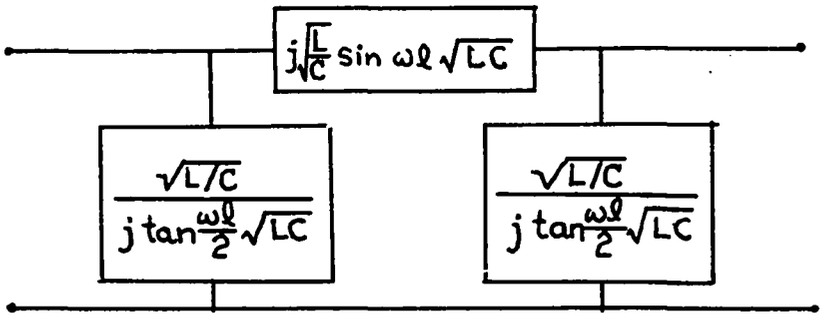
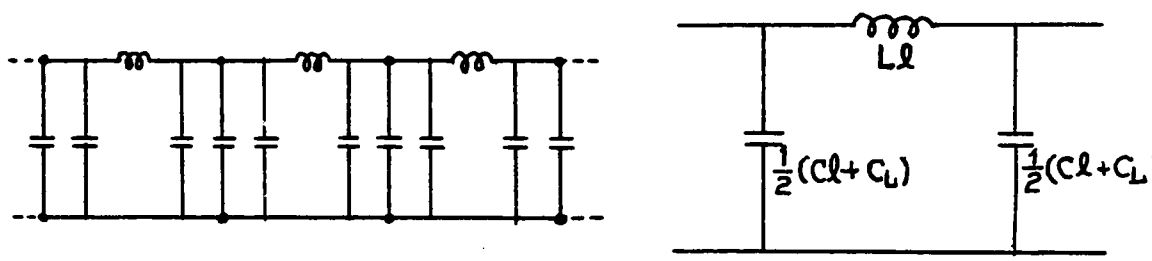


Fig. 6. Equivalent π-network for the lossless transmission line

Near the low frequency end of the pass band of the distributed amplifier where $\sin\omega\ell\sqrt{LC} \approx \omega\ell\sqrt{LC}$ and $\tan\frac{\omega\ell}{2}\sqrt{LC} \approx \frac{\omega\ell}{2}\sqrt{LC}$ the equivalent network can be further reduced to a lumped L, C network. The transmission line is connected to the MOS transistors at equal intervals. The internal capacitances of the transistors load the line, as shown in Fig. 7(a), producing an effect analogous to the inductive loading of a telephone line. The degree of loading (smoothness of line) depends on the loading interval.[15,16] These discontinuity points cause the line to have a filter characteristic.



(a) (b)

Fig. 7. Capacitively loaded line

Let C_L be the loading capacitance per section (transistor). This capacitance is divided and combined with the low frequency equivalent π-network, forming still another π-network, as shown in Fig. 7(b).

The cutoff frequency is roughly estimated by

$$f_c = \frac{1}{\pi\sqrt{L\ell(C\ell+C_L)}}, \qquad (27)$$

since at cutoff frequency the approximation leading to Fig. 7(b) may not be true.

The low frequency limit of the impedance is

$$Z_{\pi} = \sqrt{\frac{L}{C+(C_L/\ell)}} . \tag{28}$$

The low frequency gain of the one-stage amplifier is

$$A = \frac{ng_m}{2}\sqrt{\frac{L}{C+(C_D/\ell)}} . \tag{29}$$

In general, the substitution of $L'=L\ell$ and $C'=C\ell+C_L$ in the previous equations for lumped filters will yield approximations for low frequencies.

The line length per section can be obtained as follows. The LC product, related to the phase velocity of the wave, is a constant:

$$v = \frac{1}{\sqrt{LC}} \tag{30}$$

and

$$v = \frac{1}{\sqrt{\epsilon\mu}} = \frac{c}{\sqrt{K\mu_r}} \tag{31}$$

where

v = phase velocity in meters per second

ϵ = permittivity of the medium

μ = permeability of the medium

c = velocity of light

K = dielectric constant

μ_r = relative permeability.

From (30) and (31),

$$LC = \frac{K\mu_r}{c^2} . \tag{32}$$

From (27),

$$L\ell(C\ell + C_L) = \frac{1}{\pi^2 f_c^2} . \tag{33}$$

Combining (32) and (33), the line length equation is

$$\frac{K\mu_r}{c^2}\ell^2 + C_L L\ell - \frac{1}{\pi^2 f_c^2} = 0 . \tag{34}$$

Since the characteristic impedance of the line Z_o is

$$Z_o = \sqrt{\frac{L}{C}} = vL , \tag{35}$$

it is seen from equation (34) that for higher dielectric constant, permeability, loading capacitance or characteristic impedance, shorter ℓ can be used, as practical considerations such as the size of the amplifier may dictate. It will be seen, however, that longer ℓ gives better performance. In practice, therefore, a compromise will be reached.

Consider now the equivalent network of Fig. 6. The loading capacitors, equal to $C_L/2$, are to be added at both ends. Combining the shunt elements with the shunting capacitors yields a network shown in Fig. 8.,

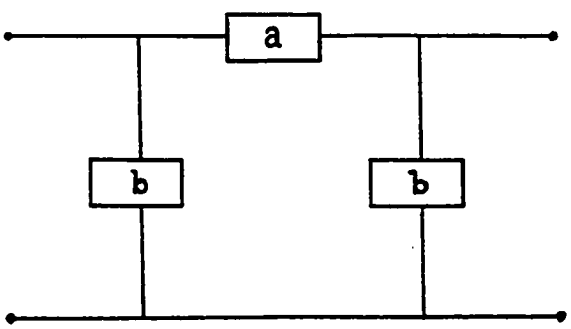


Fig. 8. Equivalent network for the loaded transmission line section

where a is the series impedance which is

$$a = j\sqrt{\frac{L}{C}}\sin\omega\ell\sqrt{LC} \ , \tag{36}$$

and b is the shunt admittance which is

$$b = j\left(\sqrt{\frac{C}{L}}\tan\frac{\omega\ell}{2}\sqrt{LC} + \frac{\omega C_L}{2}\right) . \tag{37}$$

The phase shift per section of this network is given by

$$\cos\theta = 1 + \frac{Z_1}{2Z_2} = 1+ab \tag{38}$$

$$= 1-\sin\omega\ell\sqrt{LC}\tan\frac{\omega\ell}{2}\sqrt{LC} - \frac{\omega C_L}{2}\sqrt{\frac{L}{C}}\sin\omega\ell\sqrt{LC} . \tag{39}$$

Use of the trigonometric identity $1-\sin\varphi\tan\frac{\varphi}{2} = \cos\varphi$ yields the equation

$$\cos\theta = \cos\omega\ell\sqrt{LC} - \frac{\omega C_L}{2}\sqrt{\frac{L}{C}}\sin\omega\ell\sqrt{LC} \ . \tag{40}$$

The actual cutoff frequency occurring when θ is 180°, will not be the lumped cutoff frequency f_c (i.e., the cutoff frequency if the line is replaced by a fixed LC network), but it will be expressed in term of x_k which is a relative measure of frequency with reference to f_c.

Let

$$C_L = C'\ell \tag{41}$$

where C' would be the loading capacitance per meter if it were uniformly distributed. By defining a loading ratio or loading percentage k,

$$k = \frac{C'}{C}, \tag{42}$$

the lumped cutoff frequency can be expressed as

$$f_c = \frac{1}{\pi\sqrt{L\ell(C\ell+C'\ell)}}$$

$$f_c = \frac{1}{\pi\ell\sqrt{LC}\sqrt{1+k}} \tag{43}$$

or

$$\sqrt{1+k} = \frac{1}{\pi\ell f_c \sqrt{LC}}$$

$$\sqrt{1+k} = \frac{2}{\omega_c\sqrt{LC}\,\ell} = \frac{2}{\beta_c\ell}$$

$$\sqrt{1+k} = \frac{2}{\phi} \tag{44}$$

where

ϕ = the angular length of the section of the line at the lumped cutoff frequency, i.e., the phase shift per sectional length of a pure unloaded line at f_c.

ω_c = the lumped angular cutoff frequency.

β_c = the phase shift constant of the line at the lumped cutoff frequency.

Thus, the relation between k and ϕ is

$$\phi = \frac{2}{\sqrt{1+k}} \tag{45}$$

or
$$k = \frac{4}{\phi^2} - 1 \quad . \tag{46}$$

It is seen that the angular length of the sectional line needed for the distributed amplification is a function of the loading percentage only. It is independent of the cross-sectional geometry of the line, i.e., the shape and spacing, the L/C ratio or the impedance level.

It is interesting to notice that for values of ϕ greater than 2, k will be negative. This indicates a limit on the sectional length of the line. The useful sectional angular length of the line is between zero and 2 radians at the lumped cutoff frequency f_c unless the loading capacitance is negative.

Equation (45) shows that in order for the lumped model of Fig. 7 to yield a good approximation, the loading ratio needs to be around a hundred or more, as is the case of telephone inductive loading. This is, however, seldom the case for the distributed amplifier in view of the low value of the input capacitance of the active device.

Since
$$\begin{aligned} \omega \ell \sqrt{LC} &= \frac{f}{f_c} \omega_c \ell \sqrt{LC} \\ &= \phi x_k \ , \end{aligned} \tag{47}$$

the substitution of equations (41), (42) and (45) into equation (40) will yield the result:

$$\begin{aligned} \cos\theta &= \cos(\phi x_k) - \frac{k}{2}\phi x_k \sin(\phi x_k) \\ &= \cos(\phi x_k) - (\frac{2}{\phi} - \frac{\phi}{2})x_k \sin(\phi x_k) \ . \end{aligned} \tag{48}$$

The phase shift per section of the transmission line type distributed

amplifier θ is plotted in Fig. 9 as a function of normalized frequency x_k with the angular length of section ϕ [also the loading ratio k by virtue of equation (46)] as parameters. When $\phi=2$, the second term vanishes, and represents the unloaded pure line limit which is a straight line (no distortion). When $\phi=0$, the formula reduces to equation (5) which represents the lumped filter case. For other values of ϕ the curves lie between these two limits. It may be noted from Fig. 9 that the phase shift distortion can be reduced to any desired amount by choosing a proper value of ϕ (or k).

The straight line, representing the pure line limit, intersects the $\theta=\pi$ line at $\pi/2$ times the lumped cutoff frequency. The cutoff frequency of the transmission line type distributed amplifier is therefore raised from f_c to a value between f_c and $\frac{\pi}{2}f_c$, given by the equation:

$$\cos(\phi x_k) - (\frac{2}{\phi} - \frac{\phi}{2})x_k \sin(\phi x_k) = -1 \qquad (49)$$

or

$$x_k(\frac{2}{\phi} - \frac{\phi}{2}) = \cot\frac{\phi x_k}{2} . \qquad (50)$$

The actual cutoff frequency is plotted in Fig. 10 as a function of ϕ (and k).

The impedance of the section can be found by terminating an unknown admittance Y at one end of the network shown in Fig. 8 and by demanding that the admittance looking from the other end into the network be Y. Therefore,

$$\frac{1}{\frac{1}{b+Y}+a} + b = Y \qquad (51)$$

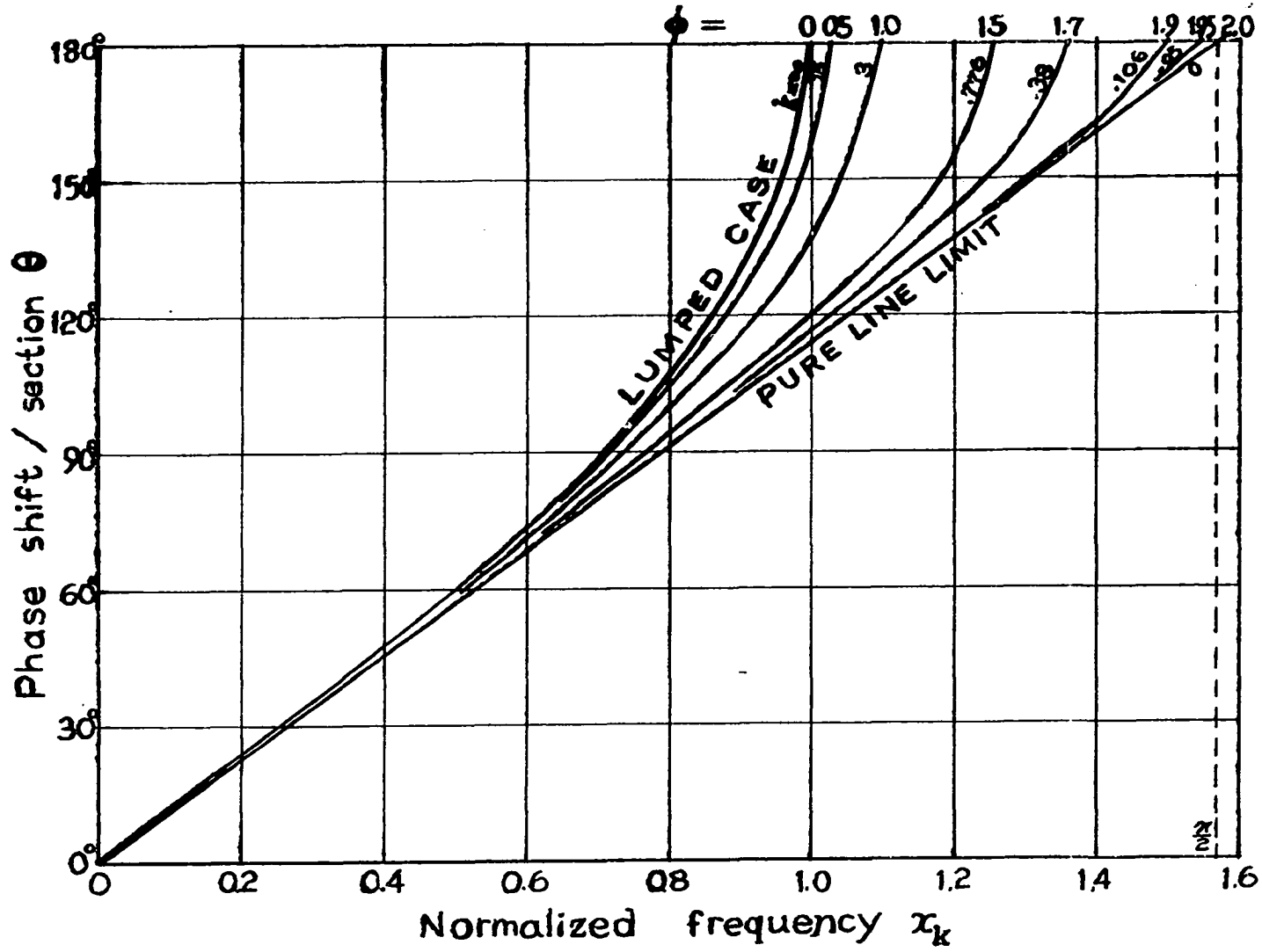


Fig. 9. Phase shift characteristics

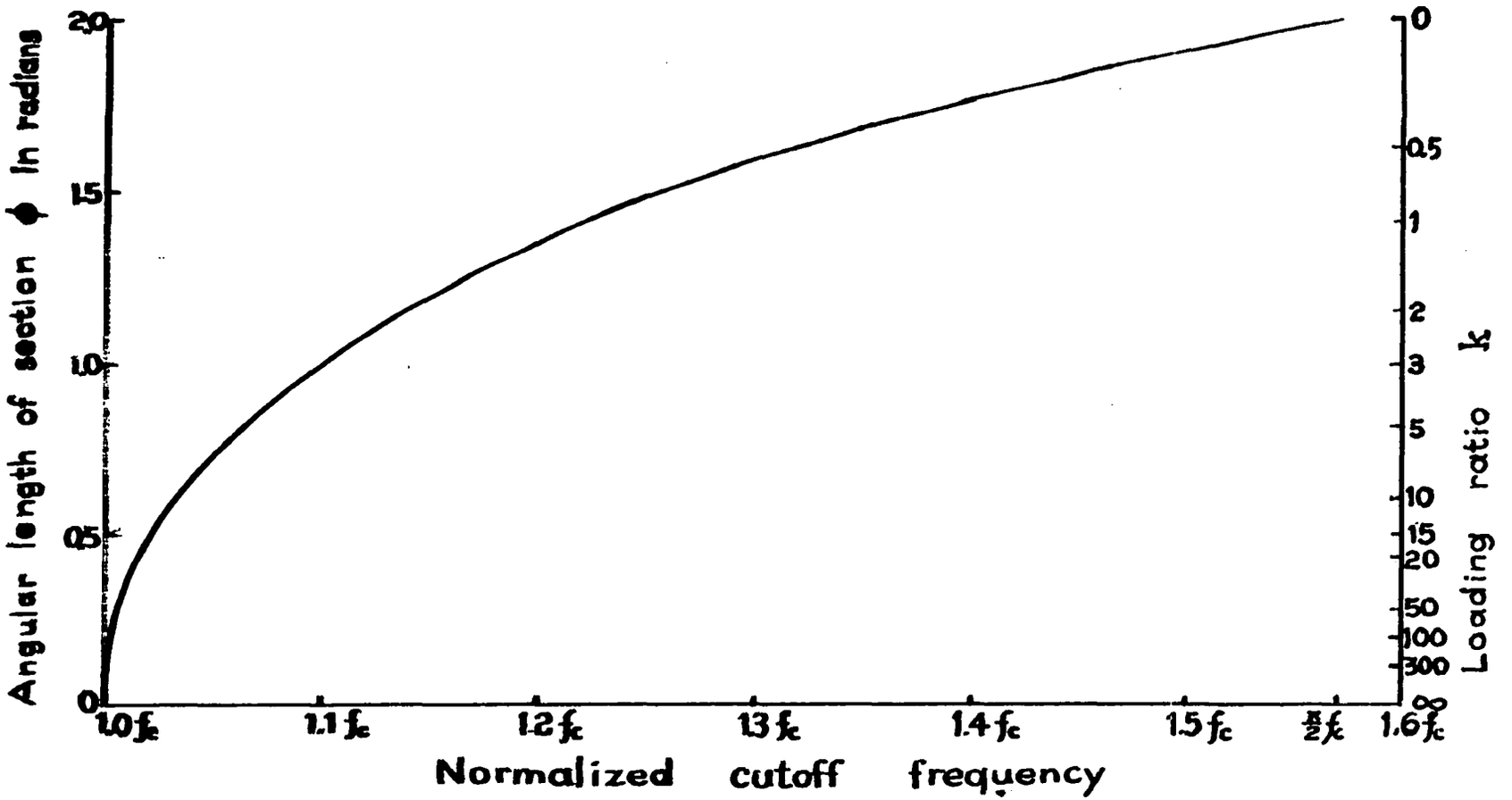


Fig. 10. Normalized cutoff frequency versus normalized line length and loading ratio

where a and b are given by equations (36) and (37). From equation (51),

$$b + Y = (Y - b)(1 + ab + aY)$$

or

$$Y = \sqrt{\frac{b(2 + ab)}{a}} \tag{52}$$

and

$$Z = \sqrt{\frac{a}{b(2 + ab)}} . \tag{53}$$

From equation (38),

$$ab = \cos\theta - 1 . \tag{54}$$

Then,

$$Z = \left[\frac{a}{b}\,\frac{1}{1 + \cos\theta}\right]^{\frac{1}{2}} \tag{55}$$

where

$$\frac{a}{b} = \frac{L}{C}\,\frac{\sin \omega l\sqrt{LC}}{\tan\frac{\omega l}{2}\sqrt{LC} + \frac{\omega C_L}{2}\sqrt{\frac{L}{C}}} \tag{56}$$

$$= \frac{L}{C}\,\frac{\sin(\phi x_k)}{\tan(\frac{\phi x_k}{2}) + x_k(\frac{2}{\phi} - \frac{\phi}{2})} \tag{57}$$

and $\cos\theta$ is given by equation (48). Alternately;

$$Z = \left[\frac{a}{b}\,\frac{1}{1 + \cos\theta}\right]^{\frac{1}{2}}$$

$$Z = \left[\frac{a^2}{\cos\theta - 1}\,\frac{1}{1+\cos\theta}\right]^{\frac{1}{2}}$$

$$= \frac{\sqrt{-a^2}}{\sin\theta}$$

$$= \sqrt{\frac{L}{C}}\,\frac{\sin \omega k\sqrt{LC}}{\sin\theta} \tag{58}$$

$$= \sqrt{\frac{L}{C}}\,\frac{\sin\ \phi x_k}{\sin\theta}\ . \tag{59}$$

In the pass band;

$$0 \leq \theta < \pi, \qquad 0 \leq \phi \leq 2, \qquad 0 \leq x_k \leq \frac{\pi}{2}, \tag{60}$$

the impedance is a positive real number. The low frequency impedance is not $\sqrt{L/C}$, but can be determined by equations (55) and (57) as x_k approaches zero as:

$$Z = \left[\frac{L}{C}\,\frac{\sin(\phi x_k)}{\tan(\frac{\phi x_k}{2}) + \phi x_k(\frac{2}{\phi^2} - \frac{1}{2})}\,\frac{1}{1+\cos\theta}\right]^{\frac{1}{2}}$$

$$= \left[\frac{L}{C}\,\frac{1}{\frac{1}{2} + (\frac{2}{\phi^2} - \frac{1}{2})}\cdot\frac{1}{2}\right]^{\frac{1}{2}}$$

$$= \sqrt{\frac{L}{C(1+k)}}\ . \tag{61}$$

This equation coincides with equation (28). The normalized impedance

characteristic is plotted in Fig. 11 with ϕ (and k) as parameters. Comparing with the lumped characteristics in Fig. 11, the transmission line type has a more linear amplitude response and a wider useful frequency range approaching the pure line limit whose impedance is a constant.

For a desired maximum percentage of tolerance of amplitude and phase shift distortions, a normalized length of section (and a normalized loading percentage) can be selected and the normalized percentage of frequency coverage can be found. Or when any one of them is defined, the other two can be found. This is plotted in Fig. 12 and Fig. 13 for design purposes.

STRIP LINE

By the nature of film deposition, line of rectangular cross section will be convenient. The main properties of such a line do not differ significantly from those of lines with circular cross section and the capacitance per unit length may be determined by electrostatic methods regardless of the nature of the cross section provided the cross-sectional dimensions and the separation between two conductors are all small compared with the wave length. This is to ensure the existence of exclusively axial currents, which, for loss-less conductors, exist in the TEM mode.[17]

For isolation of fields between input and output lines, the sandwiched strip line is preferable because the field of such a line is completely confined within its ground plates. A cross-sectional view is shown in Fig. 14.

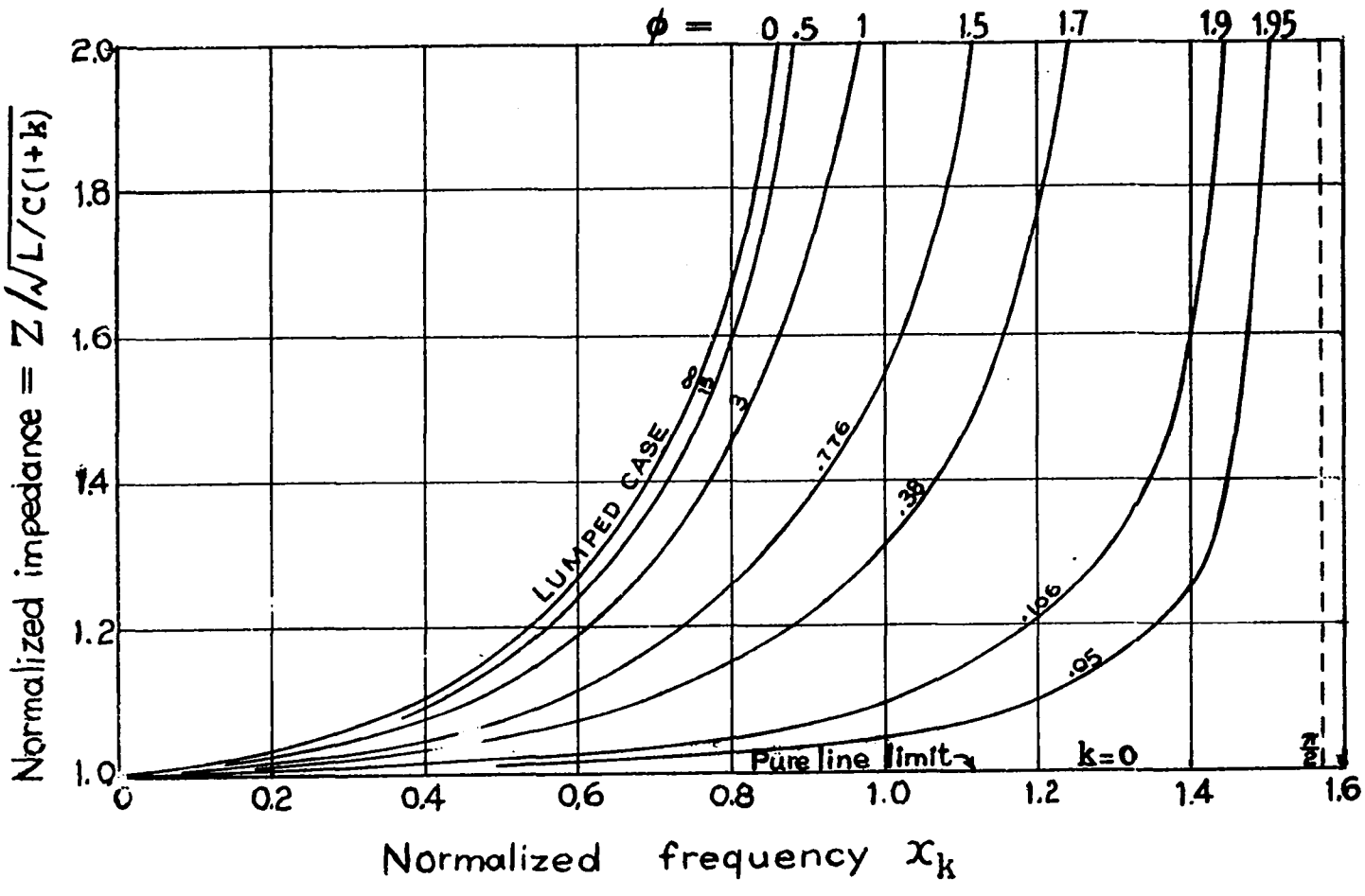


Fig. 11. Normalized impedance characteristics

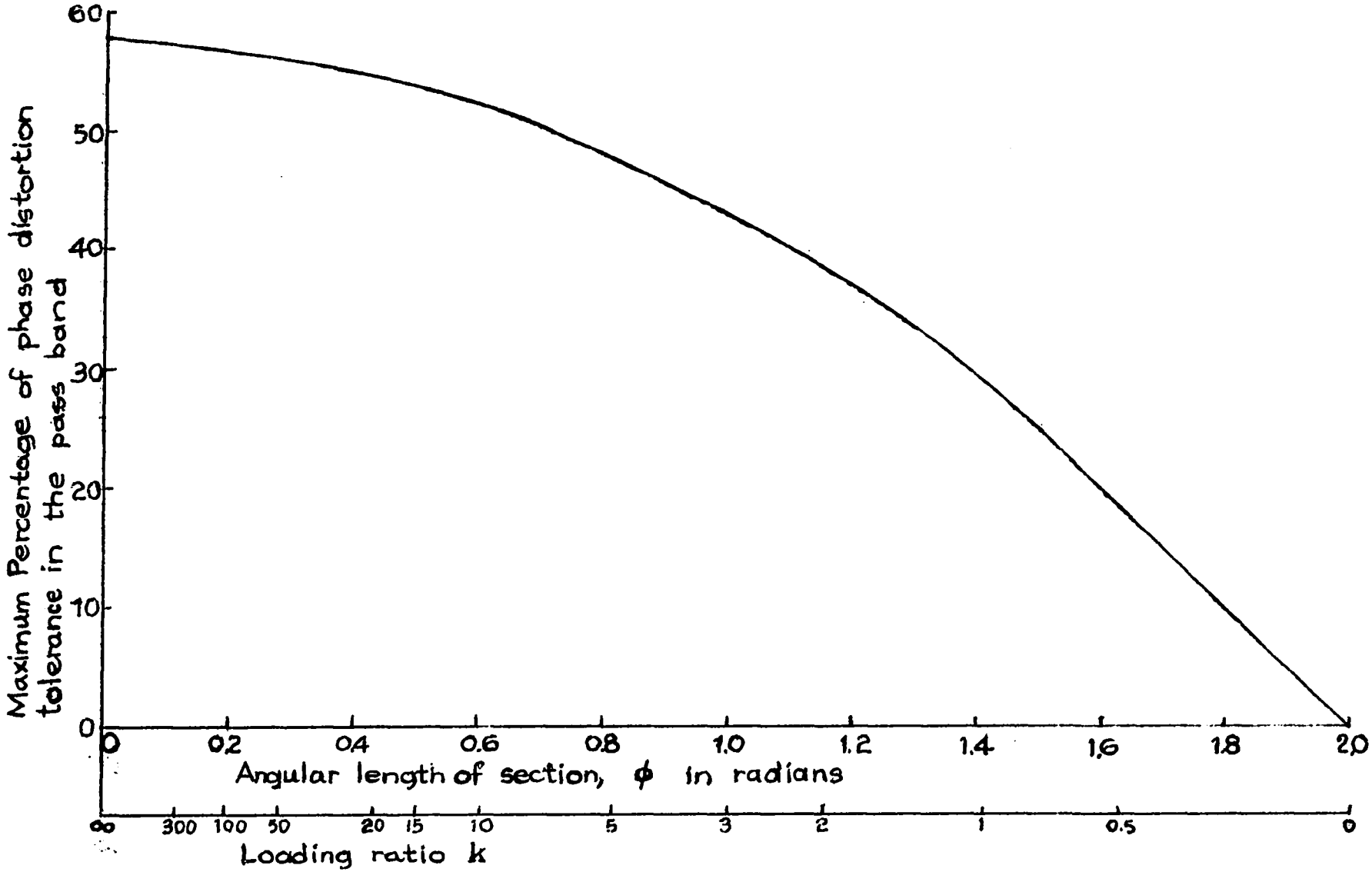


Fig. 12. Percent distortion tolerance versus normalized line length and loading ratio

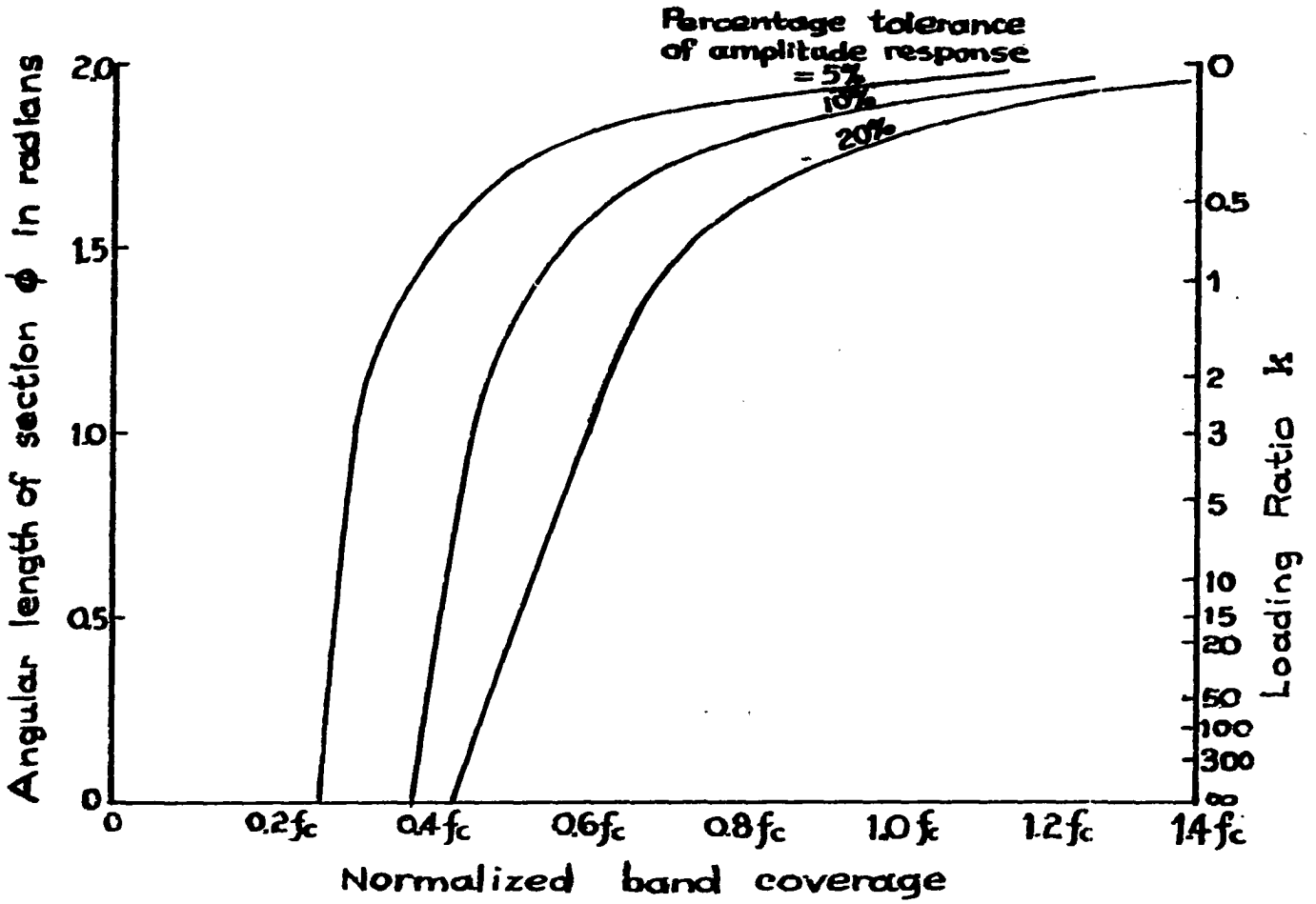


Fig. 13. Band coverage versus normalized line length and loading ratio

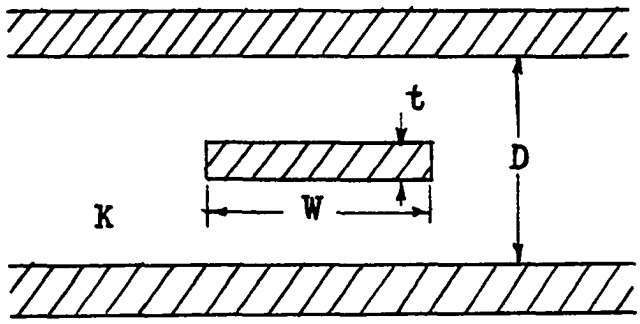


Fig. 14. The sandwiched strip line

The center strip is insulated by a medium having dielectric constant K from the top and bottom ground plates which serve as the return. If the ground plates extend far to both sides and if the center strip is very thin, the impedance of the strip line, found by conformal transformation, is given by[18]

$$Z_o = \frac{30\pi F(s)}{\sqrt{K}\, F(s')} \tag{64}$$

where

$$s'^2 = 1 - s^2 \tag{65}$$

$$s = \frac{1}{\cosh(\frac{\pi}{2}\frac{W}{D})} \tag{66}$$

and F(s) is the complete elliptic integral of the first kind of modulus s. The calculated impedance agrees very well with experimental results for $W/D \geq 0.1$.

When the thickness of the center strip is not small compared to the ground plate separation, the capacitances introduced by the side

faces and corners of the center strip should be taken into account. The correction terms for capacitances needed for this case can be calculated. The corresponding impedance variations are plotted by Cohn[20] as shown in Fig. 15 where impedance is plotted versus width-to-separation ratio W/D (down to 0.1) with thickness-to-separation ratio t/D as a parameter (0 to 0.25).

For strips of small cross section, the impedance can be approximated by[20]

$$Z_o = \frac{60}{\sqrt{K}} \ln\frac{4D}{\pi d_o} \tag{67}$$

when $W/(D-t) \leq 0.35$ and $t/D \leq 0.25$, d_o is the diameter of a circular cross-section conductor equivalent to the rectangular strip. (The relation between d_o and the strip dimensions has been determined by Marcuvitz.[21])

The inductance and capacitance per unit length can be calculated from the impedance by:

$$L = \frac{Z_o}{v} = \frac{Z_o\sqrt{K\mu_r}}{c} \tag{68}$$

and

$$C = \frac{1}{vZ_o} = \frac{\sqrt{K\mu_r}}{Z_o c} . \tag{69}$$

Other types of strip lines can be employed in distributed amplifiers, especially, the strip-to-ground line. Open wire type line with rectangular cross section can be conveniently made, but unwanted

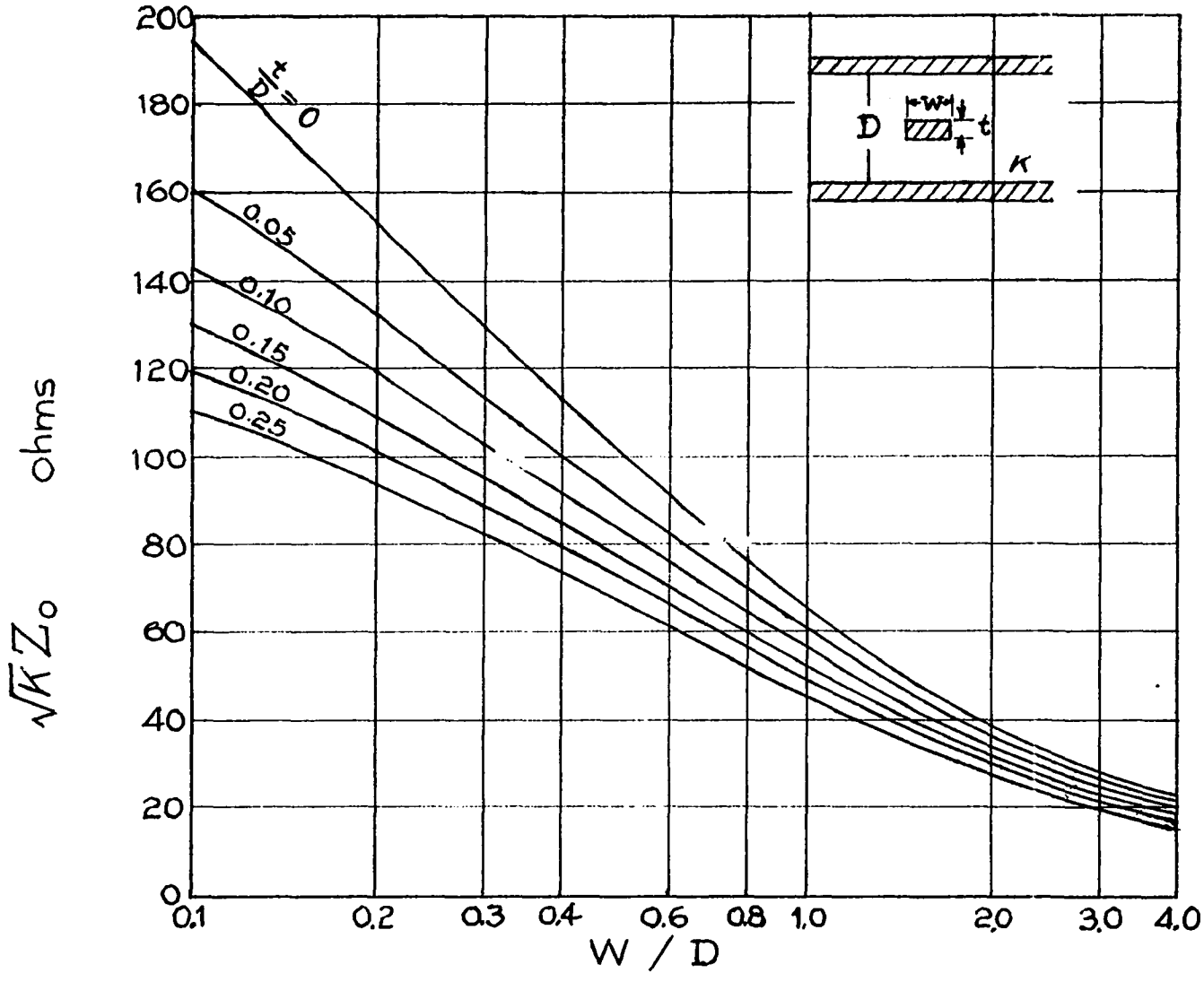


Fig. 15. Impedance of a strip line with non-zero thickness

coupling may exist.

The isolation property of the sandwiched strip line is excellent. Its transverse attenuation is given by[22]

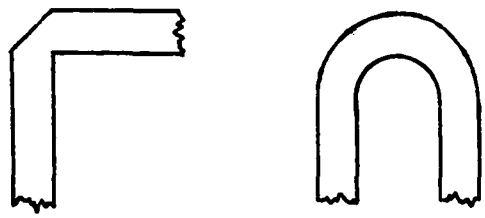
$$\alpha_t = \frac{27}{D} \tag{70}$$

where α_t is the attenuation of fields extending transversely from the strip conductor in dB per unit length and D is the ground plate spacing. At a distance equal to D, the attenuation is 27 dB. This means that two strip line circuits between common ground plates need only be separated by approximately the ground plate spacing to achieve negligible coupling.

For thin-film construction, several things are to be noticed. The first thing is the limited space available, thus the line will be bent. Two kinds of bends are shown in Fig. 16. The 45° cut bend gives a voltage standing-wave ratio of 1.04.[23] A still better bend is shown in Fig. 16(b). The effect of reflections coming from the impedance discontinuities at the bends (for the case M=4W) is negligible.[24]

As the line bends, the ground plates remain as common flat planes covering the whole section of line in order to eliminate the so-called guided mode which is a consequence of total internal reflection at the air-dielectric interface if the medium is not wholly covered. The plates will extend sufficiently over the strip to prevent such modes from propagating transversely to neighboring circuits.

The thickness of the dielectric medium and the strip are to be monitored since this is directly related to the line constants. But the



(a) (b)

Fig. 16. Bends of strip lines

tolerance is quite loose as can be seen from Fig. 15. A change in characteristic impedance of approximately 2% amounts to a change in the W/D ratio of 3%.[25] The fractional change of the impedance due to fractional change of spacing can be expressed, from equation (67), as

$$S_{Z_o} = \frac{\partial Z_o / \partial D}{Z_o / D} = \frac{1}{\ln \frac{4D}{\pi d_o}} . \tag{71}$$

Changes of inductance and capacitance are, from equations (68) and (69),

$$S_L = S_{Z_o} , \tag{72}$$

$$S_C = -S_{Z_o} . \tag{73}$$

These two changes tend to cancel each other in the cutoff-frequency equation (27). Since

$$f_c \propto (1 + \frac{C'}{C})^{-\frac{1}{2}} , \tag{74}$$

it is readily verified that the fractional change of cutoff-frequency due to fractional change of line spacing is equal to:

$$S_{f_c} = -\frac{1}{2}\,\frac{k}{1+k}\,\frac{1}{\ln\frac{4D}{\pi d_o}} \tag{75}$$

which is less than one-half the change of impedance.

Tilt of the center strip is critical for post supported strip lines.[22] For the thin-film case, the dielectric substance can be deposited evenly enough over small portions of the substrate.

Since the line constants are functions of the line shape only, the size of line cross-section can be reduced without limit. Only the resistance of the thin-film line is a problem. The well-known skin depth equation is:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{76}$$

where δ is the skin depth and σ is the conductivity. For copper at 100MC, the skin depth is 6.6 microns. If a solid wire has a radius-to-skin depth ratio not greater than about 1.5, its high frequency resistance does not differ from the dc resistance by an appreciable amount,[26] hence the ordinary resistance formula applies. For larger diameter, the central part of the wire becomes less useful. Thus the most space-saving configuration of the strip line is one which has a strip thickness around 3δ and a strip width wide enough to satisfy a desired attenuation limit. Of course, the desired line constants L

and C must also be considered.

The dielectric loss is negligible at the frequency of interest. Thus, equation (20) can be written as

$$\alpha = \frac{R}{\omega_c L} = \frac{1}{Q_L \text{ at } f_c} \qquad (77)$$

for low frequencies. From a transmission line viewpoint, the attenuation per section will be

$$\alpha = \frac{R\ell}{2Z_\pi} = \frac{R\ell}{2}\sqrt{\frac{C(1+k)}{L}}, \qquad (78)$$

where Z_π, instead of Z_o, should be used since the line is loaded. Equations (77) and (78) are identical.

MOS TRANSISTOR

In addition to the cutoff frequency of the loaded line sections, the introduction of MOS transistors with their inherent cutoff characteristics will introduce other cutoff frequency effects. A metal oxide semiconductor transistor is shown in Fig. 17.

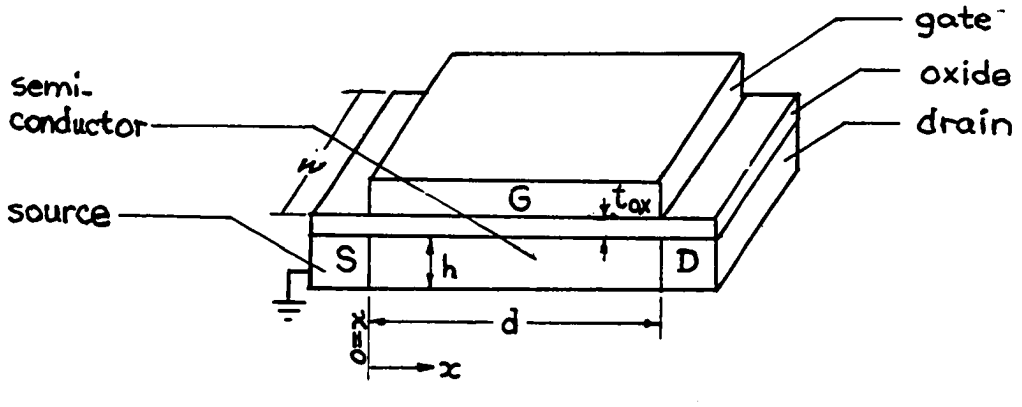


Fig. 17. MOS transistor structure

A voltage V_d is applied between the drain and the source. Another voltage V_g (with source as reference) is applied to the gate which, separated only by a thin insulation layer, exerts a field effect on the semiconductor. Charges are induced inside the semiconductor, especially near the surface directly under the gate. This alters the drain current I_d, thereby achieving a transconductance. Parameters of interest in the use of MOS transistors in a distributed amplifier are the current-voltage relations, input and output capacitances, transconductance and the associated cutoff frequency.

Let V(x) be the channel voltage within the semiconductor at a distance x from the source. Assume this voltage is uniform along h and w. The gate capacitance C_g is assumed to be independent of the channel voltage. LetΔN(x) be the number of charge carriers induced in the semiconductor per unit area of the gate electrode. The charge induced should be equal to the charge on the gate everywhere, therefore,

$$q\Delta N(x) = \frac{C_g}{wd}\left[V_g - V(x)\right] . \qquad (79)$$

There are initial charges in the semiconductor before the gate voltage is applied, which have been considered by Borkan and Weimer.[27] Let N_o be the total initial charge in the semiconductor. The drain current I_d under the field set up by the applied drain voltage is then

$$I_d = hw\mu q \left[\frac{N_o}{hwd} + \frac{\Delta N(x)}{h}\right]E_x \qquad (80)$$

where

μ = mobility of the carrier in semiconductor

q = electron charge

E_x = electric field strength in the x-direction

$$E_x = \frac{d}{dx} V(x) \quad . \tag{81}$$

Substitute equations (79) and (81) into equation (80) and perform the integration,

$$\int_0^d I_d dx = \frac{\mu C_g}{d} \int_0^V \left[\frac{N_o q}{C_g} + V_g - V(x) \right] dV(x) \quad . \tag{82}$$

Since I_d is independent of x (consider majority carriers only), the result is

$$I_d = \frac{\mu C_g}{d^2} \left[(V_g - V_o) V_d - \frac{V_d^2}{2} \right] \tag{83}$$

where

$$V_o = - \frac{N_o q}{C_g} \tag{84}$$

$$= - \frac{Q_{ss} + Q_B}{C_g} \tag{85}$$

Q_{ss} = total initial surface state charge

Q_B = total initial bulk charge.

V_o is the gate voltage required for the onset of drain current and N_o is negative for enhancement. Q_{ss} usually dominates and represents the

acceptor states or traps which must be filled before the drain current can be increased by the field-effect. N_o is positive for the depletion type, and the gate voltage is negative if the drain current is to be depleted. V_o is related to the shape of energy bands near the semiconductor-insulator interface, the volume density of charge, surface treatment, material used and other factors. Its value is difficult to precalculate, but it may be obtained by measurement, and a proper gate bias chosen.

Equation (83) is valid in the unsaturated region. The peak drain current occurs when

$$V_d = V_g - V_o \, . \tag{86}$$

This may be noted from equation (83), with V_g as a parameter. The drain current will remain saturated at this peak value when drain voltage is further increased. This is due mainly to the pinch-off effect near the region of the drain, analogous to the p-n junction field-effect transistor effect. The saturation current is then given by

$$I_{d\ max} = \frac{\mu C_g}{2d^2}(V_g - V_o)^2 \, . \tag{87}$$

The transconductance in the saturation region is

$$g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_d=\text{constant}}$$

$$= \frac{\mu C_g (V_g - V_o)}{d^2} \, . \tag{88}$$

$$g_m = \sqrt{\frac{2\mu C_g I_{d\,max}}{d}} \quad . \tag{89}$$

In the unsaturated region, the transconductance is

$$g_m = \frac{\mu C_g}{d^2} V_d \ , \tag{90}$$

and the drain conductance is

$$g_d = \left.\frac{\partial I_d}{\partial V_d}\right|_{V_g=\text{constant}} = \frac{\mu C_g}{d^2}(V_g - V_o - V_d) \ . \tag{91}$$

g_d is very small at saturation, giving rise to a pentode-like characteristic.

To find interelectrode capacitances, the charge on the gate electrode Q_G is first calculated.[28]

$$Q_G = \int_{A_G} D_{ox} dA_g = \int_0^d \epsilon_{ox} E_{ox} w dx$$

$$= \frac{\epsilon_{ox} w}{t_{ox}} \int_0^d \left[V_g - V(x)\right] dx$$

$$= \frac{C_o}{d} \int_0^d \left[V_g - V(x)\right] dx \tag{92}$$

where

D_{ox} = electric flux density

A_G = area of the gate

ϵ_{ox} = permittivity of the oxide

E_{ox} = electric field strength in the oxide

t_{ox} = thickness of the oxide layer

and

$$C_o = \frac{\epsilon_{ox} wd}{t_{ox}} . \tag{93}$$

This is the geometrical capacitance across the oxide layer. From equations (80) and (81),

$$dx = \frac{\mu C_g}{dI_d} \left[-V_o + V_g - V(x) \right] dV(x). \tag{94}$$

Substituting equations (94) and (83) into (92) and performing the integration, yields

$$Q_G = C_o \left\{ V_g - \frac{3(V_g - V_o)V_d - 2V_d^2}{3\left[2(V_g - V_o) - V_d\right]} \right\}. \tag{95}$$

The short circuit gate capacitance C_G is then

$$C_G = \left. \frac{\partial Q_G}{\partial V_g} \right|_{V_d = \text{constant}}$$

$$C_G = C_o \left\{ 1 - \frac{V_d^2}{3\left[2(V_g - V_o) - V_d\right]} \right\} . \qquad (96)$$

Similarly, charge stored in the semiconductor channel is

$$Q_{ch} = -Q_G + C_o V_o \qquad (97)$$

where $C_o V_o$ is the initial charge in the semiconductor. The short circuit drain capacitance is

$$C_D = \left. \frac{\partial Q_{ch}}{\partial V_d} \right|_{V_g = \text{constant}}$$

$$= \frac{2C_o}{3} \frac{\left[3(V_g - V_o) - V_d\right]\left[V_g - V_o - V_d\right]}{\left[2(V_g - V_o) - V_d\right]^2} \qquad (98)$$

The open circuit gate capacitance can be found from equations (92) and (83),

$$C_{Go} = \left. \frac{\partial Q_G}{\partial V_g} \right|_{I_d = \text{constant}}$$

$$= \frac{2(V_g - V_o)C_o}{2(V_g - V_o) - V_d} . \qquad (99)$$

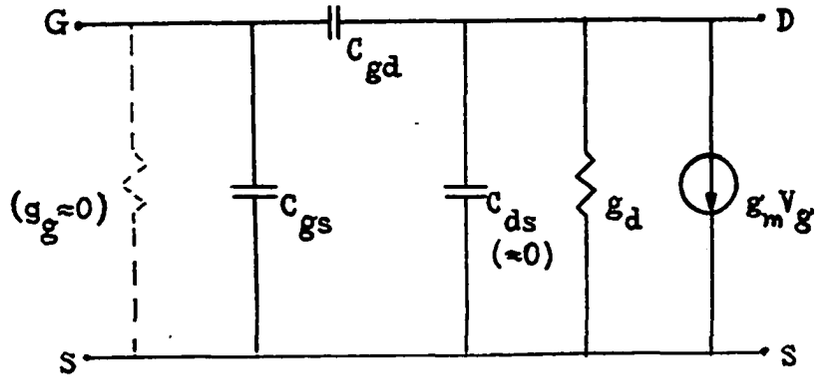


Fig. 18. Equivalent circuit showing capacitancies

The equivalent circuit is shown in Fig. 18. From this circuit and the short- and open-circuit capacitance equations, the interelectrode capacitances can be evaluated,

$$\frac{C_{gs}}{C_o} = \frac{2}{3} \frac{(V_g-V_o)\left[3(V_g-V_o)-2V_d\right]}{\left[2(V_g-V_o)-V_d\right]^2} \tag{100}$$

$$\frac{C_{gd}}{C_o} = \frac{2\left[3(V_g-V_o)-V_d\right]\left[V_g-V_o-V_d\right]}{3\left[2(V_g-V_o)-V_d\right]^2} \tag{101}$$

$$C_{ds} = 0 \, . \tag{102}$$

At saturation, equations (100) and (101) reduce to

$$C_{gs(s)} = \frac{2}{3}C_o \tag{103}$$

$$C_{gd(s)} = 0 \, . \tag{104}$$

In the saturation region, both the drain-to-gate capacitance and the drain-to-source capacitance are negligible.[27,28,29] This is due to the isolation effect of the region.

The transistor will be operated in the saturation region since the slope of the load line is high compared to the low operating current of the transistor. The gate line will be loaded by the saturated gate capacitance which is two-thirds of the geometrical capacitance.[28,30] External capacitors will be conveniently deposited for the loading of the drain line.

As to the fractional change of the cutoff frequency due to the fractional change of the transistor capacitance, the expression is readily obtained from equation (74),

$$S_{f_c} = - \frac{\frac{C'}{C}}{2(1 + \frac{C'}{C})} . \qquad (105)$$

The magnitude of this ratio is only one-fourth for the case $C'/C = 1$.

In the high frequency response of the MOS transistor, the drift mobility and the drain-source spacing play an important role. The mobility is a function of applied fields, both axial and transverse, existing in the MOS transistor. The drain-source voltage produces an axial field E_x. The mobility $\mu(E_x)$ as a function of E_x is given by the equation

$$v_d = \mu(E_x) \cdot E_x \qquad (106)$$

where v_d is the drift velocity of carriers. There exists a constant

maximum velocity $v_{d\ max}$ beyond which the carriers can not be accelerated.[31,32] When this exists,

$$\mu(E_x) = \frac{v_{d\ max}}{E_x} . \qquad (107)$$

This velocity, which corresponds to the thermal velocity of carriers, enters when one tries to deal with an extremely narrow channel length. For moderate channel length, this correction, being a complex function of drain current, geometry, etc., is usually omitted.[33] The Schrieffer correction takes account of the transverse field E_s, exerted by the gate to channel voltage difference across the oxide,[33,34]

$$E_s = \frac{[V_g - V(x)]\epsilon_{ox}}{\epsilon t_{ox}} . \qquad (108)$$

The mobility of CdS measured by Hall effect is listed as 200 cm^2/volt-sec.[35] It is to be noticed that correlation between drift and Hall mobility is rather poor. In most cases, the drift mobility was found to be less than the Hall mobility, but occasionally the reverse was true. Both the drift and Hall mobilities increase initially with gate voltage and then fall off with further increase of gate voltage as predicted by Schrieffer. A complete theory of this type is not presently available, although a computer calculated approximation for the silicon MOS transistors has been proposed.[34] From the standpoint of device design, the assumption of constant mobility used in equation (80) to (91) is sufficient for most purposes. The field-effect mobilities calculated from equation (112) below for the thin-film CdS transistors

were 150 cm^2/ volt-sec. and lower.[36] The value of 150 cm^2/ volt-sec. will be used in this design.

The transconductance of the transistor can be written as a function of frequency,

$$g_m = \frac{g_{mo}}{1 + j \frac{\omega}{\omega_{g_m}}} \tag{109}$$

where the value of g_{mo} is given by equation (88) or (90) and the angular cutoff frequency of the transconductance ω_{g_m} is[28]

$$\omega_{g_m} = \frac{g_{mo}}{C_G} . \tag{110}$$

Since at saturation,

$$C_G(s) = C_{gs(s)} + C_{gd(s)} = \frac{2}{3} C_o , \tag{111}$$

the g_m cutoff frequency at saturation becomes

$$\omega_{g_m} = \frac{3}{2} \frac{\mu}{d^2}(V_g - V_o) \tag{112}$$

$$= 3\sqrt{\frac{\mu I_{d\ max}}{2C_o d^2}} . \tag{113}$$

where C_g, the capacitance between the gate and current channel, is approximated by the geometrical capacitance C_o, a limiting value which will be approached when gate voltage increases. This is equivalent to the assumption that a conductive channel is built only into the upper

surface of the semiconductor adjacent to the insulator.

The term $\frac{\mu}{d^2}(V_g-V_o)$ or $\frac{\mu}{d^2}V_d$ is the reciprocal of the transit time needed for a carrier to travel through the gap. A shorter gap width d will reduce the transit time and the gate capacitance, and will increase the transconductance and its cutoff frequency. The smallness of the gap width is limited by the uniformity of the gap attainable and a more basic factor, heat dissipation. For a certain minimum voltage output amplitude, current will increase with the decrease of d and may exceed the temperature limit. When E_x is increased by the decrease of d, $v_{d\ max}$ may be reached and the mobility will decrease for further increase of E_x.

A low value of oxide thickness t_{ox} is desirable for a high transconductance. The lowest value is limited by the flawless flat layer obtainable in the process of deposition and by the Schrieffer effect which reduces mobility. The impedance, dimensions and loading characteristics of the line, amplifier gain and operating voltages are all related to the transistor constants. Optimization of the amplifier will be quite difficult due to the large number of non-linear parameters indicated.

Although the frequency response of the MOS transistor is theoretically limited by the dielectric relaxation time as in all solid-state transistors,[37] it is also limited in a practical sense by the dimensions, current and the temperature. For conventional amplifiers with MOS transistors, it is further limited by circuit considerations to an angular frequency which is usually considerably below ω_{gm}.[28]

CHAPTER III

DESIGN

It is proper to start the design with the MOS transistor, followed by the transmission line, and then the design of the complete amplifier, although all these subsystems are mutually correlated.

A glass substrate is chosen for ease of isolation and cadmium sulphide is used for the semiconductor. Although a silicon wafer gives higher mobility, its stray capacitances due to deposited components are not desirable.

Coplanar type MOS transistors are adopted, rather than the staggered type, for less masking work and easier heat treatment. The substrate is heated during the deposition of the CdS layer before other layers are deposited. The reheating treatment can follow right after deposition. Thus, overheating of other layers is avoided.

By control of the substrate temperature in this procedure, the resistivity of the CdS layer can be varied greatly. If the semiconductor has a high resistivity, the unmodulated current component due to the bulk of the film is negligibly small. For low resistivity semiconductors, the gate must be able to deplete the entire thickness of film to obtain saturated characteristics. For high resistivity semiconductor having its conductivity confined to the accumulation layer at the

surface, only the surface layer needs to be depleted.

It is assumed that the MOS transistors used here will operate in the saturation region. The thickness of CdS layer is chosen to be about 0.1 micron to reduce the unmodulated parallel conductance path between source and drain.

The thickness of source and drain electrode is chosen to be 300 Angstroms which is very small compared with the channel width but is comparable to the oxide layer thickness in order to avoid layer discontinuity. As the thickness of the source and drain electrodes is very thin, their width is made equal to the length of the channel, which is 150 mils, so as to keep the resistances of electrodes low compared to the impedance of the transmission line. The line connects directly to the electrodes to reduce resistive losses.

The transistor will be of the enhancement type. The operating level of the depletion type transistor depends largely on the gate voltage for the onset of drain current, V_o. As discussed in Chapter II, this is difficult to compute. For the enhancement type, it is proper to have V_o very small. Then V_o does not appear in the design equations.

Experimentally, the SiO-CdS layer combination may give a negative V_o due to absorbed oxygen on the surface of CdS layer acting as acceptors. The oxygen can be removed by a glow discharge over the CdS surface. The result is that V_o is reduced.[38] Aluminum is to be used as electrodes since it will give lower V_o.

If the semiconductor thickness is small and the insulator capacitance is high, the saturated drain current at zero gate bias is small even with semiconductors having a high carrier density. Thus,

operation is in the enhancement mode. For all values of V_d much greater than $V_o/2$, the zero gate bias current can even be considerably smaller than the drain current which would be observed in the same transistor if the gate electrode had been omitted.[39]

The channel width is directly related to the frequency response. The chosen value is six microns which is narrower than those generally used but can still be fabricated conveniently with the photoetch method.

For high transconductance, the length of the channel is made 150 mils long. The saturated drain current at the operating point is eight milliamperes which is considered to be a safe rating in heat dissipation for the channel length and width used.

The gate should be wide enough and the insulator thin enough to render sufficient electrostatic shielding of the gap region to obtain saturation characteristics. If the shielding is insufficient, a channel may not be formed and the device could operate as a space-charge-limited triode.[40] Under such conditions, the gate capacitance is lower, and the highest transconductance is not achieved. The width of the gate is seven microns. The gate can be thicker than the source and drain electrodes. A thickness of 0.1 micron is chosen.

The g_m cutoff frequency, given by equation (113), is $2\pi x10^8$ cps.

$$\omega_{g_m(s)} = 3\sqrt{\frac{\mu I_{d\ max}}{2C_o d^2}} \quad . \qquad (113)$$

From this, C_o is evaluated,

$$C_o = \frac{9\mu I_{d\ max}}{2\omega_{g_m}{}^2 d^2} \qquad (114)$$

$$= \frac{9 \times 150 \times 8 \times 10^{-3}}{2 \times 4\pi^2 \times 10^{16} \times 6^2 \times 10^{-8}}$$

$$= 38 \text{ pF.}$$

The transconductance of the transistors is computed from equation (89) which is

$$g_m = \frac{\sqrt{2\mu I_{d\ max} C_g}}{d}$$

$$= \frac{\sqrt{2 \times 150 \times 38 \times 10^{-12} \times 8 \times 10^{-3}}}{6 \times 10^{-4}}$$

$$= 0.016 \text{ mhos.}$$

This high value of transconductance is needed for the amplifier with the strip line impedance as a load.

The relation governing the saturation voltage is

$$g_m = \frac{\mu C_g}{d^2} V_d \ , \qquad (90)$$

from which,

$$V_d \text{ (at the knee)} = \frac{d^2 g_m}{\mu C_g} \qquad (115)$$

$$V_d = \frac{36 \times 10^{-8} \times 0.016}{150 \times 38 \times 10^{-12}}$$

$$= 1 \text{ volt.}$$

Thus, the designed operating point is at the place where drain current is eight milliamperes and the knee of drain current saturation starts at $V_d = 1$ volt. V_0 is made negligible for the enhancement mode, therefore, the operating gate bias is also one volt [see equation (86)].

Thickness of the oxide layer is evaluated from equation (93) to be

$$t_{ox} = \frac{\epsilon_{ox} wd}{C_o} \tag{116}$$

$$= \frac{2.25\text{x}10^{-9}\text{x}150\text{x}2.54\text{x}10^{-5}\text{x}6\text{x}10^{-6}}{36\pi \times 38 \times 10^{-12}}$$

$$= 1.2 \times 10^{-8} \text{ meter}$$

$$= 120 \text{ Angstroms.}$$

This rather thin layer permits high transconductance, and also insures saturation.

The drain current will be, according to equation (83),

$$I_d = \frac{150\text{x}38\text{x}10^{-12}}{36\text{x}10^{-8}}\left[V_g V_d - \frac{V_d^2}{2}\right]$$

$$= 16 \times 10^{-3}\left[V_g V_d - \frac{V_d^2}{2}\right]. \tag{117}$$

At saturation,

$$I_d = 8 \times 10^{-3} V_g^2 \ . \tag{118}$$

The interelectrode capacitances are

$$C_{gs} = \frac{2C_o}{3} \frac{3 - 2V_d}{(2 - V_d)^2} \tag{119}$$

$$C_{gd} = \frac{2C_o}{3} \frac{(3 - V)(1 - V_d)}{(2 - V_d)^2} \tag{120}$$

$$C_{ds} = 0, \qquad \text{at } V_g = 1 \text{ volt.} \tag{121}$$

At saturation,

$$C_{gs(s)} = \frac{2}{3} C_o \tag{122}$$

$$= 25.3 \text{ pF.}$$

$$C_{gd(s)} = 0, \qquad V_d \leq V_g = 1. \tag{123}$$

The capacitance $C_{gs(s)}$ will load the transmission line.

The characteristic impedance of the transmission line is chosen as 90 ohms. Using silicon monoxide which has a dielectric constant of 2.25 as the dielectric material, the impedance normalized to the dielectric medium is

$$Z_{nor.} = Z_o \sqrt{K} = 90\sqrt{2.25} \tag{124}$$

$$= 135 \text{ ohms.}$$

From the standpoint of amplifier gain, the highest impedance is desired. It has been found experimentally that the impedance of a strip line is practically limited to a value where $Z_o\sqrt{K}$ is about 200 ohms.[18] This corresponds to a D/W ratio of 10 or more. From the standpoint of line thickness, lower impedance will result in thinner structure although it requires a larger cross-sectional area of the center strip to compensate the loss. Low impedance also yields better phase shift and amplitude characteristics by increasing the line distributed capacitance, but the line length (hence space and line resistance) will be increased somewhat. The 90-ohm impedance is a compromise.

The attenuation per section of the loaded line is

$$\alpha = \frac{R\ell}{2Z_\pi} \tag{78}$$

$$= \frac{R\ell\sqrt{1 + k}}{2Z_o} . \tag{125}$$

The substitution of equation (45) into equation (125) yields

$$\alpha = \frac{R\ell}{\phi Z_o} \tag{126}$$

or

$$R = \left(\frac{\phi}{\ell}\right)\alpha Z_o , \tag{127}$$

where

$$\frac{\phi}{\ell} = \omega_c\sqrt{LC}$$

$$\frac{\phi}{\ell} = \frac{\omega_c}{v} \tag{128}$$

is a constant. Thus, the line resistance per meter R is directly proportional to the line characteristic impedance Z_o for a specified attenuation.

The attenuation is specified to be five percent, i.e., a one-volt input (E_1) will give a 0.95 volt output (E_2) after traveling a line section. This seems to be reasonably small. Since

$$v = \frac{c}{\sqrt{K\mu_r}} \tag{31}$$

$$= \frac{3 \times 10^8}{\sqrt{2.25}}$$

$$= 2 \times 10^8 \text{ meters/second,}$$

The ratio ϕ/ℓ is

$$\frac{\phi}{\ell} = \frac{2\pi \times 10^8}{2 \times 10^8} = \pi \text{ radians/meter.}$$

The attenuation in nepers per section is

$$\alpha = \ln \frac{E_1}{E_2} \tag{129}$$

$$= 0.0506 \text{ nepers/section.}$$

The resistance constant of the line is then

$$R = \pi \times 0.0506 \times 90$$

$$= 14.3 \text{ ohms/meter.}$$

Choose a center strip thickness of three times the skin depth at cutoff frequency which is 20 microns for copper. The strip width necessary for this thickness is given by

$$R = \frac{\rho}{tW} \tag{130}$$

where ρ is the resistivity of the copper strip which is 17240 ohm-meter/micron^2. The resistance of the two ground return plates in parallel connection has been omitted. From equation (130):

$$W = \frac{\rho}{Rt} \tag{131}$$

$$= \frac{17240}{14.3 \times 20}$$

$$= 60 \text{ microns},$$

and the ratio t/D is equal to (1/3)W/D. The ground plate separation is then found from Fig. 15. After a few cut-and-try calculations along the constant impedance line, the result is

$$\frac{W}{D} = 0.17$$

and

$$D = 353 \text{ microns}$$

$$= 13.9 \text{ mils}.$$

If thickness t is increased to 25 microns, width W will be 48 microns,

the same method will yield

$$\frac{W}{D} = 0.15$$

and

$$D = 320 \text{ microns}$$
$$= 12.6 \text{ mils}$$

This configuration is adopted. The thickness of dielectric medium on either side of the center strip is

$$\frac{D - t}{2} = 5.8 \text{ mils.}$$

The thickness of the ground plates is chosen to be one mil, the same thickness as t, in order that their resistance may be negligible.

For simplicity of deposition procedures, the drain line is identical to the gate line. The drain line loading capacitance is conveniently made by overlapping a partial area of the drain layer having the same thickness as that used in the MOS transistors. It will be deposited at the same time that the transistor insulators are deposited. The overlapping area A_{C_d} is two-thirds that of the channel as can be seen from equation (122). This is

$$A_{C_d} = \frac{2}{3} A_G \qquad (132)$$

$$= \frac{2}{3} \times 150 \times 25.4 \times 6$$

$$= 15200 \qquad \text{square microns.}$$

The capacitance per meter of the line is given by equation (69),

$$C = \frac{1.5}{90 \times 3 \times 10^8}$$

$$= 55.6 \quad pF/m.$$

The inductance per meter is given by equation (68),

$$L = \frac{90 \times 1.5}{3 \times 10^8}$$

$$= 0.45 \quad \mu H/m.$$

Equation (34) gives the length of the line per section,

$$\frac{K\mu_r}{c^2} \ell^2 + C_L L \ell - \frac{1}{\pi^2 f_c^2} = 0 \qquad (34)$$

$$\frac{2.25}{9\times10^{16}} \ell^2 + 25.3\times10^{-12}\times0.45\times10^{-6}\ell - \frac{1}{\pi^2\times10^{16}} = 0$$

or

$$2.5\,\ell^2 + 1.14\,\ell - 1.013 = 0$$

where the positive root is

$$\ell = 0.448 \text{ meters.}$$

The loading percentage is

$$k = \frac{C_L}{C\ell}$$

$$k = \frac{25.3 \times 10^{-12}}{55.6 \times 10^{-12} \times 0.448}$$

$$= 0.985.$$

The angular length of the section at the nominal cutoff frequency is

$$\phi = \frac{2}{\sqrt{1 + k}}$$

$$= 1.42.$$

This value of ϕ (and k) suggests good line characteristics. The amplifier has quite linear phase shift and flat gain response with respect to frequency. The phase shift function is

$$\cos\theta = \cos(1.42x_k) - (\frac{2}{1.42} - \frac{1.42}{2})x_k\sin(1.42x_k)$$

$$= \cos(1.42x_k) - 0.7x_k\sin(1.42x_k). \qquad (133)$$

This is plotted in Fig. 19. The actual cutoff frequency is governed by the equation

$$x_k(\frac{2}{\phi} - \frac{\phi}{2}) = \cot\frac{\phi x_k}{2} \qquad (50)$$

or

$$0.7\ x_k = \cot 0.71\ x_k.$$

x_k is found from this equation to be

$$x_k(\text{at cutoff}) = 1.22.$$

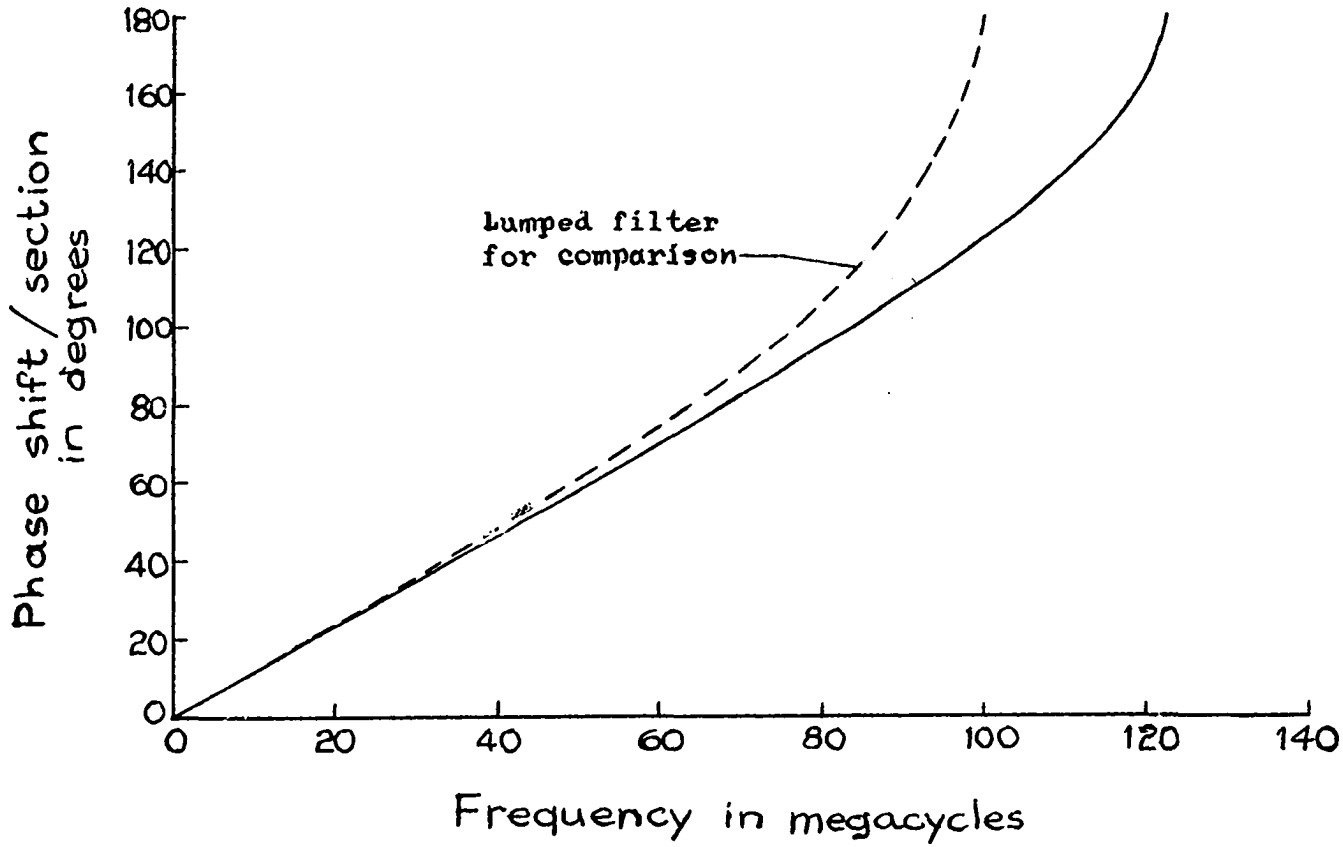


Fig. 19. Phase shift characteristic of the designed amplifier

The actual cutoff frequency is then 122 times the nominal cutoff frequency or 122 MC.

The impedance of the line section at low frequency is

$$Z_\pi = \sqrt{\frac{L}{C(1+k)}}$$

$$= \frac{\phi}{2} Z_o \qquad (134)$$

$$= \frac{1.42}{2} \times 90$$

$$= 64 \text{ ohms.}$$

The impedance function is

$$Z = Z_o \frac{\sin \phi x_k}{\sin \theta}$$

$$= 90 \times \frac{\sin(1.42x_k)}{\sin \theta} \text{ ohms} \qquad (135)$$

and the normalized impedance is given by

$$Z_{nor.} = \frac{Z}{Z_\pi}$$

$$= 1.41 \frac{\sin(1.42x_k)}{\sin \theta} \text{ ohms} \qquad (136)$$

where the value of θ can be calculated from equation (133). Fig. 20 shows the normalized impedance function.

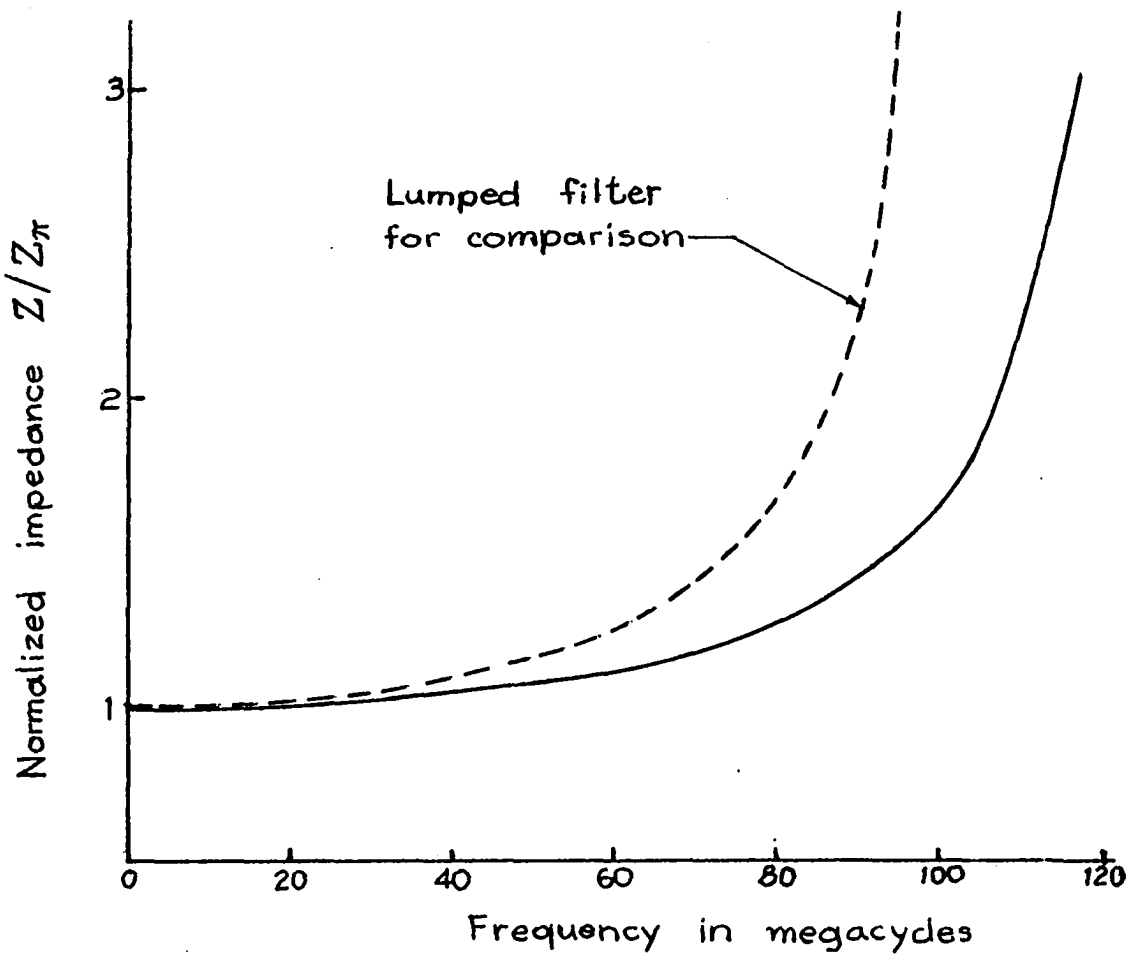


Fig. 20. Normalized impedance variation of the designed amplifier

It is constructive to compute the characteristic impedance of the strip line by equation (67), where the equivalent circular diameter of the strip is found to be 42.5 microns.[20,21] The resultant impedance checks fairly well.

The fractional change of sensitivity of the line impedance is

$$S_{Z_o} = \frac{\frac{\partial Z_o}{\partial D}}{\frac{Z_o}{D}} = \frac{1}{\ln \frac{4D}{\pi d_o}}$$

$$= \frac{1}{\ln \frac{4 \times 320}{\pi \times 42.5}}$$

$$= 0.44$$

which is small. An error of 10% in deposition thickness monitor will result in an impedance error of only 4.4%.

The sensitivity of cutoff frequency is

$$S_{f_c} = \frac{\frac{\partial f_c}{\partial D}}{\frac{f_c}{D}} = \frac{1}{2} \frac{k}{1 + k} \frac{1}{\ln \frac{4D}{\pi d_o}}$$

$$= \frac{1}{2} \frac{0.985}{1.985} \times 0.442$$

$$= 0.11$$

which suggests a frequency change of only 1.1% for the above change in thickness. The change of cutoff frequency due to the change of

transistor capacitance is

$$S_{f_c}(\text{due to } C_L) = \frac{\frac{\partial f_c}{\partial C'}}{\frac{f_c}{C'}} = \frac{1}{2}\,\frac{k}{1+k}$$

$$S_{f_c} \leq 0.25$$

which is tolerable even when the transistor capacitance varies from its value at saturation to its maximum theoretical value C_o. The unsaturated gate capacitance, which is found from the sum of equations (119) and (120), is plotted in Fig. 21. The actual variation will round off the corner like the dotted curve.

Each single stage will consist of five MOS transistors. The voltage gain of one stage, when the reverse termination is omitted, is

$$A \text{ (in dB)} = 20 \log_{10}(ng_m Z_\pi) \qquad (137)$$

$$= 20 \log_{10}(5\text{x}0.016\text{x}64)$$

$$= 14.2 \text{ dB}.$$

The number of transistors per stage is chosen by the space available on standard substrates. Since the input and output impedances will be approximately the same, stages can be conveniently cascaded by direct coupling without losses in coupling. For m stages in cascade, the gain (with reverse termination omitted) is

$$A = \left[ng_m Z\right]^m$$

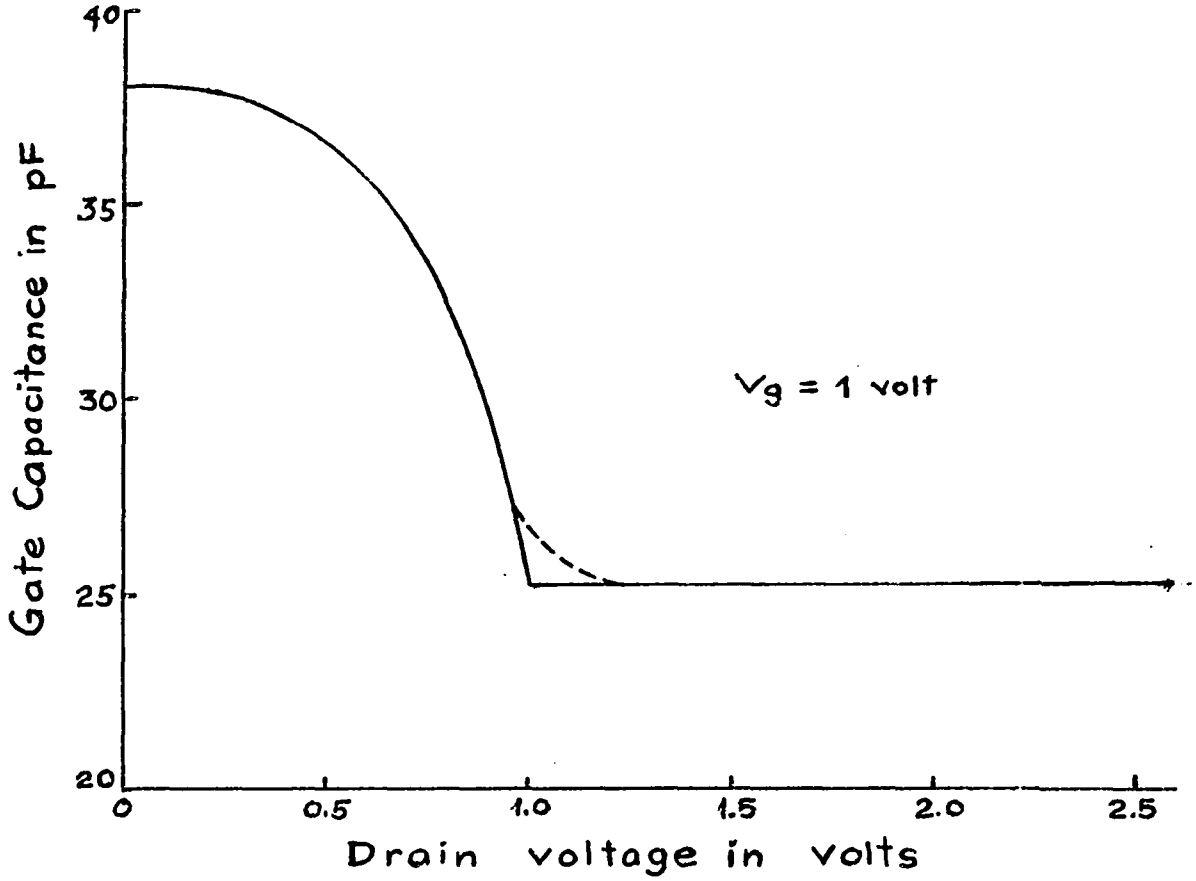


Fig. 21. Transistor gate capacitance

$$A = \left| n g_{mo} Z_o \frac{\sin(\phi x_k)/\sin\theta}{1 + j x_k} \right|^m \qquad (138)$$

$$= \left[7.2 \times \frac{\sin(1.42 x_k)/\sin\theta}{\sqrt{1 + x_k^2}} \right]^m . \qquad (139)$$

The variations of g_m and Z have compensation effect. The low frequency gain of a four stage amplifier is 57 db. The gain-band-width product is approximately

$$G \cdot BW = 122 \times 10^6 \times 5.12$$

$$= 620 \times 10^6$$

for a single stage. Equation (139) is plotted in Fig. 22.

For the reduction of peak response, the drain line can have a slightly higher actual cutoff frequency, say, 125 MC. It is apparent from Fig. 9, that for a slight change of ϕ and k, only the frequency near cutoff is affected when ϕ has a value such as 1.42. This is unlike the lumped filter case where only the product LC can be changed, and if so, additional phase distortion will be introduced over the entire band. To find the line length corresponding to 125 MC actual cutoff frequency (x_k=1.25), ϕ is first determined from equation (50):

$$1.25 \left(\frac{2}{\phi} - \frac{\phi}{2}\right) = \cot(0.625\phi)$$

$$\phi = 1.49 \quad \text{radians.}$$

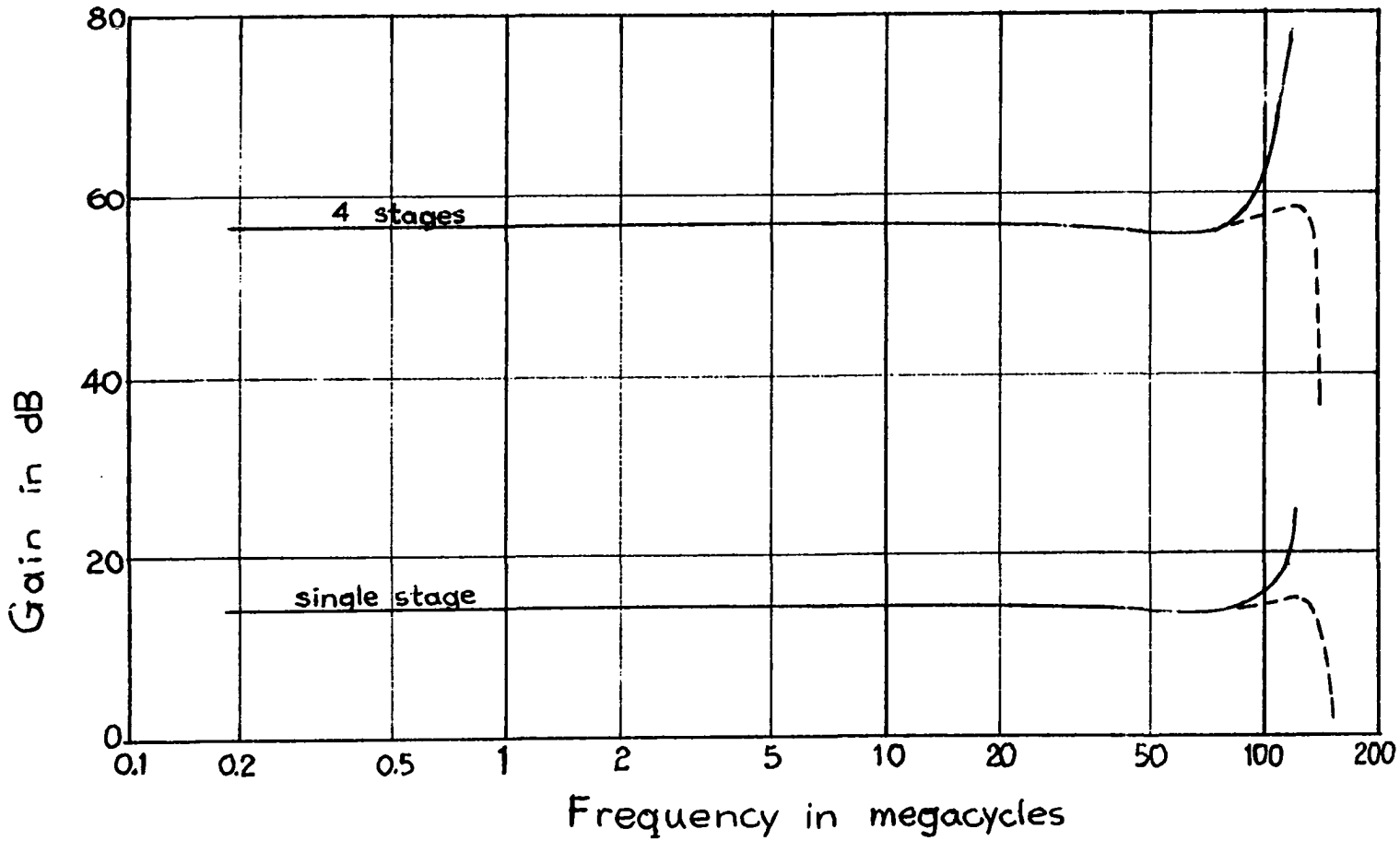


Fig. 22. Gain of the designed amplifier

$$\therefore \qquad k = 0.8 \ .$$

Equations (41) and (42) are used in equation (34), yielding the equation

$$\ell^2 \frac{K\mu_r}{c^2}(1 + k) = \frac{1}{\pi^2 f_c^2} \tag{140}$$

or

$$\ell = \frac{c}{\pi f_c \sqrt{K\mu_r(1 + k)}} \tag{141}$$

$$= 0.474 \text{ meters.}$$

This arrangement is shown in Fig. 27. The peak response within 122 MC is reduced by this phase shift effect; beyond 122 MC, it is attenuated by the gate line. The attenuation is given by

$$\alpha = \cosh^{-1}\left[2\left(\frac{f}{f_c}\right)^2 - 1\right] \tag{142}$$

which is equal to 0.21 nepers per section at 125 MC. The average number of gate sections which the signal passes through is two per stage. For four cascaded stages, the peak is theoretically reduced to 19% of its original value. After peak reduction the response may look somewhat like the dotted curves shown in Fig. 22.

The maximum percentage of phase shift deviation is calculated by comparing Fig. 19 with a linear phase shift line tangent to the curve

at the low frequency end point. This is plotted in Fig. 23. A dotted curve representing the lumped filter case is shown for comparison.

The circuit diagram is shown in Fig. 24. Drain power supply is 2.5 volts and gate bias is one volt. Three blocking capacitors C_1, C_2, and C_3 are included in the thin-film circuit. Their value is arbitrarily chosen to be 0.03 microfarads which gives a lower end cutoff frequency of about 83 KC.

A transmission line section is utilized in the coupling circuit. Since the input and output impedances are approximately equal, the coupling line section is identical to the section of gate line. This line section combining with output-end and input-end capacitances forms a π-network to provide smooth signal flow from drain line to gate line in cascade. External blocking capacitors should be added in series with the coupling line between stages.

The cross-sectional views of the strip line and the MOS transistor are shown in Fig. 25. The theoretical characteristic of the transistor given by equation (117) is drawn in Fig. 26.

By the nature of deposition processes, only layers of uniform thickness can be deposited. Consequently, the ground plate spacing of the line is thicker at the places where the center strips lie than at other places as shown in Fig. 25. The outer plate is not actually a smooth plane. In order to compensate the increase of capacitance due to this narrowed spacing, the upper half of the medium is thickened. The line capacitance can be thought of as consisting of two parts. One is the parallel plate capacitance formed by the upper and lower faces of the strip with the ground planes. The other is the fringing

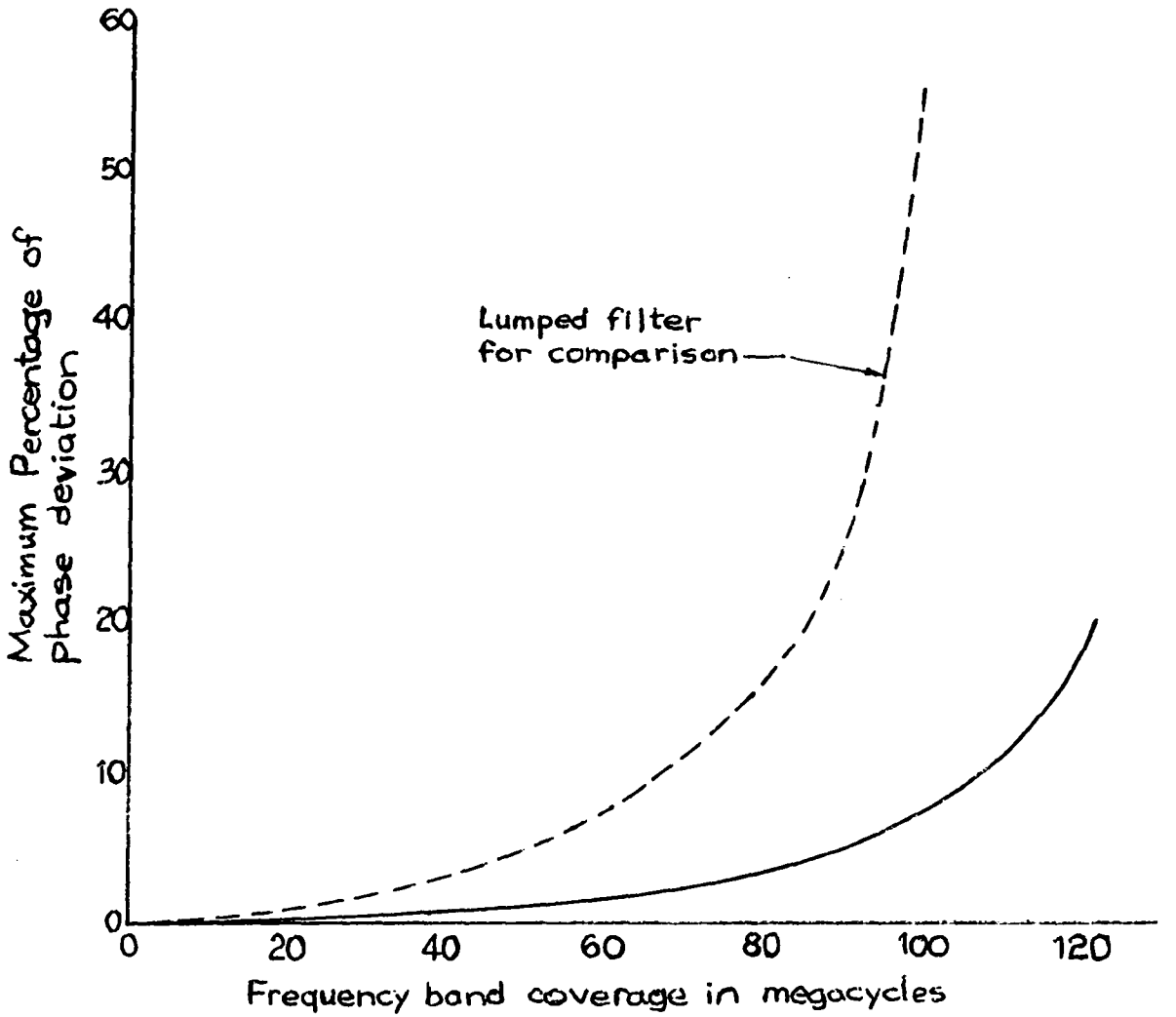


Fig. 23. Maximum phase shift distortion versus band coverage of the designed amplifier

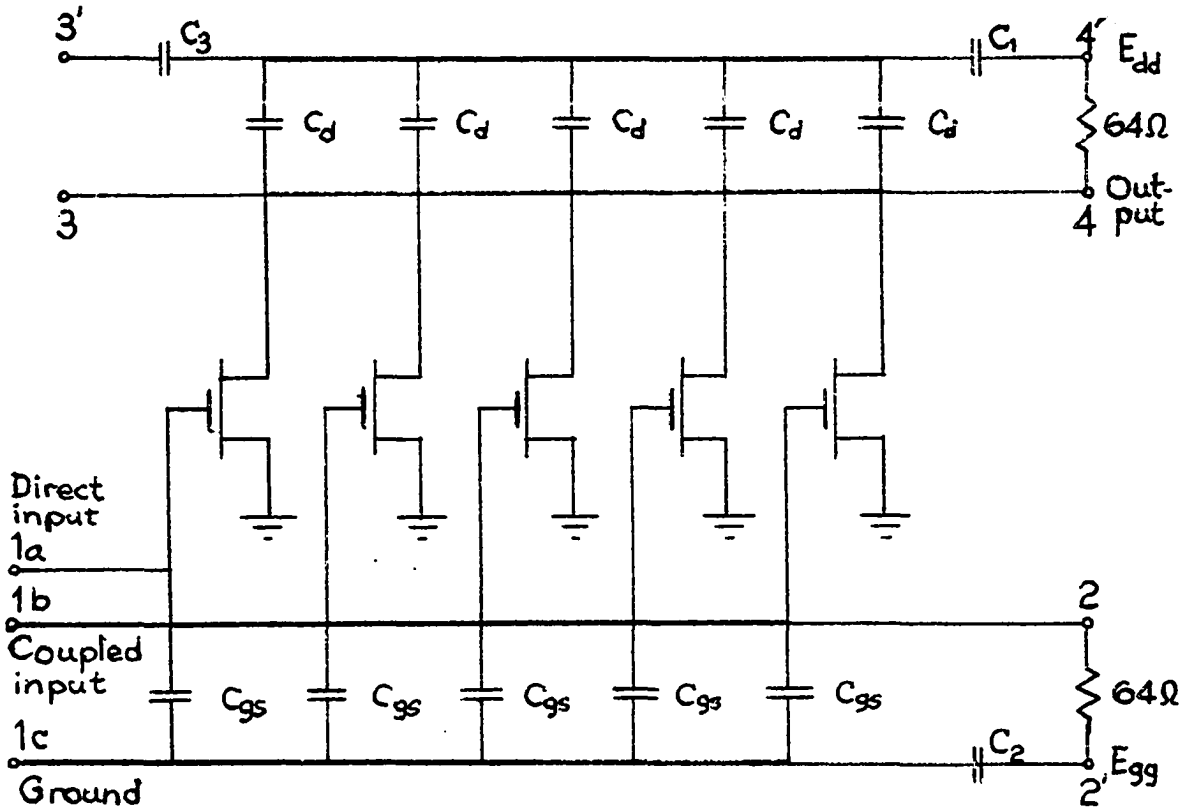
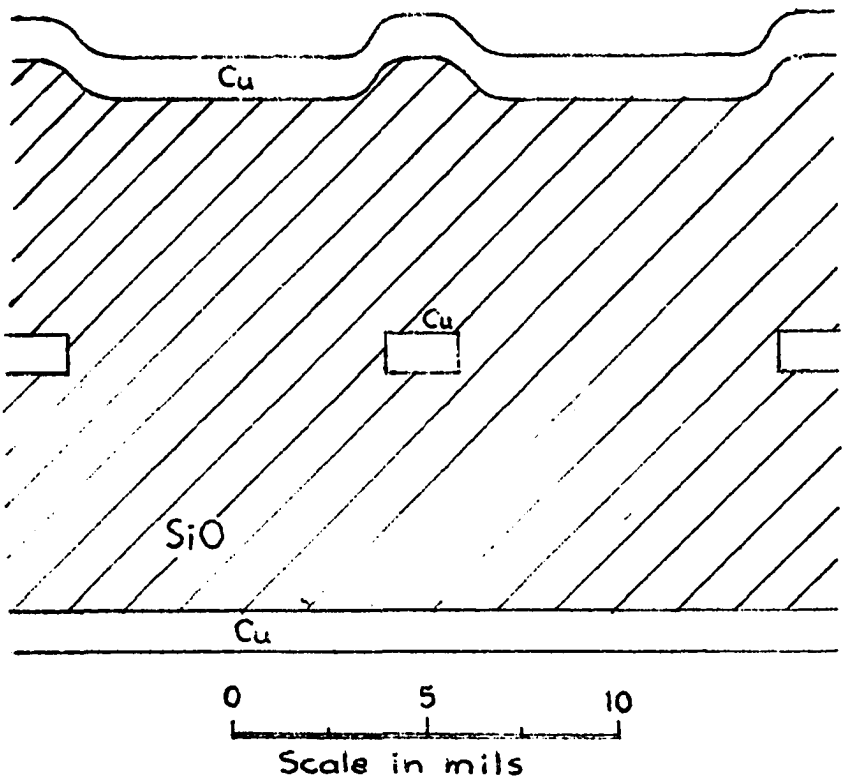
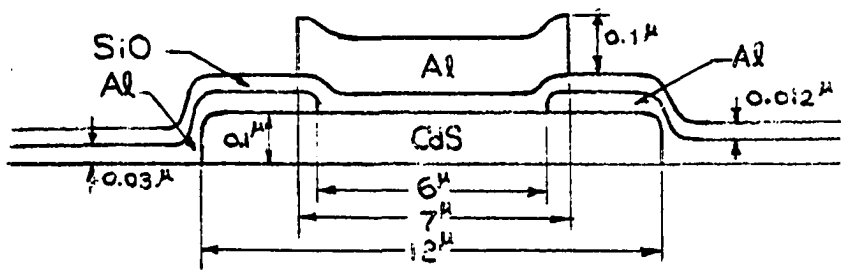


Fig. 24. Circuit schematic diagram showing one stage



(a) The strip line



(not shown to scale)

(b) The MOS transistor

Fig. 25. Cross-sectional view of the strip line and the MOS transistor

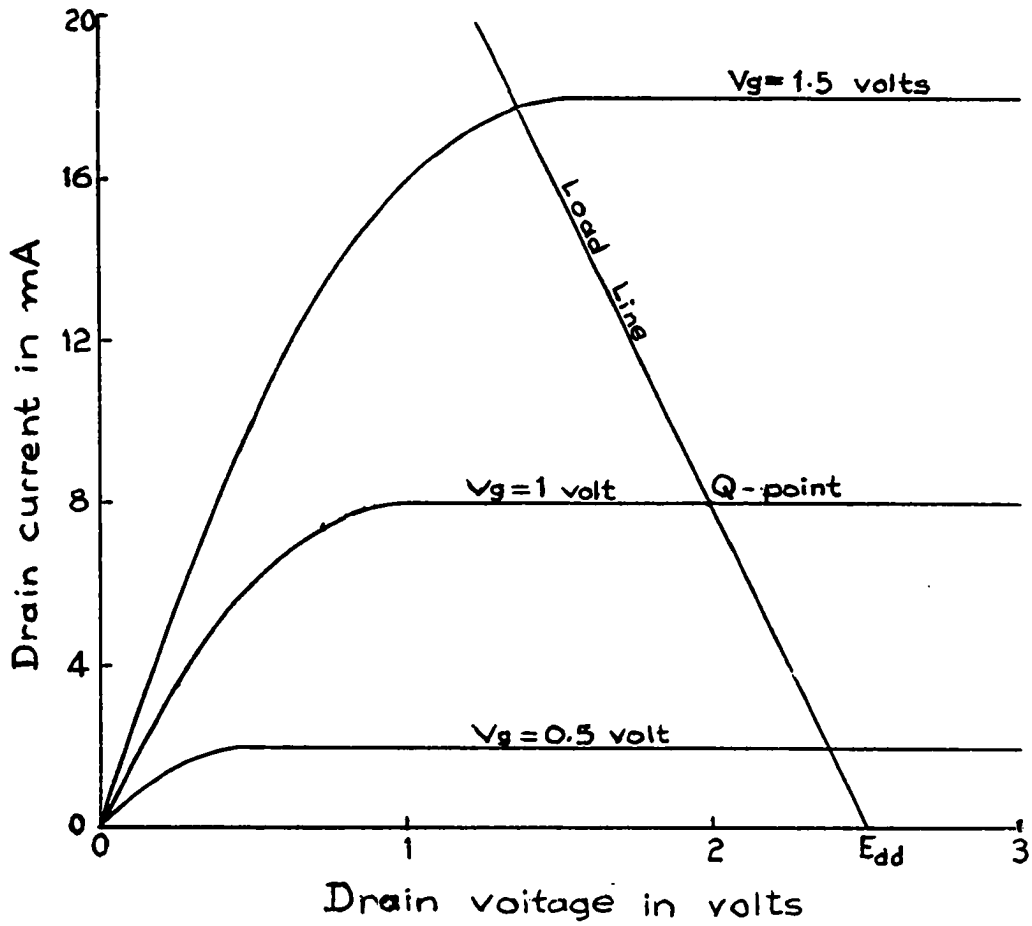


Fig. 26. Theoretical transistor characteristics

capacitance due to the side faces and the non-uniform fields. From Table 1 and Table 2 of Begovich's paper,[19] the fringing capacitance is found to be 78% of the total capacitance for the configuration in design. The upper parallel plate capacitance is then counted as 11%. Let y be the amount of thickness in microns by which the upper medium must be thickened. The increase in the fringing capacitance should be made equal to the decrease in the parallel plate capacitance, i.e.,

$$0.78C \frac{25 - y}{D - 25 + y} = 0.11C \frac{y}{\frac{D}{2} + y}. \qquad (143)$$

y is found to be 20 microns, hence, the upper medium should be 6.6 mils thick.

A 2"x2" glass substrate is chosen. The advantages of glass substrate are that the area can be larger in view of better insulation, construction can be more complex and the fabrication processes are simplified.[41]

The process of surface cleaning depends on the type of glass used. Summary of detailed cleaning processes has been given by MacAvoy and Halaby.[42]

Cadmium sulphide is to be deposited first. During this deposition, a substrate heater is used to keep the substrate temperature at about 180°C inside a vacuum system having an oil diffusion pump with a liquid nitrogen trap. This is to avoid an excess of dissociated cadmium in the deposited layer. The layer is to be recrystallized in the presence of copper or silver at temperatures above 450°C for the improvement of mobility.[43-45]

Accurate patterns are obtained by the photo-etch method utilizing photo-resist coating and glass masks. This method has been tested for MOS transistor models having six micron, eight micron and ten micron channel widths. The cut ruby-paper patterns were first reduced photographically by fifteen times using Kodak high-resolution 2"x2" glass plates, high resolution developer and fixer. Reversal or non-reversal pattern was made according to the special etching process needed for the layer over which the patterned film will be used as a mask. The reduced patterns were multiplied by the use of a step and repeat projector and Kodalith ortho-plates. The patterns were further reduced by fifteen more times to their actual size. The glass masks thus made were accurate and clearly defined.

For the photo-resist coating, the Kodak metal-etch resist, the Kodak photo-resist and the AZ-1350 coating of the Shipley Co. have been tested. The AZ-1350 coating together with its associated developer and remover gives best resolution and easiest removal. The coating was applied by dipping method and was drained at 60 degree inclination at room temperature for 40 minutes to one hour. It was then baked, exposed and developed. Each process has its optimum time depending upon the special substance and thickness of the film and the etching method used. Though these processes have interdependent parameters, they must be optimized in their order one at a time before the whole process can become optimum and the high resolution of one-half micron can be obtained. These optimum times have been determined for the MOS transistor models.

The optimum baking time was found to be ten minutes at $60^{o}C$

oven temperature with ventilation. Without baking, the development time became short and very critical. Otherwise the fine gate electrodes are loosened and deformed. Too much baking time produced a "shadow" effect on the film edge which reduces the resolution. The baking is especially needed for fine structures. The optimum time for exposure was four minutes for a 275 watt ultra violet lamp at one foot distance. A light collimator was usually needed and the time was increased accordingly. Best development time was found to be one minute for concentrate AZ remover solution.

Aluminum layers were etched by 1% NaOH solution. To obtain chemical resistance to NaOH for the coating, the substrates were reheated at 140°C for ten minutes before etching. The etched aluminum patterns were satisfactory.

Metal masks have also been tested. The best result was obtained with steel plates using ferric chloride as etching solution. Metal masks can be used in the fabrication processes of the strip lines.

The layout diagram of the substrate is drawn in Fig. 27. A detail diagram of the transistor blocks in Fig. 27 is shown in Fig. 28.

The neighboring strip separation is ten mils. The transverse attenuation between neighboring strip calculated from equation (70) is

$$10\alpha_t = 10 \times \frac{27}{D}$$

$$= 21.6 \text{ dB.}$$

The ground planes extend enough over the edges of the center strips to provide uniform line constants and perfect shieldings.

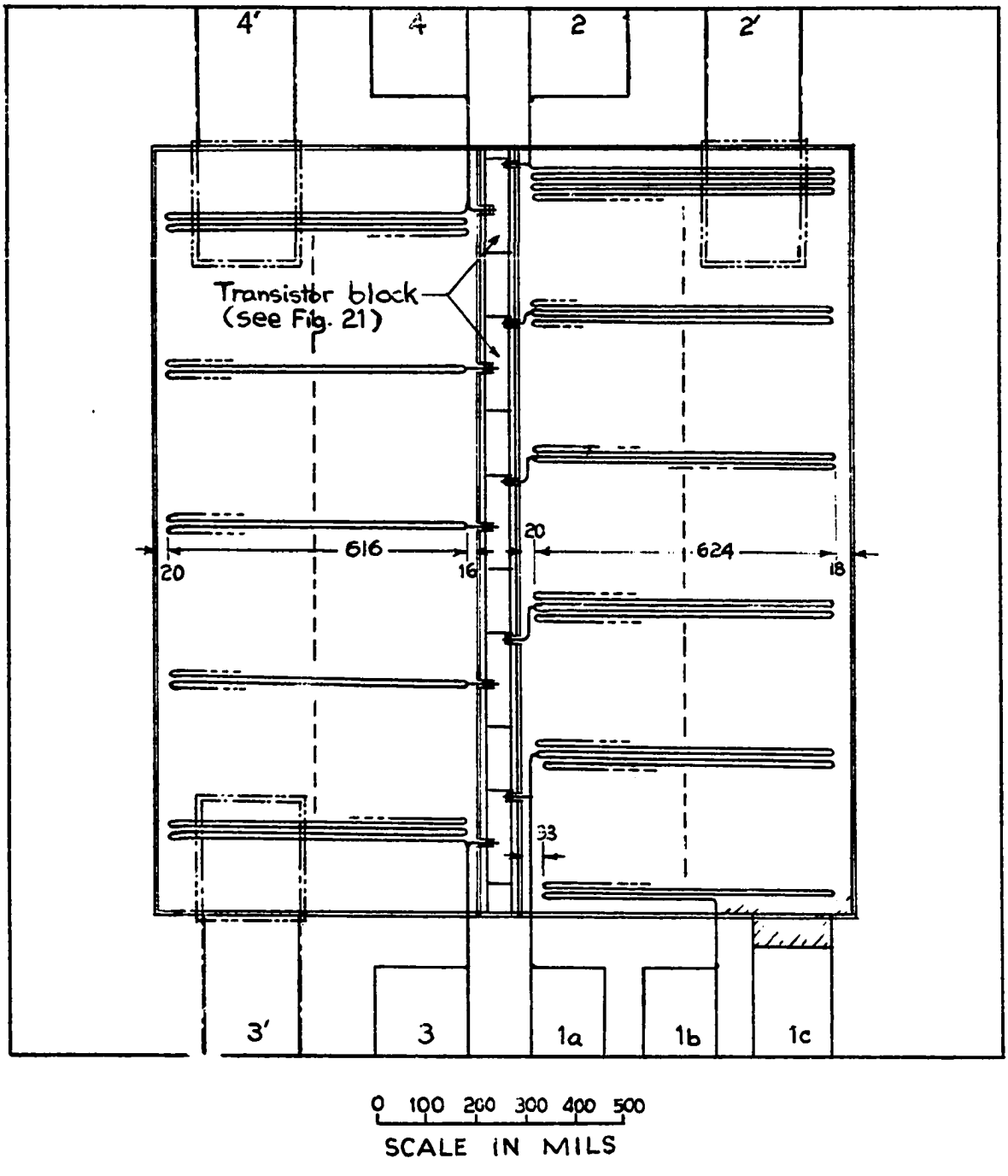


Fig. 27. Layout of the substrate

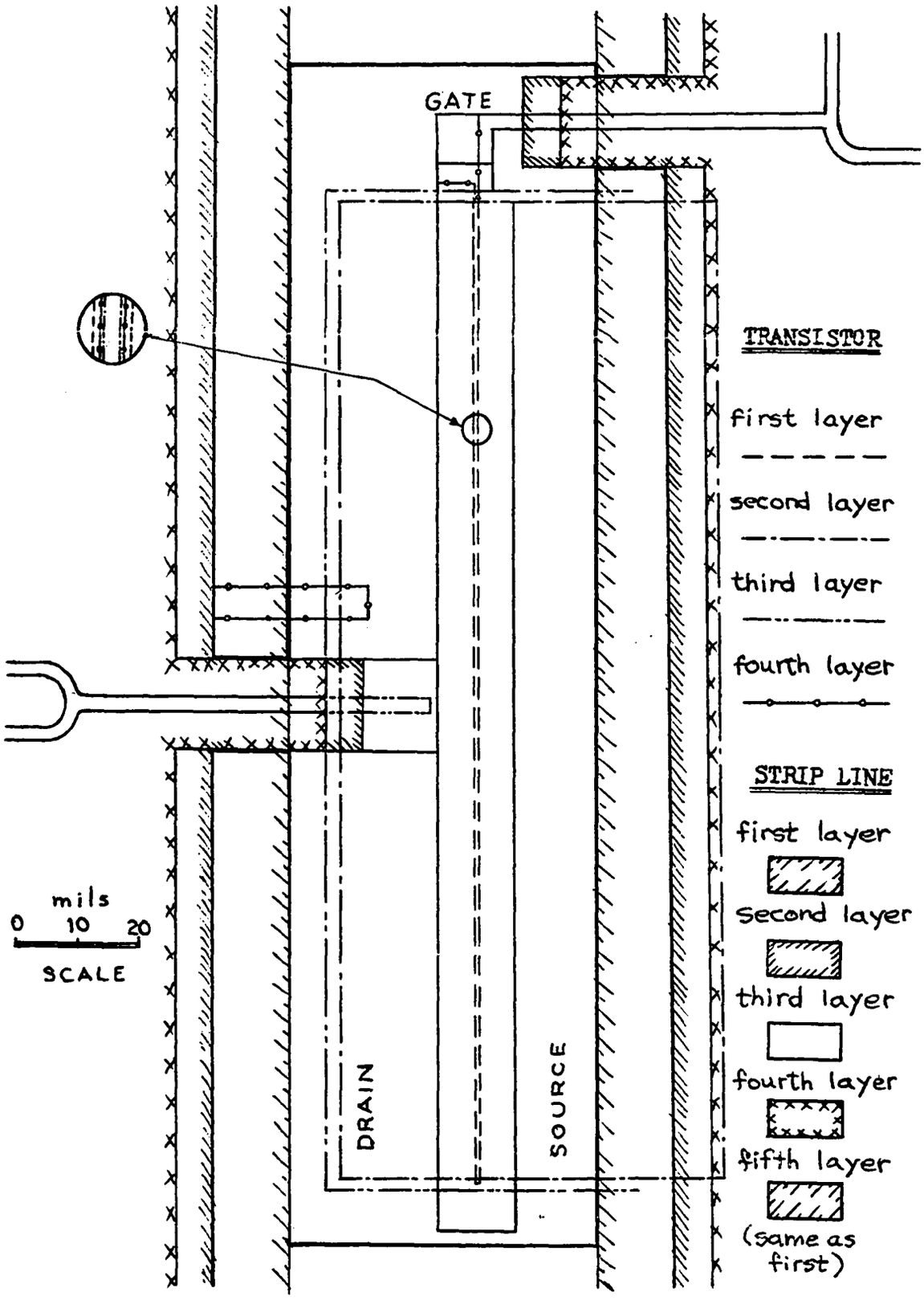


Fig. 28. Transistor block details

There are 28 turns (bends) per section in the gate line and 30 turns per section in the drain line. The gate line has an additional section provided for coupling use, utilizing the space available.

The transistor blocks having four layers are first fabricated using photo-resist masking. The resolution will be one-half micron. The pattern of transistor blocks can be obtained by the repeat projector. The second deposition after the first cadmium sulphide layer produces the aluminum drain and source electrodes, a part of the latter will be covered directly by the ground plate of the transmission line. The silicon monoxide insulator is the third layer which actually covers the whole transistor except the connection areas. The second and third depositions are also used to make the blocking capacitors C_1, C_2, and C_3. The fourth layer yields the gate electrodes and the drain line loading capacitors.

When the transistor blocks are finished, the strip lines are then deposited. The sandwiched strip line has five layers. Metal masks will be used except for the center strips (third layer) which must be made by a photo-resist coating method. The deposition through the metal mask is direct, no etching process on the substrate is involved. The designed resolution for the metal masking can be as rough as six mils, the fabrication of the metal masks if therefore simplified.

For the consideration of the mechanical strength of the metal masks, the ground plates (first and also last layers) of the gate and drain lines are separated. During the deposition of the center strips, they are connected together. The design has the advantage of avoiding any chance of ground line coupling between input and output circuits.

Separate ground returns are usually important in ordinary distributed amplifier construction.

These connections between gate and drain ground plates also seal up the edges of the sandwiched lines and provide isolation between transistors. The chance of a coupling between lines or between line and transistors is completely eliminated.

The second and fourth depositions are silicon monoxide layers which are again separated into two parts for mask strength consideration and the prevention of guided modes.

A dielectric piece is deposited over the gate electrode during the deposition of the second layer for protection against possible etching in the fabrication process of the center strips. The MOS transistors are thus completely enclosed with the dielectric layers which will resist moisture, oxidization, etc.

There are 0.3-inch spaces left on two sides of the substrate. Output and input terminals are on opposite sides with separate ground terminals. The cascading of stages is very convenient.

CHAPTER IV

CONCLUSION AND RECOMMENDATION

It has been shown that uniform transmission lines and thin-film MOS transistors can be used in distributed amplifier circuits. At very low frequency, the amplifier, as constructed with uniform transmission lines, behaves as an amplifier with lumped LC filters. At the low frequency end the transmission line is approximately a straight through four terminal network and the amplifier stage is simply parallel connected. An equivalent LC π-network where the values of series inductance and shunt capacitances vary widely with frequency has been taken as the model of a transmission line section. The transistors connected to the lines constitute the additional capacitive loads which are fixed with frequency. Mathematical analysis following this model shows that the actual cutoff frequency of the amplifier is not obtainable if a fixed value LC π-network approximation for the line section is employed in calculation. The behavior of distributed amplifiers using uniform lines must differ from that using lumped LC filters. In view of more variables involved in the transmission line case, it is desirable to define a normalized loading ratio, k, and a normalized angular length of the line section, ϕ. There exists a maximum allowable length of line section corresponding to the value 2 radians, (ϕ=2), for

any given cutoff frequency although the phase shift per section ranges from zero to π radians in the pass band. When ϕ varies from 0 to 2, k varies from infinity to zero. In terms of these two quantities, formulas have been derived and characteristics have been plotted. These formulas and characteristics are universal and useful in all cases for amplifiers of this type. The traditional lumped distributed amplifier is included as a special case corresponding to $\phi=0$. This may be seen from the fact that the universal formulas can be reduced to the traditional formulas mentioned in the beginning of Chapter II by letting ϕ approach zero. For example: the phase shift per section given by

$$\cos\theta = \cos(\phi x_k) - (\frac{2}{\phi} - \frac{\phi}{2})x_k \sin(\phi x_k) \tag{48}$$

can be reduced to

$$\cos\theta\Big|_{\phi\to 0} = \left[\cos(\phi x_k) - 2x_k^2(\frac{\sin(\phi x_k)}{\phi x_k} - \frac{\phi\sin(\phi x_k)}{4x_k})\right]_{\phi\to 0} \tag{144}$$

$$= 1 - 2x_k^2$$

$$= 1 - 2(\frac{f}{f_c})^2 \tag{5}$$

which is the phase shift formula for the lumped case; and the impedance formula given by

$$Z = \sqrt{\frac{L}{C}}\,\frac{\sin(\phi x_k)}{\sin\theta} \tag{59}$$

can be reduced in the following way. Since by equation (45)

$$\sqrt{1 + k} = \frac{2}{\phi},$$

the normalized impedance can be expressed as

$$z_{nor.} = \frac{z}{z_{x_k=0}} = \frac{z}{\sqrt{\frac{L}{C(1 + k)}}}$$

$$= \sqrt{1 + k}\,\frac{\sin(\phi x_k)}{\sin\theta}$$

$$= \frac{2x_k}{\sqrt{1 - \cos^2\theta}}\,\frac{\sin(\phi x_k)}{\phi x_k}. \qquad (145)$$

Letting $\phi \to 0$, this formula reduces, by the use of equation (144), to

$$z_{nor.} = \frac{2x_k}{\left[1 - (1 - 2x_k^2)^2\right]^{\frac{1}{2}}}$$

$$= \frac{1}{\sqrt{1 - x_k^2}}. \qquad (146)$$

Transforming back to the impedance without normalization,

$$z_{nor.} = \frac{z_{x_k=0}}{\sqrt{1 - x_k^2}} \qquad (14)$$

which is the impedance formula for the lumped case.

Better phase shift performance is obtained for the transmission line type amplifier. The phase shift characteristic of this type amplifier has increasing linearity when ϕ is increased, with the limiting case $\phi=2$ representing the pure unloaded smooth line which gives no phase shift distortion at all. The phase distortion can be reduced to any desired amount by choosing a proper value of ϕ(or k), contrasting to the lumped type where the amount of phase shift distortion is fixed no matter what series inductance to loading capacitance ratio is chosen. The increased phase linearity is important when amplifier stages are to be cascaded.

A smoother impedance variation (hence gain) over the pass band is also obtained. The range of the peak response produced near cutoff frequency is narrowed. The peak value may be reduced for the transmission line case by using slightly different lengths of input and output lines without introducing appreciable phase distortion over the pass band. The characteristics of a traditional distributed amplifier with lumped filter sections can be improved by introducing negative feedback between coils as first proposed by Ginzton.[1] This changes the ladder filters to equivalent m-derived networks. This method will introduce an increased attenuation of the amplitude characteristic in the middle of the pass band.

Design curves for the discussed amplifiers have been drawn. For a desired phase shift and amplitude tolerance, the values of ϕ and k can be chosen from the curves.

The feasibility of utilizing the transmission lines in distributed amplifiers makes it convenient to design a thin-film distributed

amplifier. The annoying problems associated with traditional distributed amplifiers, such as lead inductance loading effect, self resonance of coils, stray capacitances, coupling between input and output circuits, etc., are eliminated by the use of thin-film construction and strip lines. For isolation of fields between input and output lines, the sandwiched strip line is recommended because of its near perfect self confinement of electric and magnetic fields within its ground plates.

The tolerance on the accuracy of values of the thin-film components as required by the amplifier performance has been investigated and found to be generally quite loose for the transmission line case. Sensitivities of the gain and the cutoff frequency due to changes of the strip line thickness and the transistor loading capacitance have been shown to be small. The effects of changes of line capacitance and inductance on the cutoff frequency tend to cancel each other as compared with the lumped filter case where such compensation does not exist.

It is convenient to use silicon monoxide as the medium insulating the center strip of the sandwiched transmission line. This reduces the line length needed and is desirable since the space available is quite limited. The strip lines will be bent on a thin-film substrate. A circular bend having a strip spacing to width ratio of 5:1 is used. This will give negligible attenuation loss. The transverse attenuation between neighboring strips is 21.6 dB, therefore, unwanted coupling is very small.

A thin-film distributed amplifier using sandwiched strip lines and MOS transistors in the enhancement mode has been thoroughly designed

with its performance predicted. It is recommended that the transistors be operated in the saturation mode and coplanar construction be adopted. The saturation mode is advantageous due to its stable capacitive loading as discussed in Chapter II. The coplanar construction is recommended for ease in thin-film manufacturing, since substrate heating procedures and the number of masking processes are grave economic considerations.

The theoretical calculations associated with this design indicate fairly linear phase shift and amplitude characteristics with an angular length of section ϕ=1.42 radians and a loading ratio k=0.985. The gain for the four stage cascaded amplifier is 57 dB with an actual cutoff frequency of 122 megacycles per second. The transistors of the designed amplifier have moderate saturated gate-to-source capacitance values and high transconductances. The dimensions of the sandwiched strip lines has been optimized so that their occupied space is a minimum. The fractional sensitivity of impedance change due to deviation of line thickness is only 0.44. The fractional sensitivity of cutoff frequency change due to line thickness deviation is as low as 0.11 and that due to transistor capacitance change (for various operating points) is 0.25.

The photo-etch method by which accurate patterns are obtainable has been tested for MOS transistor models having six micron, eight micron, and ten micron channel widths using various photo-resist coatings. The use of Shipley Co. type AZ-1350 coating produced the best results with accurately defined patterns after going through optimization procedures. It is recommended that the same careful optimization procedures used to eliminate the process variables one at a time be taken

for the purpose of obtaining the one-half micron high resolution required by this design since the channel length is only six microns, which is narrowed for the benefit of high frequency response and high transconductance. For the fabrication of the thin-film distributed amplifier stages, the author recommends the pattern of the transistor block be reduced photographically and multiplied by a repeat projector.

The method using metal masks has also been tested with good results for application in the fabrication of strip lines. The strip lines are to be deposited after the deposition of MOS transistors. The resolution of metal masks for this design can be as rough as six microns. It is quite easy to prepare such masks. The use of materials during the deposition of strip lines to complete the capsulization of transistors is recommended.

There are five transistors in a single substrate stage associated with the input and output strip line sections, the between-stage coupling line section and three blocking capacitors. Connection terminals are located on two sides providing very easy cascade operation.

The practical feasibility of a thin-film distributed amplifier has been indicated, and it is recommended that experimental amplifiers of this type be developed. Such distributed amplifiers are expected to find wide use in video and broadband VHF and UHF amplifiers.

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