AN ULTRA-LOW POWER RF RECEIVER BASED ON DOUBLE-GATE CMOS (FINFET) TECHNOLOGY

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AN ULTRA-LOW POWER RF RECEIVER BASED

ON DOUBLE-GATE CMOS (FINFET)

TECHNOLOGY

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Subthreshold region: include weak and moderate inversion

Moderate inversion: Gate-to-source voltage is close to threshold voltage.

Weak inversion: Gate-to-source voltage is far below threshold voltage.

Inversion coefficient: parameter describing the transistor's working region, for example, weak, moderate and strong inversion

Chapter 1

Objective

1.1 Motivation

In the past 40 years, many kinds of electronic circuits were developed at an amazing speed. The low power integrated circuit (IC) is one of the targets designers are pursuing. Among the applications of low power ICs, wireless RF transceivers are new emerging application that requires small size, low cost and low power. One of the most critical components in wireless transceiver is the wireless receiver.

The objective of this research is to study and realize an ultra-low power RF receiver based on double-gate CMOS (FinFET) technology. In this work, tradeoffs and strategies for low power receiver design are investigated. A low power global position system (GPS) receiver is taken as an example to test our study.

1.2 Overview

This dissertation is organized as follows. Chapter 2 describes techniques for the design of analog circuits for low power. It focuses on the importance of moderate inversion usage in this design, which is the main method to reduce the power consumption of RF receiver. Chapter 3 and 4 focuses on the design, test and model integrated passive devices, such as inductors and varactors. Chapter 5 introduces a new double-gate CMOS architecture, FinFET. We characterized the FinFETs with I-V, C-V,

and S-parameter measurements at GHz frequency range. A BSIM3SOI model is developed for further implementation and validation of the FinFET transistor RF circuits in moderate inversion. Starting from Chapter 6, we apply the passive and active devices to the GPS receiver front-end circuit design. In Chapter 6, the GPS receiver's architecture, system design and implementation requirement are described. Chapters 7 to 9 describe the GPS receiver front-end sub-blocks, such as ultra-low power LNA, VCO and mixer design, respectively. The performances and trade offs of each building blocks are summarized at the end of each chapter. Chapter 10 concludes the dissertation with a brief summary of results and discussion of future research directions.

Chapter 2

Low Power Techniques

2.1 Introduction

The silicon CMOS technology has become dominant in integrated circuits. CMOS gate lengths have reduced from 10um in the 1970's to the present day geometries of less than 90 nm. According to the 2004 International Technology Roadmap for Semiconductors (ITRS), by 2006, MOS transistors with a physical gate length of 80 nm will become widely available. Its scalability provides decreased power consumption at enhanced performance levels. When the CMOS devices are scaled into the sub-100nm dimension, the deep sub-micron CMOS opens up new frontiers in low voltage and current circuit design. In this chapter, design techniques are outlined first, and the advantages of modern CMOS devices are analyzed and the ultra low power consumption for RF front end circuits is investigated.

2.2 Low Supply Voltage Technique

Conventional CMOS technology has, for over 3 decades, been locked into designing processes with high performance digital circuits as the objective. Analog/RF designers basically just used discrete solutions or hybrid blocks of bipolar GaAs, and more recently BiCMOS and Heterojunction Bipolar Transistors (HBT). Not only are digital device models not sufficient for the accurate circuit simulation, the analog/RF designer must face a constantly shrinking design space. One of the most difficult

problems is the constantly decreasing supply voltage for modern CMOS processes, causing reduced voltage headroom and dynamic range for analog and RF application [1].

2.1.1 Opportunities for Reduced Supply Voltage

Here a typical differential local oscillator (LO) is shown in Figure 2.1. It is an example capable of operating with a very low supply voltage. It contains two stacked transistors. The inductors comprising the resonant load do not consume additional voltage headroom, additionally the output is allowed to swing above the supply voltage, VDD. Theoretically, the LO may operate on a supply voltage as low as VDsat1+VDsat3, where VDsat is the MOSFET saturation voltage. Furthermore, if the devices M1 and M2 are designed to operate in the subthreshold regime, VGS and VDsat may be quite small.

The main challenge in operating under a low VDD is the reduction in output voltage swing. Generally, system level considerations are critical when designing low voltage circuits and choosing the optimal power supply voltage. Supply voltage is not typically considered a variable parameter available to the designer, because it is impractical from an integration perspective if each component requires its own unique supply. However, it is entirely reasonable that two supply voltages will be available in a network environment: e.g. high voltage for active mode and low voltage for sleep mode. Recent research in low voltage digital design has shown that significant savings in memory leakage power may be achieved by reducing the supply to a few hundred mill volts during standby periods [2]. If a lower voltage supply is made available for use in digital standby mode, it may also be available for analog circuits [3].

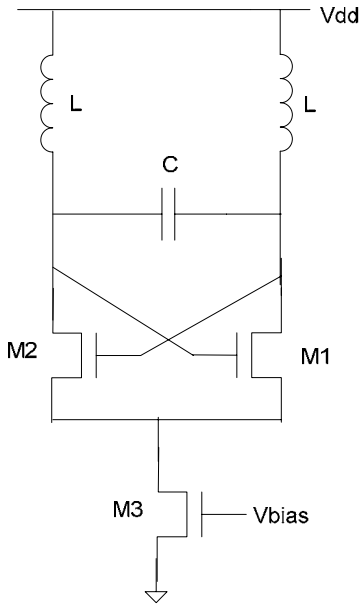


Figure 2.1 Schematic of low power supply LO.

2.2.2 Challenges for Low Power Supply

For analogue circuits, down-scaling supply voltage and process feature size will not automatically reduce power consumption and, in fact, usually it often has the opposite effect in analog design. In analogue chips, power is consumed to maintain the signal energy above the thermal noise floor in order to achieve the desired signal-to-noise ratio or dynamic range. Since minimum power consumption is related to the ratio between supply voltages and signal amplitude, power-efficient analogue circuits should be designed to maximize the voltage swing. Reducing the supply voltage, while maintaining the signal-to-noise ratio and bandwidth, therefore requires that the transconductance be increased. This is normally done at the expense of power or by reduced channel length. Therefore the approach for analogue designs must therefore be different.

2.3 Subthreshold Operation Technique

2.3.1 Fundamental of Subthreshold Operation

For gate-source voltage (V_{GS}) less than the extrapolated threshold voltage V_t but high enough to create an inversion region at the surface of the silicon, the device operates in the subthreshold region. In this work, both weak and moderate inversion are considered as subthreshold operation even we know V_{GS} may larger than V_t in moderate inversion. Later in this chapter we will point out this work is based on moderate inversion because of the bandwidth limitation.

In subthreshold region, the channel charge is much less than the fixed charge in the depletion region and the drain current arising from the drift process is negligible. The drain current is caused by a gradient in minority-carrier concentration, i.e. diffusion current.

In subthreshold operation, the surface potential is approximately a linear function of the gate-source voltage [4]. Assume that the charge stored at the oxide-silicon interface is independent of the surface potential in the subthreshold region, and then changes in the surface potential $\Delta\psi_s$ are controlled by changes in the gate-source voltage ΔV_{GS} through a voltage divider between the oxide capacitance C_{ox} and the depletion-region capacitance C_{js}. Therefore,

$$\frac{d\psi_s}{dV_{GS}} = \frac{C_{ox}}{C_{js} + C_{ox}} = \frac{1}{n} \tag{2.1}$$

where n is called subthreshold slope factor and takes on a values from 1 to 2.

The drain current equation in the subthreshold region is

$$I_D = \frac{W}{L} I_t \exp\left(\frac{V_{GS} - V_t}{nU_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{U_T}\right)\right] \tag{2.2}$$

where U_T is the thermal voltage. V_t is the gate to source threshold voltage. I_t is intrinsic or specific current.

$$I_t = 2n\mu_0 C_{ox} U_T{}^2 \tag{2.3}$$

Physically, I_t represents the characteristic current for the device in the center of the moderate inversion region, providing a convenient normalization factor. The drain current of a given device may be normalized to I_t, producing the inversion coefficient,

$$IC = \frac{I_D}{I_t \frac{W}{L}} \tag{2.4}$$

The inversion coefficient provides a very useful way of identifying the operation region and level of inversion [5] of MOS transistors,

$IC << 1$: Weak inversion

$IC \approx 1$: Moderate inversion

$IC >> 1$: Strong inversion

Unlike in strong inversion, the minimum drain-source voltage required to force the transistor to operate as a current source in the subthreshold region is independent of the overdrive [4].

Calculating $\partial I_D / \partial V_{GS}$ from (2.4) and using (2.3) gives

$$g_m = \frac{W}{L}\frac{I_t}{nU_t}\exp\left(\frac{V_{GS}-V_t}{nU_T}\right)\left[1-\exp\left(-\frac{V_{DS}}{U_T}\right)\right] = \frac{I_D}{nU_T} = \frac{I_D}{U_T}\frac{C_{ox}}{C_{ox}+C_{js}} \tag{2.5}$$

The ratio of the transconductance to the current of an MOS transistor in subthreshold region is

$$\frac{g_m}{I_D} = \frac{1}{nU_T} \tag{2.6}$$

The Equation above predicts that this ratio is independent of the overdrive, ΔV . For the transistor in the strong inversion, the g_m / I_D ratios is

$$\frac{g_m}{I_D} = \frac{2}{\Delta V} \tag{2.7}$$

where ΔV is the overdrive voltage. Comparing (2.6) to (2.7), we find the g_m / I_D of subthreshold region may 4 to 8 times higher than in strong inversion.

2.3.2 Advantages of Subthreshold Operation

Motivated by the needs for low power narrow-band wireless communication systems, the micro-power RFIC front-end, a LNA combined with a down-conversion mixer, has been designed using weak inversion CMOS techniques [6].

Within the active (saturation) region a device may be biased in the moderate or weak inversion region. The available transcondance per amp may 4 to 8 times higher than in strong inversion. This can be a big benefit for wireless applications where power consumption is much concerned if the bandwidth is available.

The second advantage of subthreshold operation is the relatively low drain saturation voltage $V_{Dsat,}$ which is typically around 3 to 4 U_T (about 78mV) [7] at room temperatuer. More practically as a result of anticipated temperature variation $V_{Dsat,}$ must be greater than 120mV. Compared with strong inversion, the value of V_{Dsat} in weak inversion is independence of gate voltage. The low saturation voltage implies that transistors operating in weak or moderate inversion require less overhead resulting in greater headroom than do devices in strong inversion. Therefore subthreshold operation is a natural choice for circuits operating with reduced supply voltage when the bandwidth is available.

The third advantage of subthreshold operation is low flicker noise achieved in moderate inversion since the flicker noise is reduced with less current flow [8, [9]. A detailed explanation follows in chapter 5.

Finally, nonlinearity is not a problem. In subthreshold region the third order intercept point voltage (V_{IIP3}) is approximately [10]

$$V_{IIP3} = 4U_T \approx 100 - 120mV \tag{2.11}$$

If the system signal is much less than 100 mV we could ignore the effects os V_{IIP3}. The second order intercept point voltage (V_{IIP2}) is inversely proportion to input offset voltage (V_{os}) [10]

$$V_{IIP2} = \frac{4(U_T)^2}{V_{OS}} \tag{2.12}$$

For 80 nm FinFET the V_{OS} is approximately 4.8 mV per square root of finger numbers [11]. For a 200 um device it has 2000 fingers. The V_{OS} is calculated 0.1 V. Thus the V_{IIP2} is 25 V. Since for this work the amplitude of signal is on the order of micro-volts, the effects of IP2 and IP3 could be ignored.

2.3.3 The challenges of Subthreshold Operation

Although there are many advantages obtained in weak inversion region there are drawbacks as well. The first and obvious problem is the reduced bandwidth. Traditionally, transistors for high frequency applications are operated in strong inversion to take advantage of the high device transit frequency (f_T) in this regime. Transit frequency is defined as the frequency where the current gain of the device falls to unity and is normally given by:

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{2.9}$$

Since g_m in weak or moderate inversion may be ten or more times smaller than that in strong inversion mode, f_T in the weak inversion is several orders of magnitude below that in the strong inversion although the Cgs in subthreshold may several times smaller than that in strong inversion shown in Figure 5.15 in Chapter 5. In the past, this speed limitation prohibits the applications in RF design. However, technology scaling is beginning to provide the solution since in the weak or moderate inversion, f_T is inversely proportional to the square of the channel length in (2.10)

$$f_T \approx \frac{I_t e^{\frac{\Delta V}{nU_T}}}{L^2 C_{ox}} \tag{2.10}$$

The present deep submicron CMOS technology makes this feasible. As shown in Figure 2.2 [3], the peak f_T is around 100GHz, decreasing sharply at lower inversion coefficient. At the center of moderate inversion, indicated by the vertical line at IC equal 1, f_T is approximately 5 GHz for the 130nm process. The bandwidth is adequate to implement circuits operating in the hundreds of MHz or above. In the Figure 2.3, device f_T is simulated across inversion level for three generations of submicron CMOS. At the center of moderate inversion, f_T is approximately 6 GHz for 180 nm, 12 GHz for 130 nm, and 21 GHz for 90 nm node. The current state of the art, 90nm CMOS device, can provide sufficient bandwidth for subthreshold circuits up to the low GHz range, such as GPS receiver front end which works at 1.5 GHz. From now on, we will only concentrate on the moderate inversion since it can provide enough bandwidth for low GHz application.

As a result the expected gm efficient improvement is only expected to be 2 to 4 greater than square law.

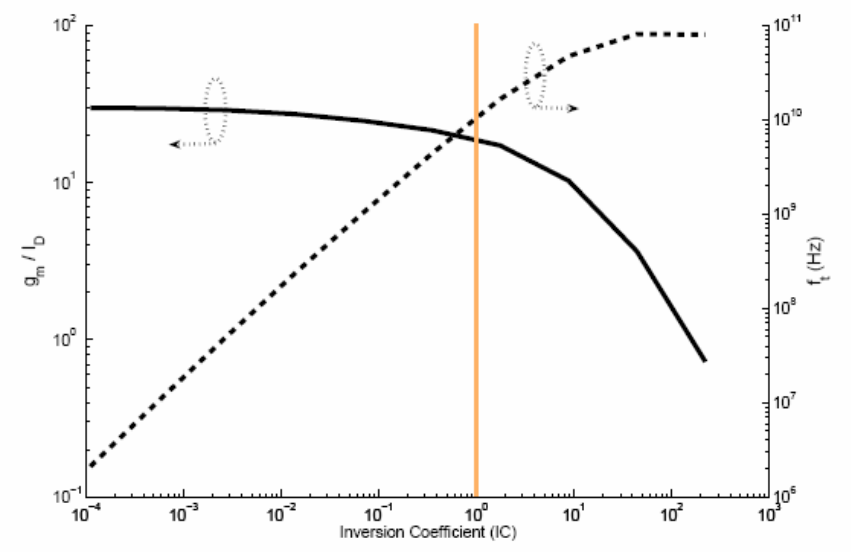


Figure 2.2 g_m/I_D and f_T for a modern CMOS 0.13um process [3].

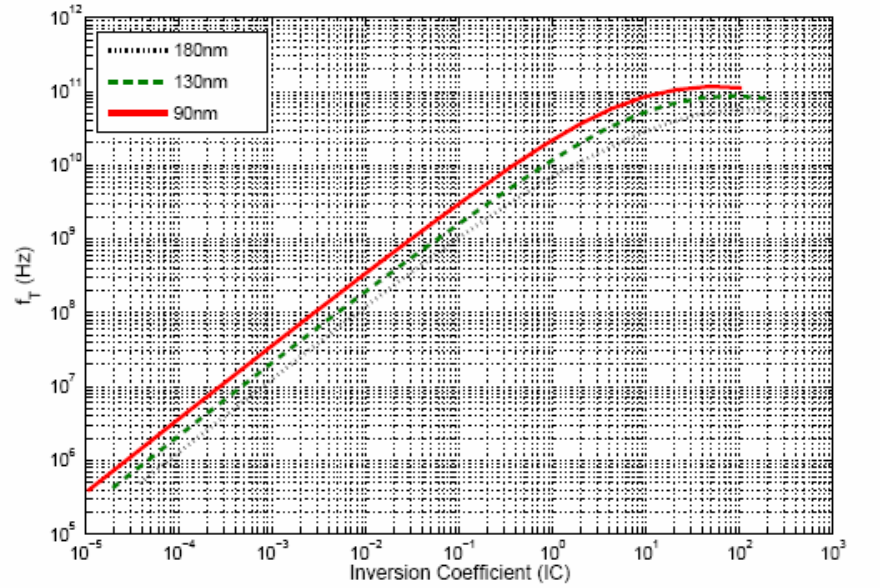


Figure 2.3 Comparision of f_T with technology scaling [3].

In addition to the reduce f_T , the current mismatch is another problem. In subthreshold region the drain current has an exponential relationship with the gate

voltage. As a result any small change in the gate to source voltage will have a larger change in drain current, which makes it unpredictable for the circuit. Fortunately, with the device area increase the current mismatch will decrease since [12]

$$A_{\Delta I} = \pm \frac{1}{\sqrt{fin}} \cdot \sqrt{\left(\frac{\Delta L}{L}\right)^2 + k\left(\frac{\Delta W}{W}\right)^2 + \left(1.2\frac{\Delta T_{Si}}{T_{Si}}\right)^2 + \left(\frac{\Delta Tox}{5 \cdot Tox}\right)^2} \tag{2.10}$$

Where $A_{\Delta I}$ is the ratio of current mismatch.

Chapter 3

Integrated Inductors

3.1 Introduction

The inductor is a key component in high RF frequency circuits. In the past a few years there was a great drive to improve the quality factor of integrated inductors so that a radio-on-chip system can be readily realized [13]. Bulk silicon inductors generally have peak Q's of less than 10 with low self-resonant frequencies [14]. These values are typically not satisfactory for high performance, voltage-controlled oscillator (VCO) designed to meet the stringent phase noise and low power constraints.

In this chapter, the inductor structure and layout were discussed first. Then the inductor model and model parameters extraction methods were presented. Finally, the model simulation results were compared with the measurement for some typical inductor and the conclusion was drawn.

3.2 Structure and Layout

High quality factor integrated circular spiral inductors were fabricated in SPAWAR Systems Center's novel 0.5 μm TSOI CMOS technology with a stacked 1.7 μm-thick aluminum metal. The geometry of the spiral inductors can be described by the following parameters: number of turns (n), turn width (w), turn spacing (s), inner diameter (d) or inner to outer radius ratio ($IDOD$). These parameters are shown in Figure

3.1(a). The die photo is shown in Figure 3.1(b). The width of the spiral metal is from 15 um to 50 um. The inner-to-outer diameter ratio is from 0.3 to 0.7. And the number of turns is from 1.5 to 10.5. Figure 3.2 shows a cross-section of an integrated inductor fabricated in this technology. The test frame with ground-signal-ground pad was laid out for shielding.

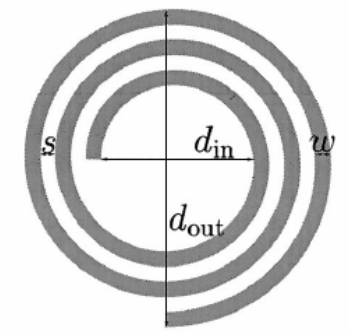
The inductors we investigated can be grouped in the following classes:

1) Same *IDOD*, but different *n* and *w*;

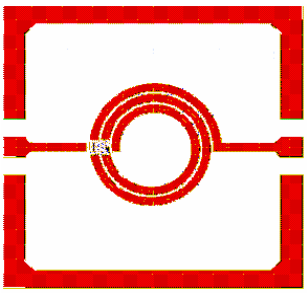
2) Same *w*, but different *IDOD* and *n*;

3) Same *n*, but different *IDOD* and *w*.

All the inductors have a fixed spacing between the turns, s = 3 μm. In this case, the inner radius (R_i) can be derived analytically from the parameters set (*n*, *w*, *IDOD)*, R_i=*IDOD*n*(w+s)/(1-IDOD).* Three families of inductors were characterized by s-parameter measurement with HP 8720D network analyzer and Cascade Microtech coplanar ground-signal-ground (GSG) probes. De-embedding was carried out to remove the parasitic components.



(a)



(b)

Figure 3.1 (a) Structural parameters of an on-chip spiral inductor, (b) Die photograph of the spiral inductor.

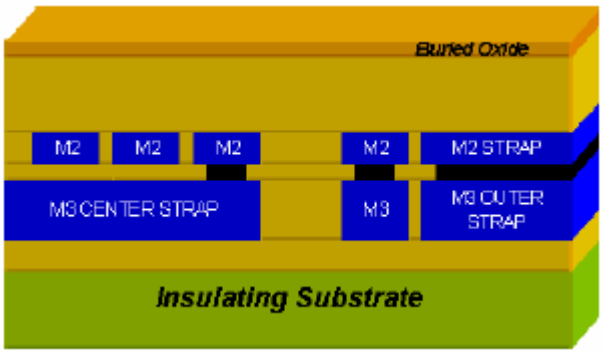
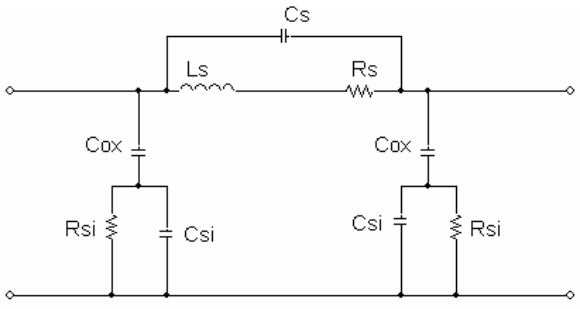
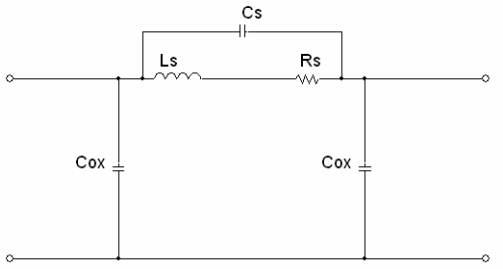


Figure 3.2 Cross-section of inductor.

3.3 Inductor Model and Parameter-extraction Method



(a)



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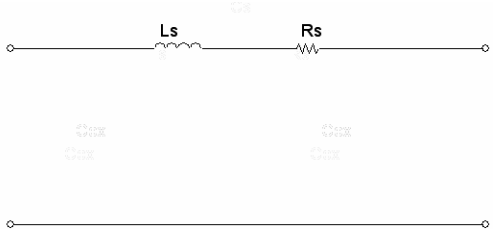


(c)

Figure 3.3 Equivalent circuit for models: (a) with substrate, (b) without substrate, (c) equivalent circuit at low frequency.

The equivalent circuit for the inductor is shown in Figure 3.3, where Ls is the inductance and Rs is the parasitic series resistance of the metal wire. The overlap between the spiral and the underpass allows direct capacitive coupling between the two terminals of the inductor. This path is modeled by the series capacitance Cs. In a conventional inductor structure, the oxide capacitance between the inductor and the silicon substrate has to be taken into account, as well as the sub-circuit of the substrate, which are shown in Figure 3.3(a). However, including these parasitic circuit elements makes the extraction of the important intrinsic inductor parameters very tricky and inaccurate. In order to improve the inductor performance the silicon substrate has been etched away. As a result, the self resonance frequency and quality factor Q of the inductor increase. The resulting circuit model can be simplified to the one shown in Figure 3.3(b). The meaning of C_{ox} in this circuit is no longer the capacitance between the

inductor and the substrate; instead, it models the remaining parasitic capacitive coupling between the inductor and the surrounding grounded structures. At low frequency, 100MHz, both the coupling capacitor Cs and the parasitic capacitor C_{ox} can be neglected, thus the circuit model is further reduced to the one in Figure 3.3(c). For this series RL circuit, the two components can be easily extracted from the Y-parameter:

$$Ls = -\frac{1}{\omega}\mathrm{Im}\left(\frac{1}{Y_{21}}\right) \tag{3.1}$$

$$Rs = -\mathrm{Re}\left(\frac{1}{Y_{21}}\right) \tag{3.2}$$

However, as the Y-parameters cannot be measured accurately, they are obtained by the transformation from the measured s-parameters. The overall capacitance can found from the self-resonance frequency:

$$C = \frac{1}{\omega_0^2 Ls} \tag{3.3}$$

where C includes C_{ox} and C_s.

All parameters (L, R and C) in the inductor model are functions of the number of turns (*n*), the turn width (*w*), the turn spacing (*s*), and one from the following: the outer diameter d_{out}, the inner diameter d_{in}, the average diameter d_{avg} = 0.5*(d_{in}+d_{out}), or the inner and outer diameter ratio (*IDOD*). By fitting the data, expressions for Ls, Rs and Cs were determined. We have successfully obtained these parameters for inductors in a broad range: the number of turns from 1.5 to 5.5, turn width from 15 um to 50 um, and inner and outer diameter ratio from 0.1 to 0.7.

Due to large amount of data collected, computer software was employed to find the dependence on the geometric parameters. However the selected software (Origin 7) can only fit two independent variables, therefore, the following three approach was used:

a) Ls = *f* (w, n), while IDOD is fixed,

b) Ls = *f* (n, IDOD), while *w* is fixed.

c) Ls = *f* (IDOD, w), while *n* is fixed,

As the approach c) is not practical, the approaches a) and b) were adopted.

3.4 Results and Model Verification

3.4.1 Series Inductance (Ls)

The empiric expression of the series inductance is based on the data fitting technique in reference [15]. For fix *IDOD,* the expression is

$$Ls = P_1 n^{P_2} w^{P_3} \tag{3.4a}$$

Taking the logarithm of Eq. (4a) we can get the following monomial relation:

$$\log Ls = \log P_1 + P_2 \log n + P_3 \log w \tag{3.4b}$$

For the inductors with IDOD = 0.5, the fitted the parameters are found: $P_1 = 0.26591$, $P_2 = 2.21235$ and $P_3 = 0.72121$. Therefore, the inductance can be modeled as:

$$Ls = 0.26591 n^{2.21235} w^{0.72121} \tag{3.4c}$$

In a same way, the inductor model can be fitted following the approach b). As an example, inductors with $w = 25$ can be modeled as:

$$Ls = 1.07185 n^{1.54863} IDOD^{0.51154} \tag{3.5}$$

3.4.2 Series Resistance (Rs)

The series resistance of the inductor can be expressed as [16]:

$$R_s = \frac{\rho_r l}{w \cdot t_{eff}} \tag{3.6}$$

where ρ_r is the resistivity of the metal; l is the overall length of spiral, which equals $n\pi d_{avg}$; w is the line width; t_{eff} is the effective thickness. With the consideration of the skin effect, the effective thickness can be calculated as $t_{eff} = \delta \cdot (1 - e^{-t/\delta})$; where t is the physical thickness of the metal and δ is the skin depth. At 1 GHz, the skin depth of Al and Cu is 2.8 um and 2.5 um, respectively.

3.4.3 Series Capacitance (Cs)

The Series capacitance Cs models the parasitic capacitance coupling between the inductor and the under-path. It can be approximated as a parallel-plate capacitor [17].

$$C_s = nw^2 \frac{k \cdot \varepsilon_{ox}}{t_{M2-M3}} \tag{3.7}$$

Where t_{M2-M3} is the oxide thickness between spiral and the under path, which is 0.9 um in our sample; $k = 0.7$ is a fitting parameter.

3.4.4 Model Verification

With the method described above, the parameters of the series resistance, inductance and capacitance can be extracted; the results from two samples are shown in Table 1.

The measured and simulated S-parameters have been compared in Figure 3.4 and Figure 3.5, where the numbers of turns are 2.5 and 4.5, respectively. The measured inductances as the function of frequency are plotted in Figure 3.4(b) and Figure 3.5(b).

The total error [18] between the measured and the simulated s-parameter calculated as follows by (3.8) is less than 3% over the frequency range from 0.1 to 10 GHz.

$$\varepsilon_{tot}(S) = 100 \cdot \frac{1}{4} \cdot \sum_{ij} \left\{ \sum_{freq} \frac{\left| measS_{ij} - simS_{ij} \right|^2}{\left| measS_{ij} \right|^2} \right\} \frac{1}{N_{freq}} \tag{3.8}$$

The simulation is carried out with ADS. We also compared the results from inductors with other structural parameters, they consistently have good agreement.

Table 3.1 Extracted circuit model parameters.

Turn	w (μm)	IDOD	Ls(nH)	Rs (Ω)	Cs(fF)
2.5	25	0.5	2.8	0.13	41.48
4.5	25	0.5	12	0.36	75

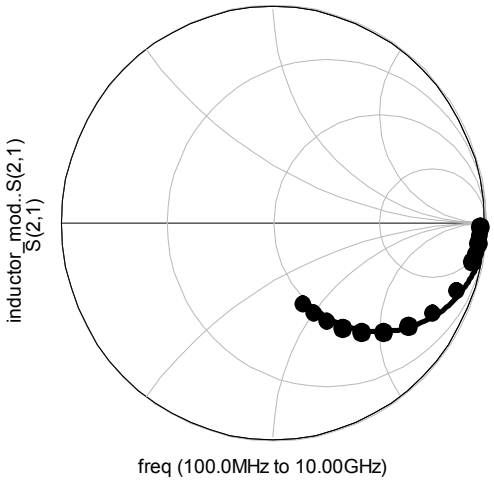


Figure 3.4 (a) Measured (dot) and simulated (line) s-parameter, n=2.5, *w*=25um, s=3um, and *IDOD*=0.5.

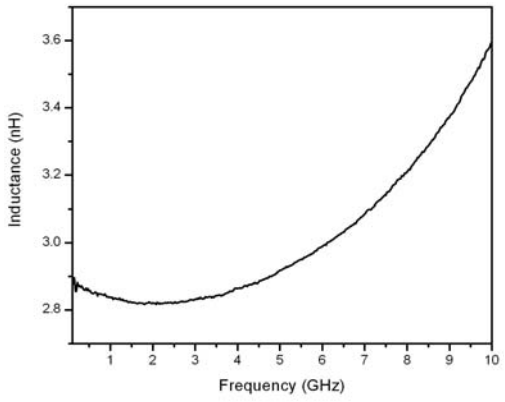


Figure 3.4 (b) Measured inductance as a function of frequency. n=2.5, *w*=25um, *s*=3um, and *IDOD*=0.5.

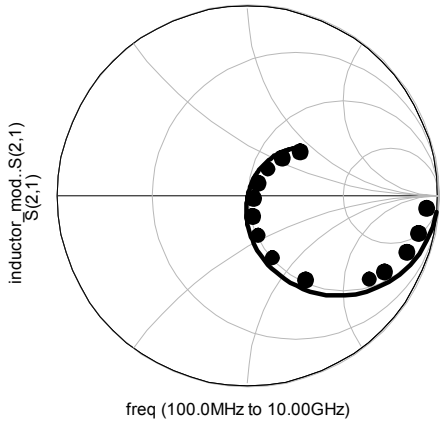


Figure 3.5 (a) Measured (dot) and simulated (line) s-parameter, n=4.5, *w*=25um, *s*=3um, and *IDOD*=0.5.

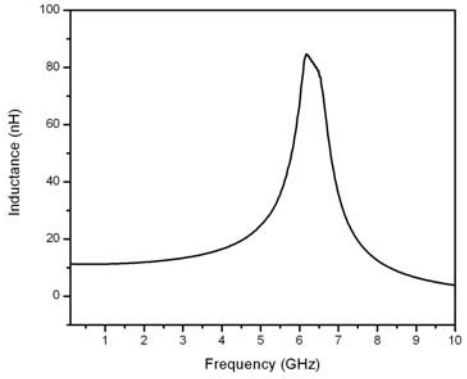


Figure 3.5 (b) Measured inductance as a function of frequency. n=4.5, *w*=25um, *s*=3um, and *IDOD*=0.5.

A typical fit of the Verilog-A model vs. the measurement data for two inductor instances is shown in Figure 3.6. Figure 3.6 shows that a 6.5 nH inductor has a peak Q of 18, which is higher than the best Q of 15 reported in [19] for a 5.5 nH inductor in a silicon-on-sapphire (SOS) technology with a thicker 2.5µm aluminum metal. The 6.5 nH inductor has a self-resonant frequency at about 10 GHz, which is about twice the self-resonant frequency reported in [19].

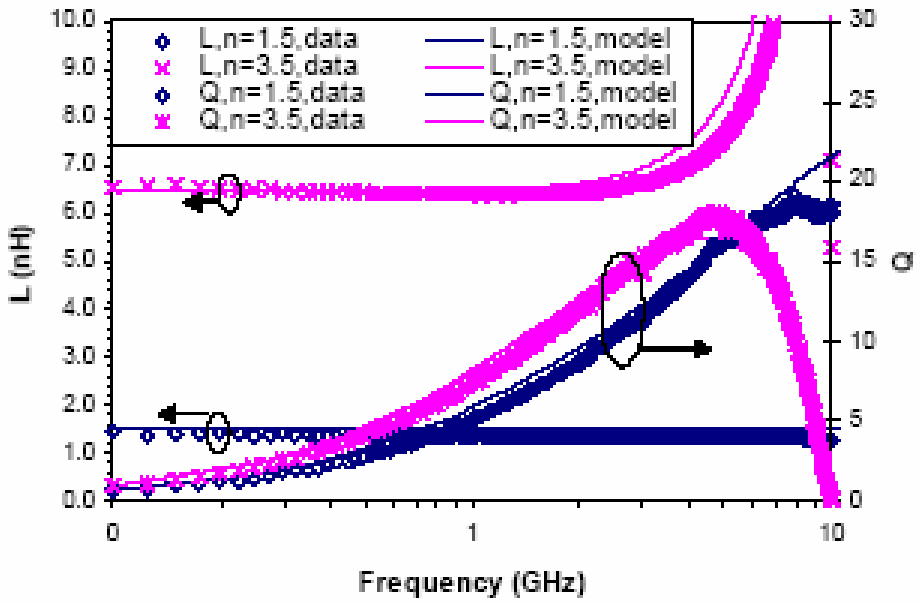


Figure 3.6 Comparison between measurement data and model simulation.

We also find the model developed is accurate for inductors with the number of turns less than 5.5, fortunately most practical on-chip spiral inductors fall in this range. When the number of turns is larger than 5.5, the error becomes larger and more circuit elements must to be included in the model. As shown in Figure 3.7, the model can not predict the behavior for frequency higher than 7 GHz.

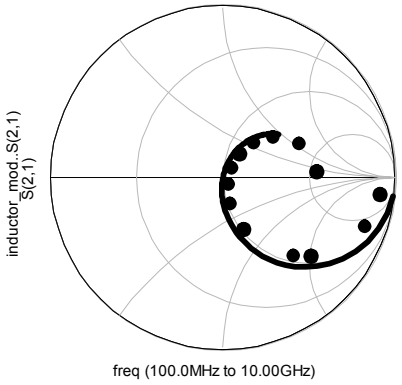


Figure 3.7 Measured (dot) and simulated (line) s-parameter, n=5.5, *w*=25um, *s*=3um, and *IDOD*=0.5.

3.5 Conclusion

Based on the above analysis, we found that small IDOD ratio inductors were turn-restricted. For example, if *IDOD* equals to 0.1and 0.2, n should be maintained less than 2, and 3 respectively. Generally I*DOD*s of 0.4 to 0.5, *w* of 15 um to 30 um and *s* of 3 provide a better model fit. The obtained equivalent Spice circuit model shows good agreement between the simulated and measured s-parameters over a wide frequency range.

Chapter 4

Integrated Varactor

4.1 Introduction

Integrated voltage-controlled capacitors (varactors) are widely used as frequency tuning elements for RF applications [20, [21], such as voltage controlled oscillators (VCOs). The core of a VCO is the LC tank circuit, composed of a varactor and an inductor.

Several RF models for the MOS varactor have been reported [21, [22, [23, [24]. The physical model proposed in [21] was derived by considering the device structure but consisted of separate models for different operating regions of the device, i.e. in accumulation and in depletion, respectively. The theoretical model reported in [22] includes the physics-based equations. The SPICE compatible models exploiting a sub-circuit based on the BSIM3v3 model were presented in [23] and [24].

This chapter presents a RF model of an accumulation-mode MOS varactor with a high capacitance tuning range in a multi-finger layout, and it is based on physical parameters. The model describes the voltage dependent capacitances and resistances along with the parasitic inductance, capacitance and resistance terms. A single topology with the lumped elements derived from the device has been proposed for easy integration into common circuit simulator as well as direct linkage to a p-cell. Good agreements between measured data and simulation results were obtain in the frequency range of 0.1 to 25 GHz by de-embedding the test frame inductance.

4.2 Structure and Layout

Accumulation-mode MOS varactors were fabricated in SPAWAR Systems Center's Integrated Circuit Fabrication Facility in their 0.5 um CMOS-SOI technology where the substrate has been removed. This process has low parasitic capacitance which facilitates fabricating high quality, high frequency RF varactors by decreasing the losses normally associated with bulk silicon processes. The varactors designed, fabricated and tested employ a multi-fingered layout with finger lengths of 0.5 um, 0.8 um, and 1.0 um, finger widths of 5 um and 10 um, and total widths of 1000 um. A representative cross-section of the device is shown in Figure 4.1 with a micrograph for a typical layout shown in Figure 4.2.

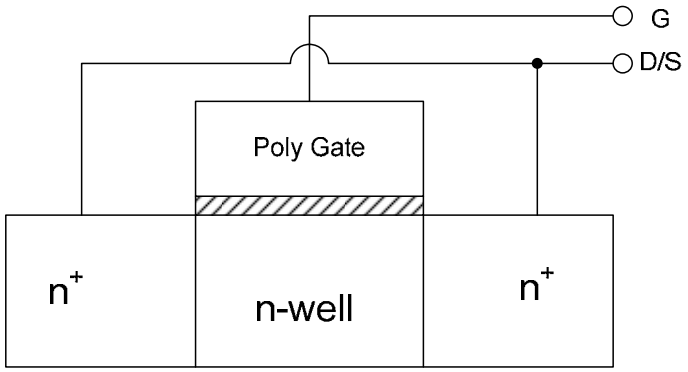


Figure 4.1 The cross-section of the single varactor.

Measurements confirm that the varactors have a tuning ratio that varies from 1.7 for the 0.5 um device to 2.6 for the 1.0 um device. The worst case self-resonant frequency of 21.5 GHz was observed for the W = $200\times5\mu m$, L = 1.0 um device at its maximum capacitance of about 2.13 pF at 500 MHz, as shown in Figure 4.3(a). As observed in

Figure 4.3(b), the quality factor remains satisfactory (above 8) up to 12.8 GHz. These figures are significant compared to other varactors which have been created recently [23].

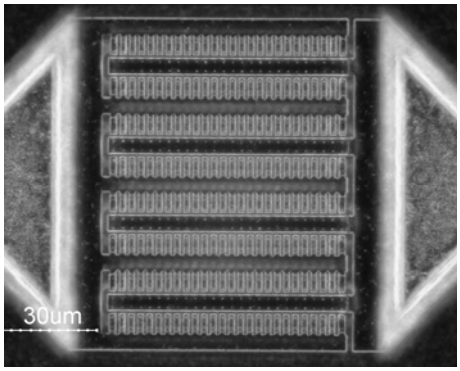
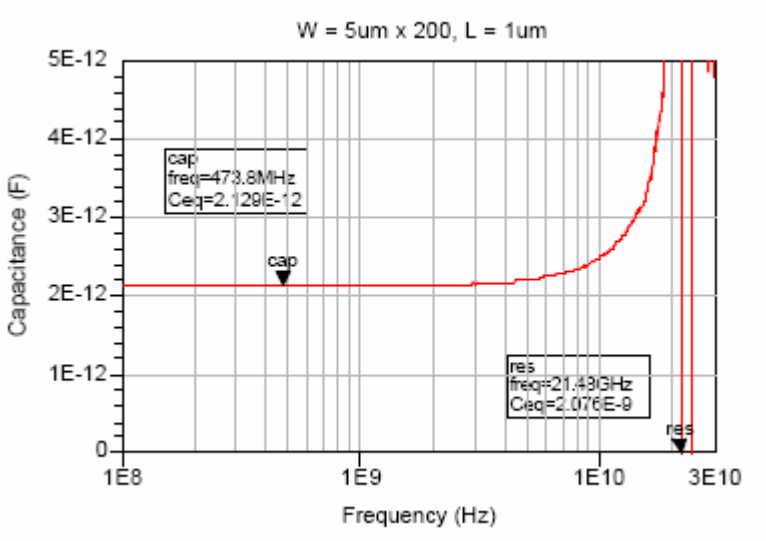
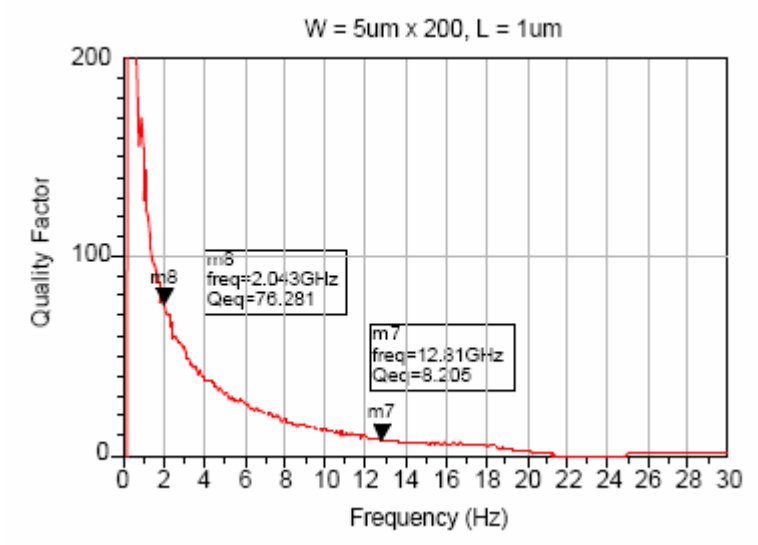


Figure 4.2 The micrograph of the varactor under test.



(a)



(b)

Figure 4.3 (a) Capacitance versus frequency and (b) quality factor versus frequency.

4.3 Model Parameter Extraction and Model Verification

To verify and parameterize the proposed equivalent circuit show in Figure 4.4, the fabricated accumulation-mode MOS varactors were laid out and extracted. Direct parameter extraction was performed with Y-parameter analysis based on S-parameter data using an HP8720D network analyzer. Cs was extracted out at 1 GHz, with the Rs and L extracted at self-resonance. De-embedding was carried out to remove parasitics, which consisted primarily of an inductance term. Rm1 and Rg and Rs/dcnt (≈ 0) represent the metal1, the gate and gate contact resistance and source/drain contact resistance respectively. In order to model the gate bias dependence of C_{Var}', varactors capacitance per unit width was described as follows,

$$C_{Var}' = \frac{P_{1C}V_G}{1+P_{2C}|V_G|} + P_{3C} = C_f' + C_{avg}' + \frac{LC_{ox}V_G}{1+\beta|V_G|}. \quad (4.1)$$

Where

$P_{1C} = LC_{ox}$,

$P_{2C} = \beta$, and

$P_{3C} = C_f' + C_{avg}'$.

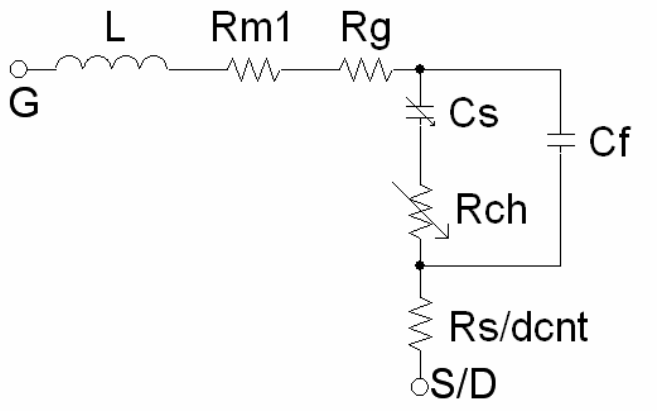


Figure 4.4 The equivalent varactor circuit.

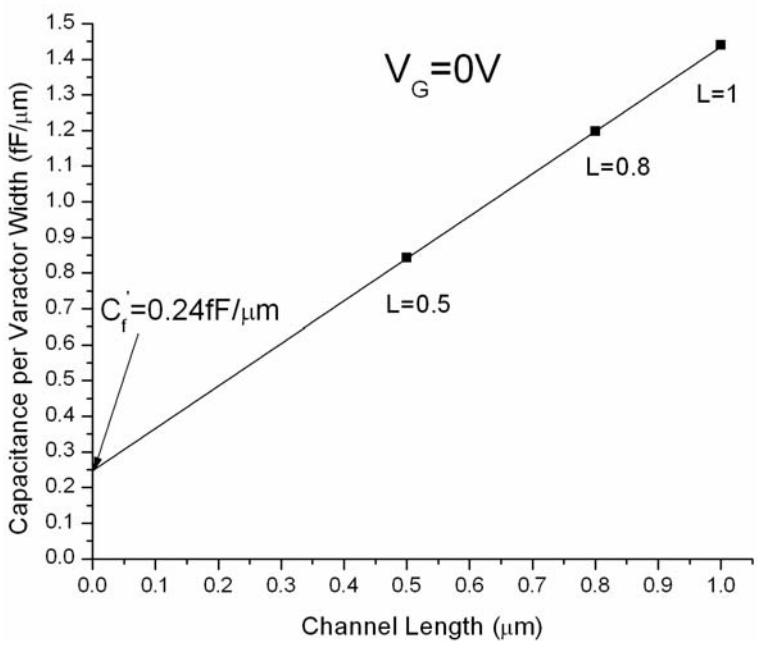


Figure 4.5 Capacitance versus length at V_G=0V.

The fringe capacitance per micrometer of varactor width, C_f', was obtained by plotting the varactor capacitance at V_G equal zero and extrapolating to find the fixed capacitance

term or the P_{3C} component of equation (1). All three test devices with gate lengths of 0.5 μm, 0.8 μm and 1 μm respectively, are plotted as shown in Figure 4.5. C_f' is found to equal 0.24 fF/μm.

Equation (4.1) is based on the data fitting and accurately describes the nonlinear characteristic of C_{Var} as a function of the varying gate bias, as shown in Figure 4.6. For the 5_200_p8 (finger width_finger number_gate length) varactor, P_{1C} =1.64 fF/μm, P_{2C} =2.99 V^{-1}, P_{3C} =1.23 fF/μm and for 5_200_1 varactor, P_{1C} =2.89 fF/μm P_{2C} =3.63 V^{-1}, P_{3C} =1.58 fF/μm. Using the P_{3C} data and C_f' from Fig 4.5. and solving for Cox_{Avg} and δL, respectively, result in Cox_{Avg} equal 1.765 fF/μm^2 and 0.117 μm or $L_{eff} = L - 0.234$ μm.

Varactor resistance consists of both a channel term and the gate poly term. The channel resistance is modeled as follows;

$$R_{ch} = R_s + R_{acc} // R_p \tag{4.2}$$

In (3.2), R_s is the gate bias independent or static resistance term of R_{ch}. R_{acc} represents the resistance of the accumulation layer formed in the channel region. R_p is the n-well resistance in parallel with R_{acc}.

$$R_{ch} = \begin{cases} 1/K_{acc}(V_G - dV_{G,ch}), if V_G > dV_{G,ch} \\ \infty, elsewhere \end{cases} \tag{4.3}$$

In (3.3), K_{acc} is a parametric coefficient that is related to the mobility of electrons in the accumulation layer, and $dV_{G,ch}$ is relevant to the flat-band voltage. As V_G decreases below the flat-band voltage, R_{acc} can be considered as being infinite and R_{ch} approaches a constant value of $R_s + R_p$. When V_G increases above the flat-band voltage, R_{acc} dominates R_{ch}. As a result, R_{ch} decrease, finally approaching a constant value of R_s, as shown in Figure 4.6.

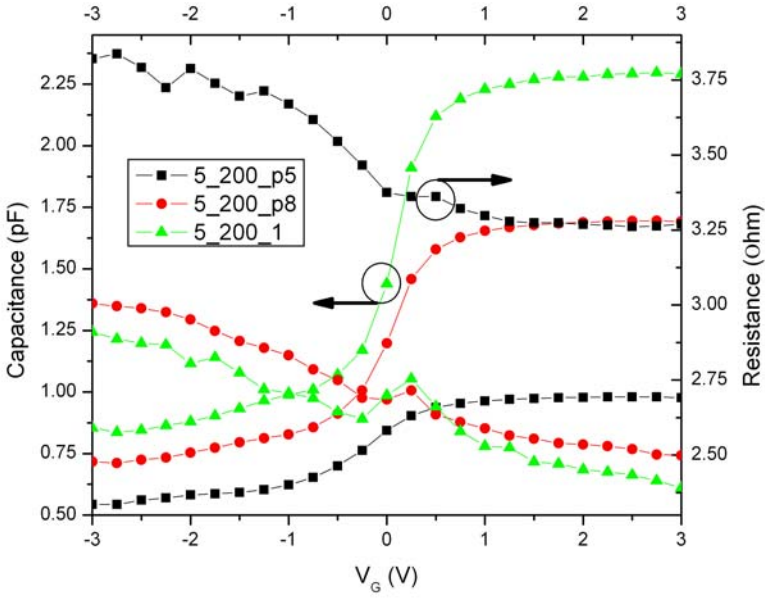


Figure 4.6 Capacitance and Resistance change verse gate bias voltage as extracted from the varactor parametrics.

Similarly, a data fitting equation is used to describe the voltage dependence of resistance:

$$R_s = \frac{P_{1R} V_G}{1 + P_{2R}|V_G|} + P_{3R}, \tag{4.4}$$

From the extracted resistance data for the 5_200_p8 varactor; P_{1R} = -0.138 V^{-1} P_{2R} = 0.191 V^{-1}, P_{3R} = 2.72 Ω and for the 5-200-1 varactor; P_{1R} = -0.0805 V^{-1}, P_{2R} = -0.0354 V^{-1}, P_{3R} = 2.65Ω.

The extracted parameter values for the series resistance and inductance are summarized in Table I for V_G =0 V.

Table 4.1 Extracted parameter values for 200 finger (W_f = 5um) varactors for L equal 1 um and 0.8 um respectively.

	L(pH)	Rm1(Ohm)	Rg(Ohm)	Cf(pF)	Cs(pF)	Rch(ohm)
5_200_0.8	35	0.05	0.078	0.24	0.958	0.658

5_200_1	35	0.05	0.0625	0.24	1.20	0.6415

Figure 4.7 and 4.8 compare the measured and simulated S-parameters at $V_G = 0$ V for the devices of Table 4.1. Note, the methods for determining L, R_{m1}, and R_g are presented in section 4. The total error between the measured and the simulated S-parameter with the proposed equivalent circuit was calculated to be in less than 1% over the frequency range from 1 to 25 GHz. Figure 4.9 shows measured and simulated C-V characteristics for the L=0.8 μm and L=1 μm devices.

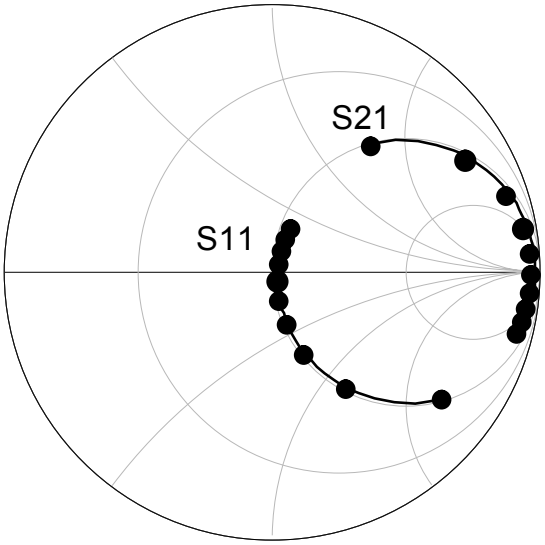


Figure 4.7 L=0.8um Vg=0V symbol is measured data and line is the simulated.

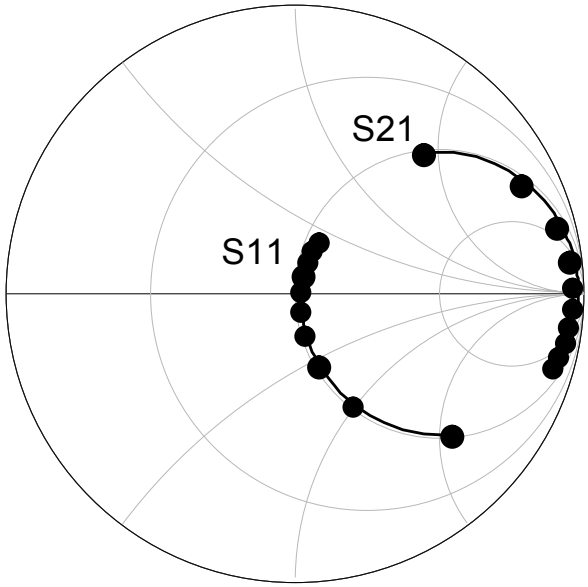


Figure 4.8 L=1um Vg=0V symbol is measured data and line is the simulated.

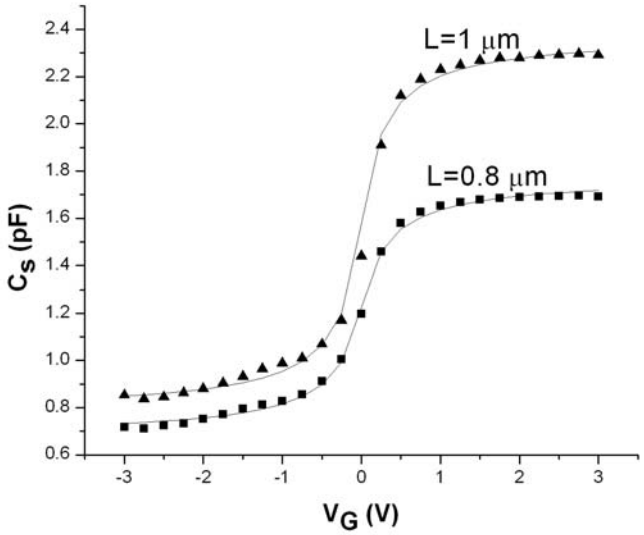


Figure 4.9 Comparison of the measured (symbol) and simulated (solid-line) C-V characteristics for the L=0.8um and L=1um devices.

4.4 Layout Summary and Usage

In the circuit design process the designer is given the option to select L in the range of 0.7 um to 1.1 um at fixed finger width W_f of 10 um**.** The designer selects the varactor channel length L and provides the desired value of C (V_G =0) for the varactor at

simulation/layout. The number of fingers n, along with the number of rows (r) and columns (c) will then be computed by the p-cell generator and modeled for simulation by the Verilog code. It is strongly suggested that all fingers be wired with 10 um wide or wider m1 line with at least two gate contacts per finger for reliability. The p-cell and Verilog-A model are restricted to W_f=10 um and m1 interconnects that are 10 um in width.

4.4.1 Capacitance Calculation and Length choice

The total capacitance of a varactor is modeled as the sum of a strongly bias dependent intrinsic capacitance (C_{int}) component and a weakly bias dependent fringe capacitance (C_f). The latter is equal to 0.24 fF/um.

a. L was selected such that L approached being LCox >> C_f. Note this includes CGDO. The minimum L has been selected to be greater than 0.8um.

b. W_f was selected such that Rg << R_{ch} . The gate resistance is propotional to W_f but channel resistance is inversely proportional to W_f. Proper W_f choice will reduce the gate resistance. Thus, it can reduce the gate resistance noise.

c. $W_{Total} \approx C_{Avg}/(LCox + C_f')$. Where C_{Avg} is the average or zero bias value of the varactor capacitance and approximately equal:

$$C_{Avg} \approx W_{Total}(L-2\delta L)\, Cox_{Avg}\, /2 \tag{4.5}$$

At V_G equal to 0 V the zero bias value of the capacitance equals:

$$C_{Var}\,(V_G=0) \approx W_T(L-2\delta L)\, Cox_{Avg}\, /2 + C_f'\, W_T. \tag{4.6}$$

Additionally,

$$C_{Min} \approx WC_f' \tag{4.7}$$

$$C_{Max} \approx WLCox_{Max} + WC_{fringe}' \quad (4.8)$$

The varactor with longer channel (L=1 um) provides a greater dynamic capacitance range with a reduced Q_{eff}, while a shorter channel length varactor (L=0.8 um) provides a higher Q_{eff} with a reduced dynamic capacitance range.

a. n_f the number of fingers equals W_T/W_f.

b. For a square varactor layout

i. $c\,(L + 1.6um) = r\,(Wf+12um)$ (4.9)

ii. $c \times r = n$ fingers (4.10)

iii. $$r = \sqrt{n\frac{L+1.6um}{(W_f+12um)}} \quad (4.11)$$

where $$n = \frac{C_{Avg}}{W_f(L \cdot Cox + C_{fringe}')}$$

then $c = n/r$ where the row value is rounded to the nearest integer and the column value solved for.

4.4.2 Resistance Estimation

The metal1, gate and contact resistance can be written as:

$$R_{m1} = \frac{\left[c(L+1.6um)/10um\right]Rshm1}{Round((r)/2)} + \frac{\left[c(L+1.6um)/10um\right]Rshm1}{Round((r)/2)+1} \quad (4.12)$$

where R_{m1} = 50 mohms.

$$R_g = \frac{W_f}{L} \cdot \frac{Rshpoly}{3n} \quad (4.13)$$

For L =1 μm, W_f = 5 μm, and n = 200, it is approximately equal to 20 mΩ. Where Rshpoly = 2.5 Ω.

$$R_{S/Dcnt} = \frac{Rm1Is}{n \cdot 2} \approx 0 \tag{4.14}$$

Where Rm1Is = 5 ohms.

4.4.3 Inductance Estimation

With the interconnect wiring set by the square feature of the varactor the inductance is better controlled and better estimated. The basic unit of inductance is estimated as follows:

$$Lp = \frac{2 \cdot 10^{-7} l}{Round(c/2)}\left[\ln\frac{2l}{w_{m1}} - 0.75\right] + \frac{2 \cdot 10^{-7} l}{Round(c/2+1)}\left[\ln\frac{2l}{w_{m1}} - 0.75\right] \tag{4.15}$$

where w_{m1} is set to 10 μm and l equal r(L+1.6 μm). This is an approximation. Due to the lack of separation between the fingers for W_f equal 5 or 10 μm it will have limited value above 5 to 10 GHz. Note the center-to-center m1 separation of the gate m1 and S/D m1 will be W_f +10 μm (m1) +2 μm (recommended m1 separation) in the p-cell.

4.5 Conclusion

In summary an equivalent RF model of an accumulation-mode MOS varactor with high capacitance tuning range in a multi-finger layout is constructed, which is composed of the following physical parameters:

1. C_f ' the total equivalent per um fringe capacitance – 0.24 fF/μm.
2. Cox_{Avg} the equivalent oxide sheet capacitance - 1.765 fF/μm^2.

3. δL the channel foreshortening distance - 0.117 μm or $L_{eff} = L - 0.234$ μm.

These parameters along with the fitting equations (4.1) and (4.4) and their coefficients can reliably be used to model the varactor capacitance, C_{Var}' and its voltage controlled channel resistance R_{ch}. Finally, the inductance and gate resistance parasitics are modeled by equations (4.12) through (4.14). The varactor model is valid for finger widths of 10 μm and lengths from 0.7 to 1.2 μm where the total width is not expected to exceed 2000 μm or 200 fingers. The accompanying p-cell and Verilog-A model are restricted to finger widths of 10 μm and m1 interconnection width of 10 μm.

Chapter 5

FinFET transistors and Modeling

5.1 Introduction

As the microelectronic industry is fast approaching the limit of bulk CMOS scaling, there are extensive research activities on advanced CMOS structures to extend CMOS scaling to less than 100 nm gate length. The FinFET is an innovative design of MOSFET, which is built on an SOI structure. The body of the transistor is etched into "fin"-like structure, which is wrapped by the gate on both sides. The double gate (DG) MOSFET is a popular choice, because this structure is scalable and the short channel effects can be suppressed for a given equivalent gate oxide thickness .

As shown in Figure 5.1, several rectangular multi-gated structures have been proposed recently, such as FinFET [25], tri-gate [26], Omega-gate [27], pi-gate [28], etc. The FinFET has emerged as the most popular device because of its ease of babrication with the well-understood bulk-MOSFET process.

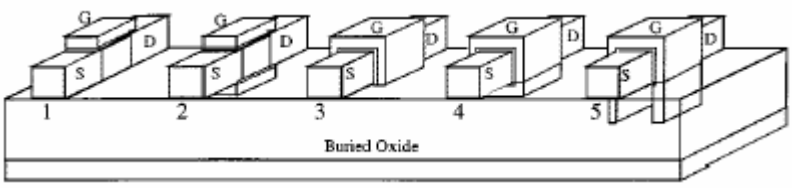


Figure 5.1 Different gate configurations for SOI devices: 1) single gate; 2) double gate; 3) triple gate; 4) quadruple gate (or: GAA structure); 5) Pi-gate MOSFET. [28]

The key challenges in the fabrication of double-gate devices are (a) self-alignment of the two gates, and (b) formation of an ultra-thin silicon film. Figure 5.2 shows the different orientations possible for a double-gate device. Several self-aligned planar devices have been proposed [29], however, the process is usually complex and the contact to the bottom gate is very challenging. Devices with ultra-thin film are generally considered incompatible with traditional processes. The FinFET is derived from the vertical MOSFET by reducing its height and converting it into a quasi-planar device.

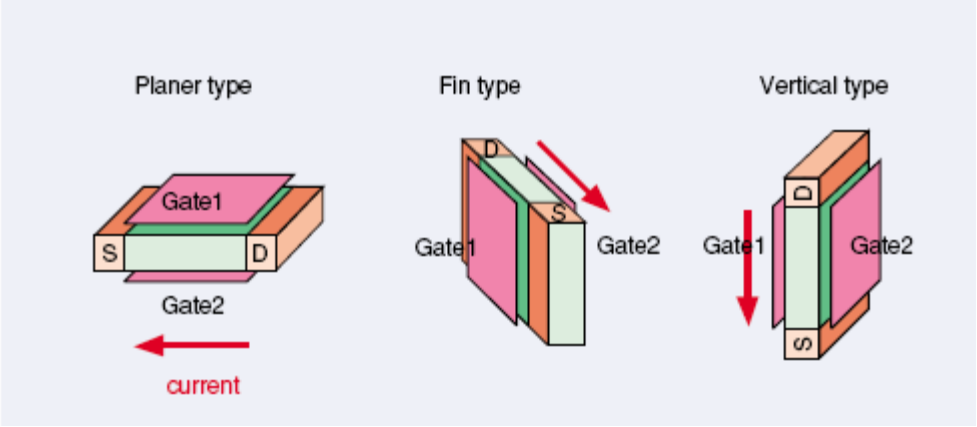


Figure 5.2 The possible Double-gate MOSFET orientations on silicon [29].

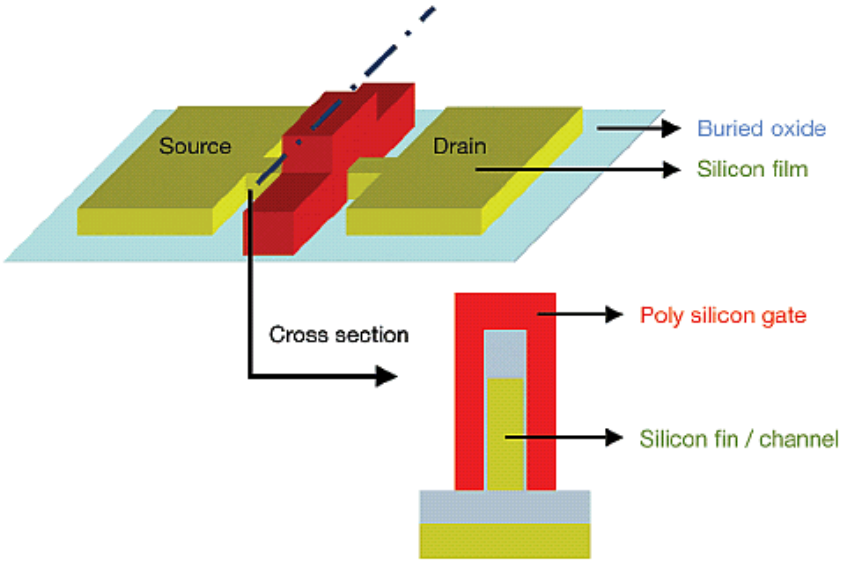


Figure 5.3 The 3-D FinFET.

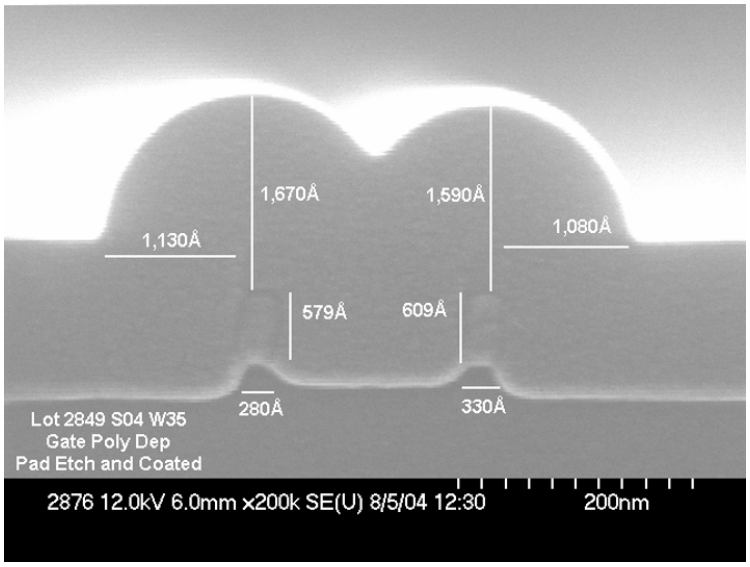


Figure 5.4 Scanning electron microscope picture of the cross section of FinFET (compliments of SPAWAR SC San Diego).

Figure 5.4 depicts the geometry of the FinEFT. The fin is a narrow channel of silicon patterned on an SOI wafer. The gate wraps around the fin on three faces. The top insulator (nitride) is usually thicker than the side insulator (oxide), hence the device has effictively two channels. The thickness of the fin represents the body thickness (T_{si}) of the double-gate structure, while its hight (H_{fin}) represents the channel width.

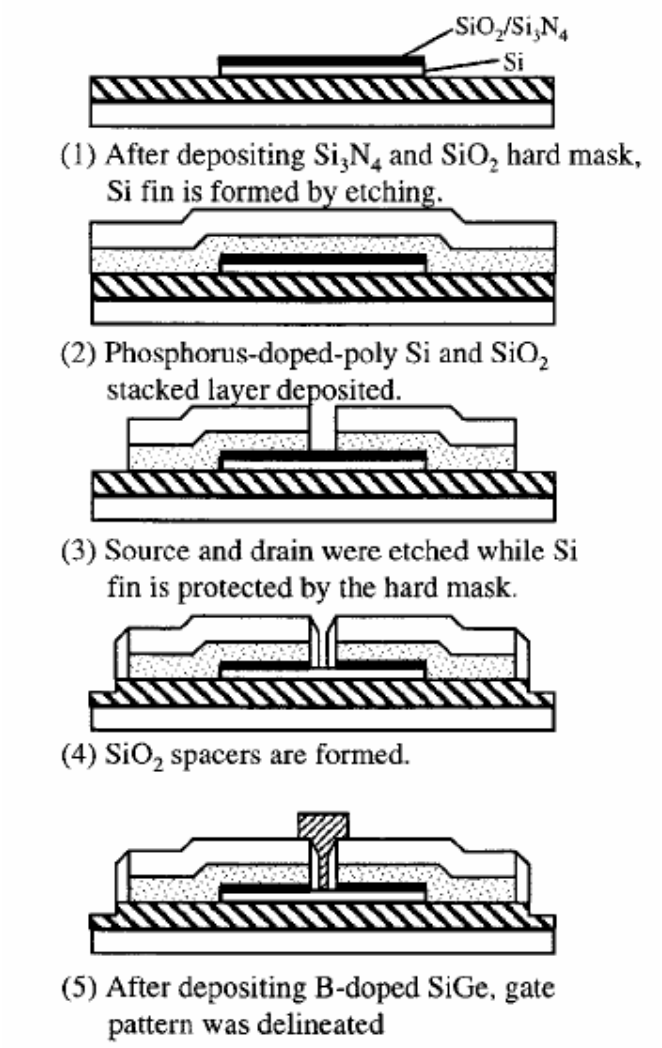


Figure 5.5 FinFET Process steps; from [25]

Figure 5.5 shows the basic process-steps involved in the fabrication of the FinFET. Since it was first proposed [25], refinements have been reported consistently [30, [31].

5.2 Performance of FinFET Transistors

The FinFET transistors were fabricated using SOI deep sub-micro (DSM) technology at SPAWAR system center, San Diego. There were two wafers made using the same mask. For the first run there are only four dies working on the whole wafer and

most measurements were made with these transistors there. For the second run the finger yield is low. Although transistors seemed to be working but their drain current much is less than expected. Some measurements were also made on this wafer. The discussion is that follows is an attempted to explain the problem.

5.2.1 DC Measurements

HP4155A semiconductor analyzer was used to make the DC measurement. Figures 5.6 to Figure 5.9 show FinFET (10 um width, 56 nm length) I-V characteristics.

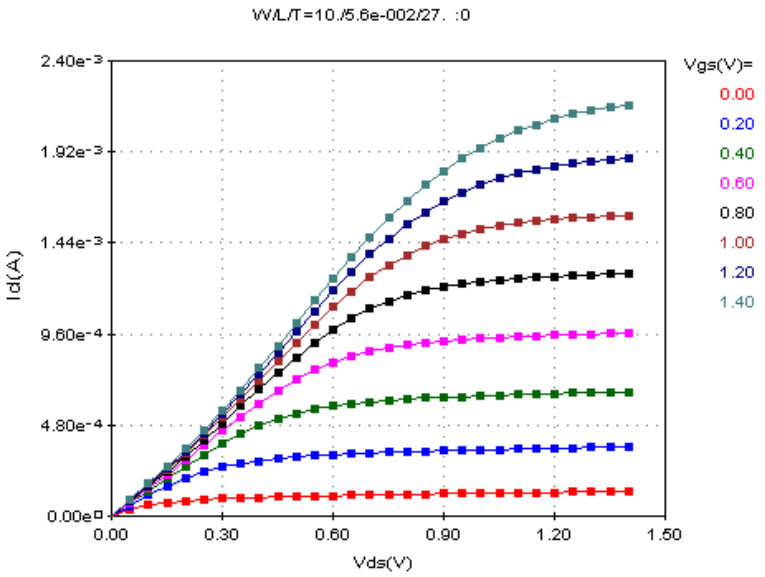


Figure 5.6 FinFET drain current versus drain voltage at various gate voltages.

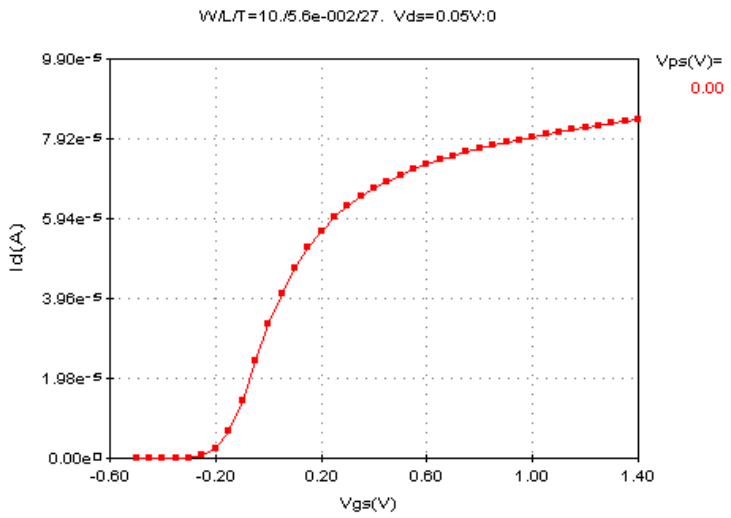


Figure 5.7 FinFET drain current versus gate voltage with drain voltage equal 50mV.

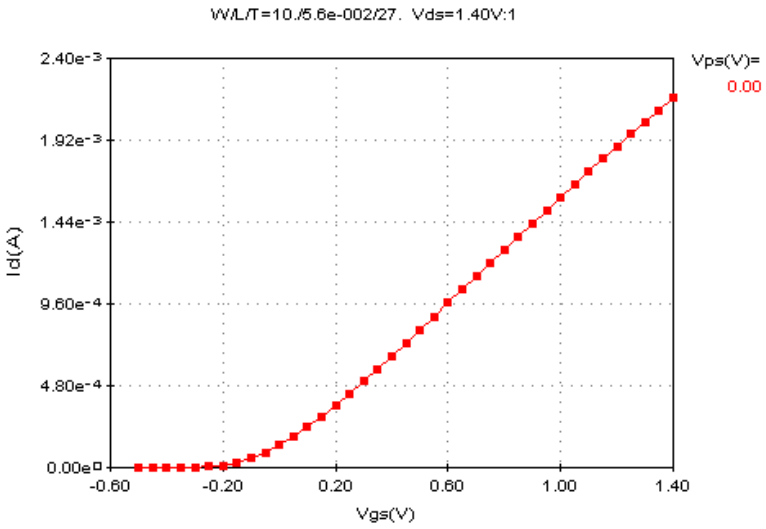


Figure 5.8 FinFET drain current versus gate voltage with drain voltage equal 1.4V.

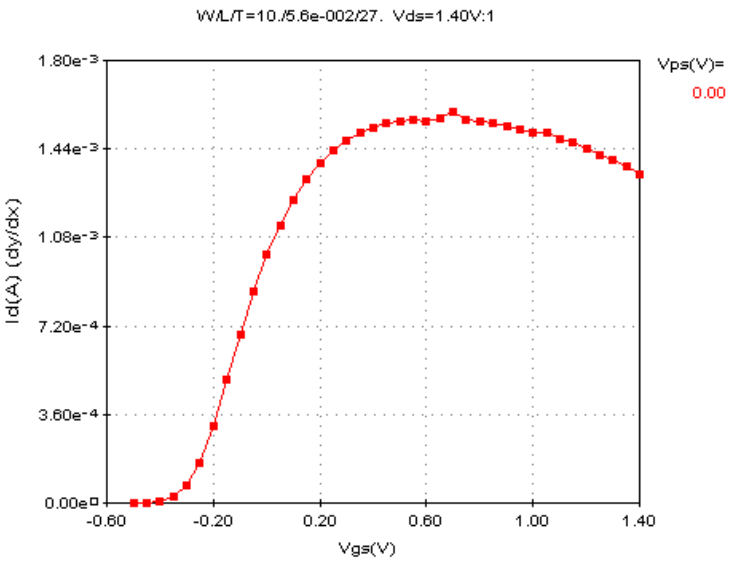


Figure 5.9 FinFET g_m versus gate voltage with drain voltage equal 1.4V.

In saturation, the ideal drain current has a square-law dependence on the gate-to-source voltage for long channel devices. But from the drain current curves shown in Figure 5.6 we find that it has a linear relationship with the gate voltage. This occurs as a result of velocity saturation.

The high-field effects become prominent at moderate drain voltage with continued device scaling. The primary high-field effect is velocity saturation. In silicon, as the electric field approaches about 4×10^6 V/m, the electron drift velocity shows a weak dependence on the field strength and eventually saturates at a value of about 10^5 m/s. For an 80 nm gate length device, velocity saturation begins to kick in at 320 mV. With the gate voltage above threshold voltage and drain-to-source voltage above 320 mV the device enters velocity saturation region.

In the velocity saturation the drain current can be rewritten as

$$I_D = \frac{\mu_n C_{ox}}{2}\left(V_{GS} - V_t\right)E_{sat} \tag{5.1}$$

The values of all small-signal parameters can change significantly in the presence of short-channel effects. The limiting transconductance of short-channel MOS device in velocity saturation,

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} \approx \frac{\mu_n C_{ox}}{2} W E_{sat} \tag{5.2}$$

Figure 5.7 indicates the threshold voltage of the FinFET is around -0.1V. It is difficult to design RF and analog circuits with negative threshold voltage device. Molybdenum gate technology has been applied to modify the threshold voltage of FinFET transistors, and it was successfully adjusted to 0.4 V [32].

Figure 5.10 shows FinFET drain current versus gate voltage at different drain voltages. The subthreshold slope is about 80mV/dec for drain voltage equal 50mV, and n is 1.33.

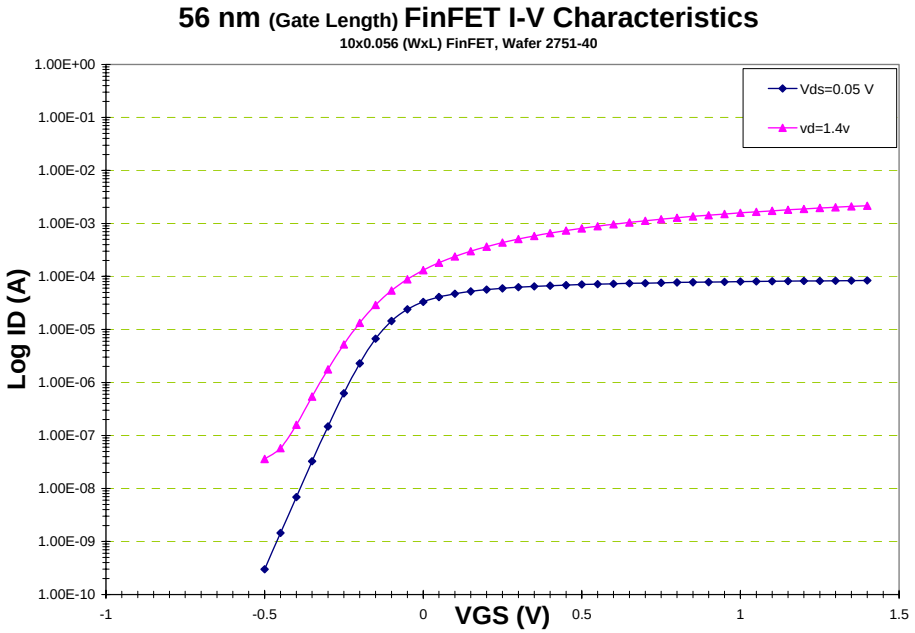


Figure 5.10 FinFET drain current versus gate voltage at various drain voltages.

5.2.2 AC Measurement

HP8720D network analyzer was used to make S-parameter measurement on FinFET transistor (W=72um, L=80nm). The $f_{\max}$ was extracted when the power gain equal to unity, that is $|S_{21}|^2 = 1$, as shown in Figure 5.11. Convert S-parameters to H-parameter. The f_T can be extracted at $h_{21} = 1$.

With the transistor working in velocity saturation region ($\Delta V \approx 0.7V$, V_t=-0.1V, V_{DS}=1.2V), $f_{\max}$ of FinFET is approximately 100 GHz, as shown in Figure 11; And f_T is approximately 42 GHz, as shown in Figure 12.

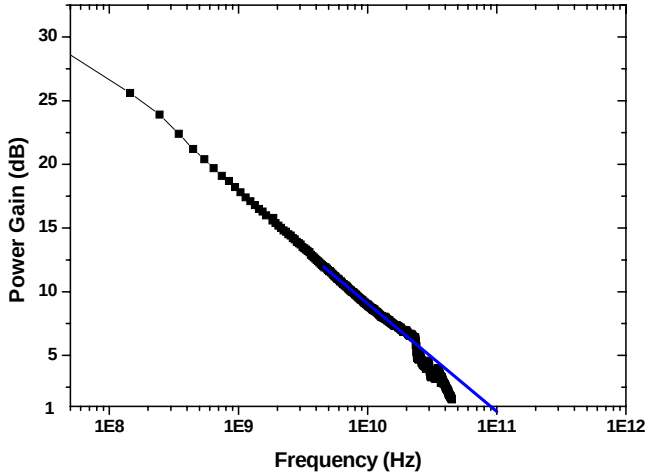


Figure 5.11 FinFET transistor power gain versus frequency ($\Delta V \approx 0.7V$, V_{DS}=1.2V).

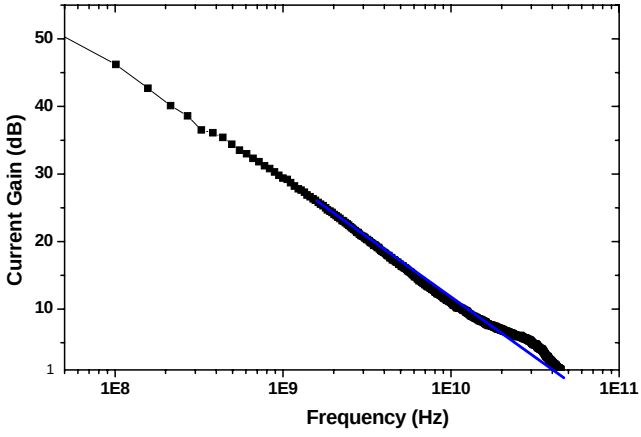


Figure 5.12 FinFET transistor current gain versus frequency ($\Delta V \approx 0.7V$, V_{DS}=1.2V).

With the transistor working in moderate inversion region ($\Delta V \approx 50mV$, V_t=-0.1V, V_{DS}=1.2V), f_t is approximately 20 GHz, as shown in Figure 5.13. An f_t of 20GHz is adequate to design low GHz applications when transistor works in moderate inversion region.

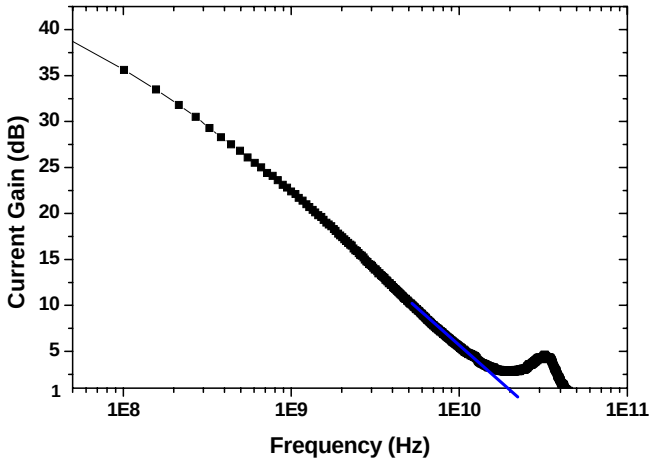


Figure 5.13 FinFET transistor current gain versus frequency ($\Delta V \approx 50mV$, V_{DS}=1.2V).

Since the FinFET with 80nm channel length works in velocity saturation region, the transition frequency, f_t can be rewritten as,

$$\omega_T \approx \frac{g_m}{C_{gs}} \approx \frac{\frac{1}{2}(\mu_n C_{ox})WE_{sat}}{\frac{2}{3}WLC_{ox}} = \frac{3}{4}\frac{\mu_n E_{sat}}{L} \tag{5.3}$$

In the velocity saturation region the transit frequency is inversely proportional to the channel length, which is different from that in the strong inversion region.

The maximum frequency of unit power gain can be rewritten as [33],

$$f_{Max} = \frac{f_T}{\sqrt{\left(R_g + 2R_S\right) \cdot gm \cdot \left(\frac{C_{fringe}}{C_{gs}}\right)}} \tag{5.4}$$

5.2.3 Noise Measurement

Figure 5.14 shows noise measurement made on FinFET transistor. It also demonstrated less low-frequency noise in moderate inversion than in the strong inversion [34]. It further supports FinFET use in moderate inversion operation in the design of RF circuits.

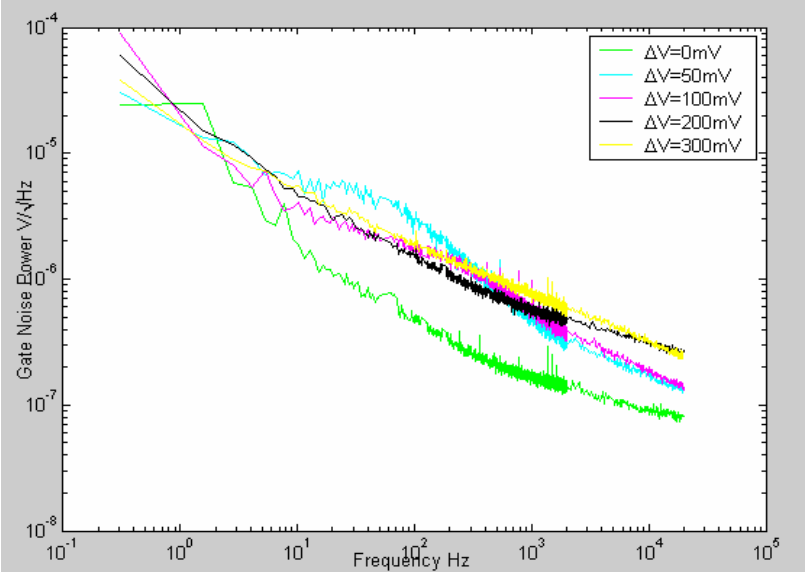


Figure 5.14 The low frequency noise of the FinFET for L=120nm, W=4.2um [9].

5.2.4 Capacitance Measurement

Measurements were performed on a Keithley 590 CV-meter and Keithley 4200 semiconductor characteristics analyzer. All measurements were performed in the dark chamber. For the equilibrium C-V measurement, the hold time and delay were set to 5 sec and 1.5 sec, respectively. The gate voltage sweep rate can be calculated as (bias range)/(total sweep time). The source and drain are shorted together, i.e. $V_d = V_s = 0$ V. Figure 5.15 shows the high frequency gate-to-channel capacitance (*hf*-C_{gc}) curve of an n-

channel FinFET. The *hf*-C_{gc} reaches its maximum value when the channel is in strong inversion and exhibits a minimum with reverse gate bias.

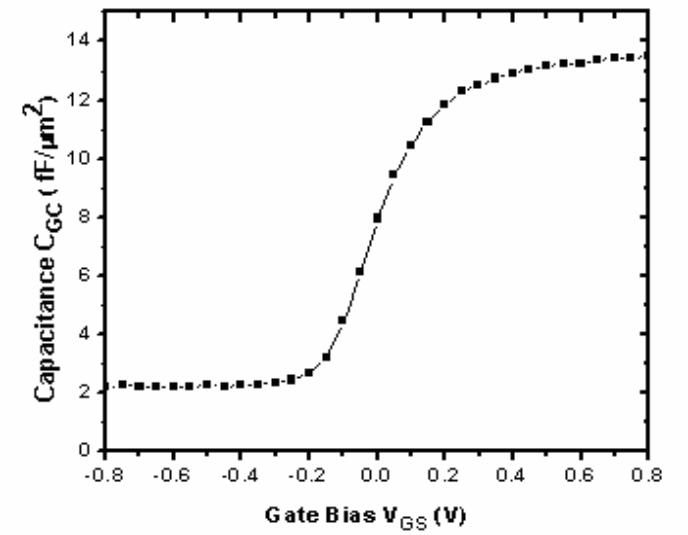


Figure 5.15 Equilibrium high frequency *C-V* curve.

The C-V measurement is a valuable diagnostic tool to characterize MOSFET. Therefore, if the influence of gate depletion capacitance can be neglected, the measured maximum gate-channel capacitance is equal to oxide capacitance. The extracted oxide thickness found is 2.4 nm, which is different from the designed 2 nm thickness [35].

5.3 FinFET Model

5.3.1 FinFET Small-Signal Model

The framework for generic physics based double-gate MOSEFT modeling has been recently reported [36]. However, to our best knowledge there is no FinFET small-signal model describes its behavior in GHz region. The FinFET structure investigated is depicted in Figure 5.16, where key geometry parameters are defined. The fabricated

transistor is shown in Figure 5.17. Based on the measurement results from this device, we developed a high frequency small signal-model.

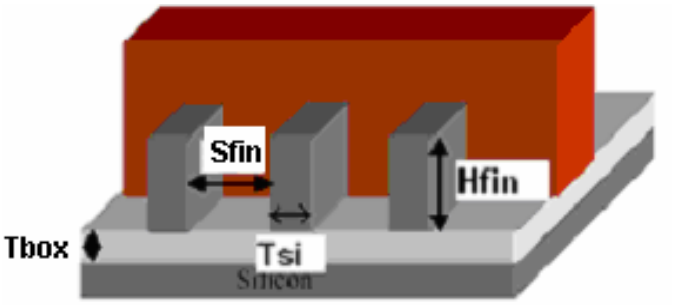


Figure 5.16 The 3-D FinFET. T_{box}=400nm, H_{fin}=50nm, T_{si}=20 nm.

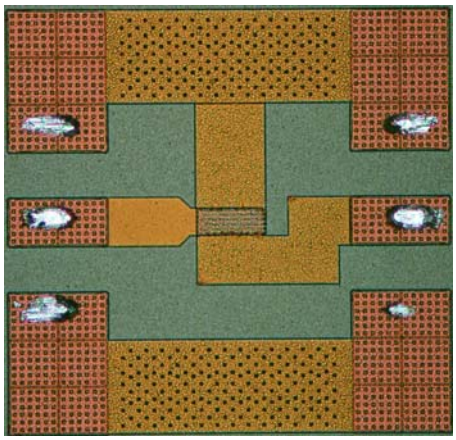


Figure 5.17 Die picture of the circuit with test frame.

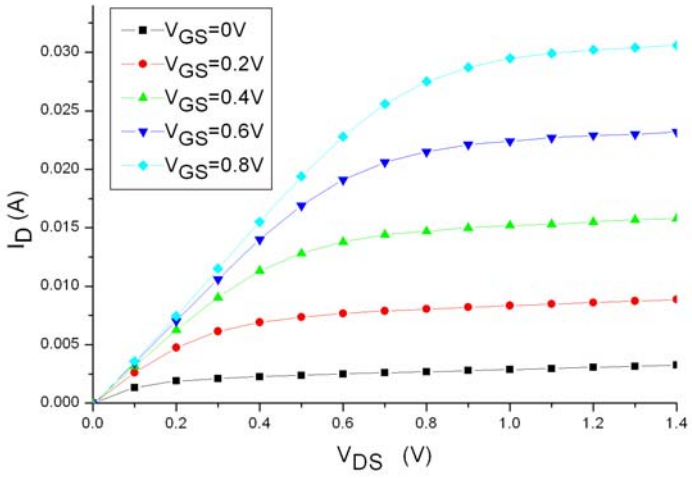


Figure 5.18 FinFET transistor characteristics (W=72 um, L=80 nm).

The FinFETs were fabricated at SPAWAR system center, San Diego. The gates of the FinFET were e-beam written at Berkeley with a range of 50 to 200 nm, and the overall gate width is 72 um. There are 720 fins in this transistor, and the gate width ($2H_{fin}$) for each fin is 100 nm. The DC I_D-V_{DS} curves are shown in Figure 5.18. The S-parameters were measured with an Agilent 8510 Network Analyzer and Cascade RF-1 probe station using GSG probes. The data was collected from 45 MHz to 10 GHz.

The equivalent circuit shown in Figure 5.19 is based on a quasi-static approximation, which is found to be adequate in the GHz range if the extrinsic components are properly modeled [37]. This model includes the complete intrinsic quasi-static MOS model, the series parasitic impedance of the gate, source and drain, as well as a substrate coupling network. The extrinsic part includes the parasitic series resistors R_g, R_d and R_s, and the parasitic series inductors L_g, L_d and L_s. The intrinsic model is composed of the voltage-controlled current source, the output resistance and the gate to channel impedance, as well as the intrinsic capacitors C_{gs}, C_{gd} and C_{ds}.

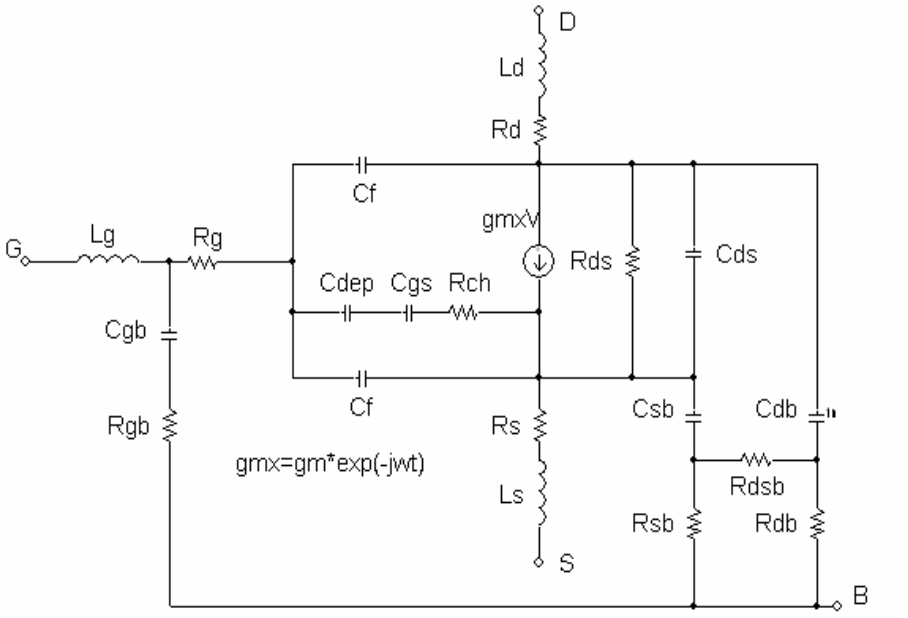


Figure 5.19 The FinFET small-signal equivalent model.

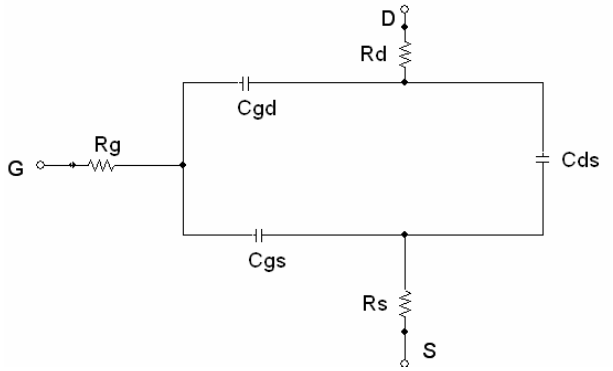


Figure 5.20 Zero bias small-signal equivalent model.

The parasitic resistance is extracted at low frequency with the device biased at V_{GS}=V_{DS}=0V. Under this bias condition the contribution from the intrinsic circuit vanishes except the three capacitors between the intrinsic nodes. In addition, in the low frequency region the parasitic inductors and the substrate coupling can be neglected. The schematic of the zero bias equivalent circuit at low frequency is shown in Figure 5.20, from which the parasitic resistors can be extracted by the Z-matrix components:

$$\mathrm{Re}(Z_{11}) = R_g + R_s \tag{5.5}$$

$$\mathrm{Re}(Z_{22}) = R_d + R_s \tag{5.6}$$

$$\mathrm{Re}(Z_{12}) = \mathrm{Re}(Z_{21}) = R_s \tag{5.7}$$

After the parasitic resistors have been extracted, the parasitic inductors can be modeled separately by means of the transmission line equations [38].

With the knowledge of the parasitic resistance and inductance, the intrinsic model can be determined. First, the S-parameters measured at low frequency and under the bias condition of Vgs=0.6V and Vds=1.2V are converted to the Z-parameters. Next the parasitic resistance terms are deducted, which is shown in Equation (5.8)-(5.11), in this way the intrinsic Z-parameters are obtained. In the intrinsic model most of the

components are in shunt connection to the internal source node, so the Z-parameters are converted to the Y-parameters, and then the circuit elements in the intrinsic model have been extracted. The circuit elements in the substrate network are fitted with the high frequency measurement results from inductor model extraction [39]. In Table 5.1 we list the extracted model parameters.

$$Z_{11}^{'} = Z_{11} - (R_g + R_s) \tag{5.8}$$

$$Z_{22}^{'} = Z_{22} - (R_d + R_s) \tag{5.9}$$

$$Z_{12}^{'} = Z_{12} - R_s \tag{5.10}$$

$$Z_{21}^{'} = Z_{21} - R_s \tag{5.11}$$

$$Z^{'} \rightarrow Y^{'} \tag{5.12}$$

Table 5.1 Extracted Model Parameters

Lg(pH)	Rg(Ω)	Rd(Ω)	Ld(pH)	Rs(Ω)	Ls(pH)
100	4.6	10	50	10	50
Cf(fF)	Cdep(pF)	Cgs(fF)	Rch(Ω)	gm(S)	t (ps)
66	1	300	10	0.1	5
Rds(Ω)	Cds(fF)	Cgb(fF)	Rgb(Ω)	Csb(fF)	Rsb(Ω)
450	260	5.6	110	11.2	60
Cdb(fF)	Rdb(Ω)	Rdsb(Ω)			
11.2	60	98			

Figure 5.21 and 5.22 show the comparison between the measured data and the simulation result from the extracted model. The discrepancy is within 5%, which is calculated from the following equation:

$$Error = \frac{100}{n}\sum_{i=1}^{2}\sum_{j=1}^{2}\left[\frac{\left|\mathrm{Re}(S_{ij}^{'}) - \mathrm{Re}(S_{ij})\right| + \left|\mathrm{Im}(S_{ij}^{'}) - \mathrm{Im}(S_{ij})\right|}{\left|S_{ij}\right|}\right]^2 \tag{5.13}$$

In summary, we developed a RF small signal model of FinFET from the extracted data, and good agreement between the model and the measurement is achieved up to 10 GHz.

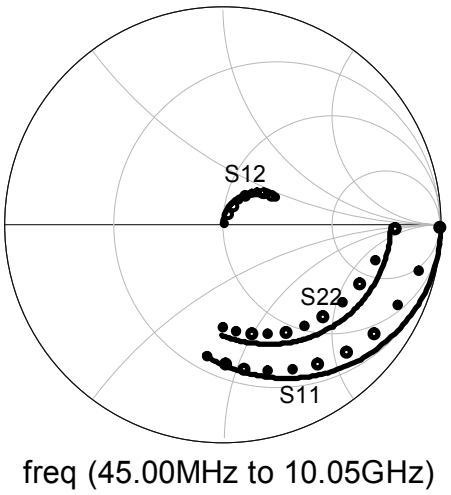


Figure 5.21 Measured (dot) and modeled (line) S-parameters (Vgs=0.6V, Vds=1.2V).

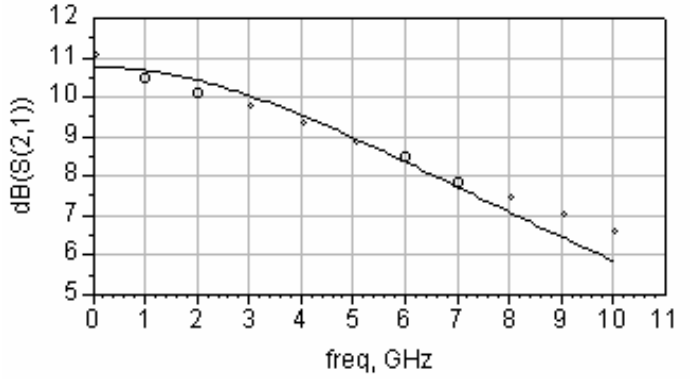


Figure 5.22 Measured (dashed) and modeled (solid line) S_{21} (Vgs=0.6V, Vds=1.2V).

5.3.2 FinFET BSIMSOI Model

FinFET BSIMSOI Model was extracted by using Utmost, a Silvaco package [40]. A Semiconductor Analyzer (HP4155A) was used to measure the I-V curve. Then the DC parameters were extracted by using DC routines in Utmost. A Capacitance-Voltage meter (Keithley CV590) was used to measure all capacitance and network analyzer (HP8720D) was utilized to do S-parameter measurement. Through AC routines in Utmost, AC and capacitance parameters have been extracted. In addition high temperature and noise measurement were done by my lab mates. After all these measurement and data analysis were finished, a complete FinFET BSIMSOI V3 model has been extracted. The detailed model parameters and simulation and measurement comparison are shown in Appendix B.

5.3.3 FinFET Model Summary

Both small-signal model and BSIMSOI model are presented in the previous sections. The small-signal model demonstrates the feasibility of FinFET operated in velocity saturation region. The BSIMSOI model supplies the opportunity to simulate the RF circuits working in moderate inversion with Cadence RF spectre tools. But the threshold voltage is approximately -0.1 V, which is not practical for RF circuits design. It is a fabrication process problem. But the FinFET fabrication process is still improved. For example, Molybdenum gate technology has been applied to modify the threshold voltage of FinFET transistors, and it was successfully adjusted to 0.4 V [32]. In this work it is reasonable to justify the threshold voltage to 0.5 V. The selected model parameters are shown in Table 5.1. This model will be used in the later chapters to simulate the RF

receiver circuits in moderate inversion. The Figure 5.23 compares the measured f_t to the modeled f_t curves in moderate inversion. The good agreement is found between the measurement and model simulated f_t curves.

Table 5.1 The modified FinFET BSIM3SOI model.

model NFIN b3soipd type=n		
+ tnom=27	version=3.1	tox=2.4e-9
+ tsi=2e-8	tbox=4.0e-7	xj=1e-8
+ nch=4.46e14	vth0=0.5	nlx=1.468104e-8
+ dvt0=2.5477237	dvt1=0.542419	dvt2=-1.416439e-4
+ u0=400	ua=2.35143e-10	ub=1e-18
+ uc=1.232366e-9	vsat=1e4	a0=1.0446036
+ ags=0.5742591	b0=1e-8	b1=-1e-7
+ lint=1.683313e-9	eta0=0.01	mobmod=1
+ capmod=2	cjswg=2e-10	cgdo=3e-10
+ cgso=3e-10	rsh=600	
+ nrd=50	nrs=50	

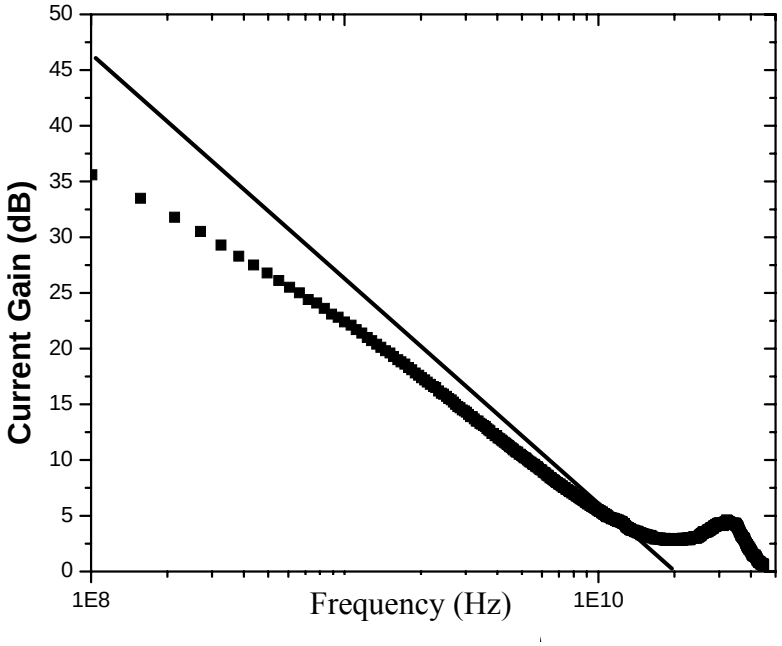


Figure 5.23 Measured (dot) and modeled (line) h_{21} ($\Delta V \approx 50mV$, Vds=1.2V).

5.4 Summary

Based on the above measurement data and analysis we found the FinFET transistor is a promising deep-sub micron device. The promising features of the FinFETs include high frequency, low supply voltage and low gate leakage current, making it an ideal candidate for the design of low power RF front-ends. It has excellent performance in both strong and moderate inversion regime. Specifically, its f_t is approxiamtely 20 GHz in moderate inversion regime, which makes it feasible to realize the ultra-low power RF receiver front-end. The only problem of current FinFET transistors is the negative threshold which makes it hard to be biased. The threshold voltage of FinFET transistor model is assumed to be modifiable to a positive value. For an instance, the VTH0 is set to 0.5 V for long channel device.

Chapter 6

GPS Receiver Design

6.1 Introduction

In Chapters 3 and 4 the passive devices, on-chip inductors and varactors, were modeled. They will be used in the following chapters to design the RF circuits for the GPS receiver. In Chapter 5 FinFET transistors were measured and characterized. It did have good performance. Especially, the f_T is around 20 GHZ at moderate inversion, which is enough to realize the circuits working below 2 GHz. The model developed was also valid for moderate inversion and it showed good agreement with the measurement. We will take advantage of the features of FinFET moderate inversion to realize the GPS receiver front-end circuits so that it can operate in ultra-low current.

As we know, the GPS is a satellite-based location/time finding system with 24 satellites orbiting the earth. It is a direct sequence spread spectrum (DSSS) functioning at two bands: L1 (1575.42 MHz) and L2 (1227.6 MHz) [41]. Most commercial GPS receivers use the L1 band only. The L1 band has two sets of codes, coarse-acquisition (C/A) and precision (P). The original 50 bit/s data is spread over a 2 MHz bandwidth (BW) for the C/A code, as shown in Figure 6.1.

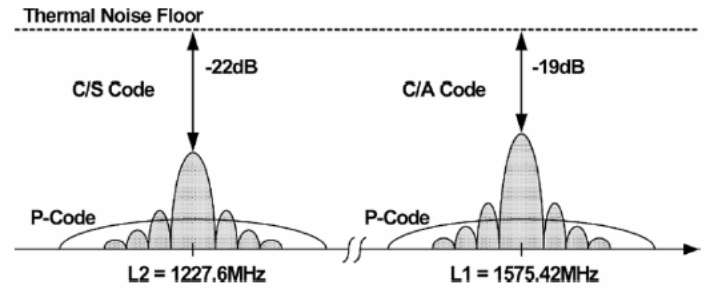


Figure 6.1 The GPS L1/L2 band signal spectrum [42].

At the antenna of a GPS receiver, the received signal power is typically -130 dBm. Since we are interested in the 2 MHz main lobe of the C/A code, the noise power is simply given by *kTBW*, which equal -111 dBm. Therefore, the received signal-to-noise ratio (SNR) at the antenna is around -19 dB. By despreading and integrating over a long time period, a receiver can exploit the inherent spread sprectrum processing gain of the navigation signals to get the proper postcorrelation signal-to-noise ratio (SNR).

6.2 GPS Receiver Architectures

6.2.1 Typical GPS Receiver Architectures

There are two architectures widely used in commercial GPS receivers today. The first is the dual-conversion architecture, which is used widely. In this architecture, the L1 band is translated to a moderate intermediate frequency (IF) of approximately 100-200 MHz where it is filtered by off-chip filter before a second downconversion to a lower IF of about 1-10 MHz. Finally, the signal is filtered again before being amplified to a detectable level, as shown in Figure 6.2.

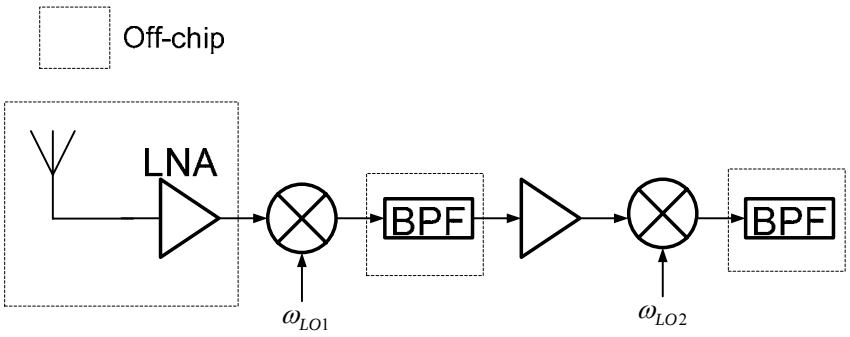


Figure 6.2 Dual-conversion GPS receiver.

The second is the single-conversion architecture, as shown in Figure 6.3. Here only one mixer is used. The L1 is directly sampled and then converted to baseband in a subsequent digital step.

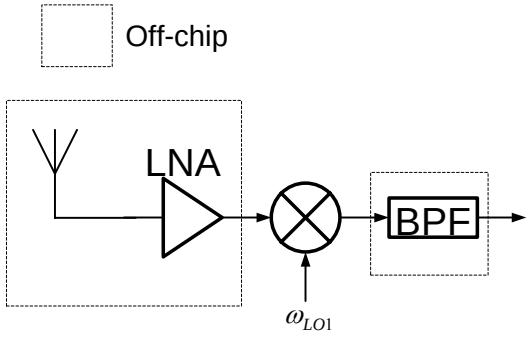


Figure 6.3 Single-conversion GPS receiver.

Both architectures have a common advantage. An off-chip LNA or active antenna is used, which gives the freedom to remotely place the antenna from the receiver itself. But they also have disadvantages. Either dual-downconversion or single-conversion architecture needs off-chip components which increase the power cost and foot print. In order to realize high integration and low power consumption, CMOS low-IF GPS receiver architecture has been presented next to minimize the usage of off-chip components and realize single-chip solution.

6.2.2 Low-IF Architecture

In general the low-IF receiver architecture is based on the replacement of the low-pass filters of a zero-IF receiver by a bandpass filter. The Low-IF receiver is insensitive to DC offsets and LO to RF crosstalk or feed through. But it suffers from the problem of limited image rejection due to the need for stringent matching of in-phase (I) and quadrature (Q) channel [43]. This limitation makes the low-IF approach unsuitable for many applications. However, when we examine the GPS signal spectrum, an opportunity emerges [44].

Figure 6.4 (a) shows a low-IF architecture with an IF of 2 MHz. The choice of 2 MHz low-IF results in an image frequency within the P-code 20 MHz bandwidth. Thermal noise dominates the 20 MHz P-code band. With an IF of 2 MHz, since the image frequency of C/A code lies in the P-code band, no other strong signals are present in this band, as shown in Figure 6.5. Thus, the receiver only need reject the noise of unwanted sideband. The required rejection is only about 15 dB, which is easily obtained with ordinary levels of component matching [45]. This consideration makes the low-IF architecture an attractive choice for highly integrated GPS receiver.

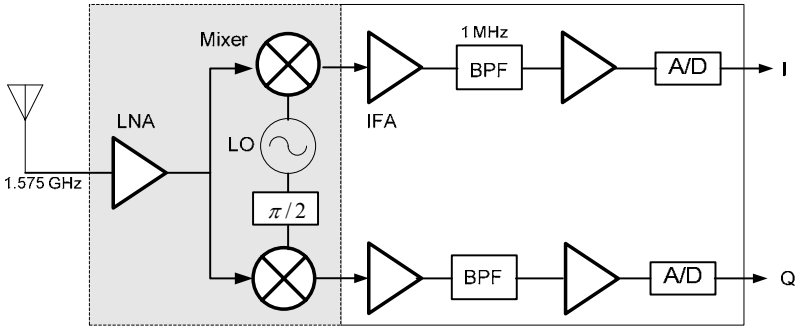


Figure 6.4 Block diagram of CMOS GPS receiver.

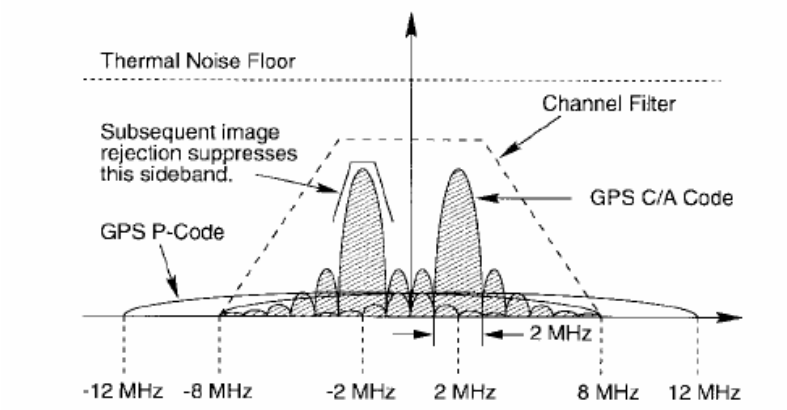


Figure 6.5 The GPS band signal spectrum after downconverted to 2 MHz IF [44].

The complete analog signal path is integrated, including the low noise amplifier (LNA), the mixer, I and Q local oscillator (LO) drivers, IF amplifier (IFA's), active filters, limiting amplifier (LA), and analog-to-digital (A/D) converters. Since most components are integrated, the power consumption can be reduced.

In general, lowing the frequency gives an immediate return on power saving. As was reported in Shaeffer's work [44], since the output intermediate frequency of mixer is around 2 MHz, most power is consumed before the IFA's. Over 60% of the power is consumed by the LNA, VCO and mixer. Therefore, in this work low power LNA, Mixer and LO designs were concentrated, as shown in the gray shaded area of Figure 6.4. The final objective is to design ultra-low power LNA, mixer and LO.

6.3 Receiver System Design

With the architecture of the GPS receiver determined, the receiver system planning is discussed next. The key point is to trade off the gain, noise figure (NF), and linearity properly among all circuits, such that every block can be implemented to satisfy low power requirement. Conventional RF system uses 50 Ω matching network at input

and output ports. However, in a low power RF receiver front-end with a single chip solution, except the first stage input impedance need to match antenna impedance, the following stages do not need to match 50 Ω or 75 Ω impedance, because it consumes large amount of current [6]. Such system is presented in Figure 6.7.

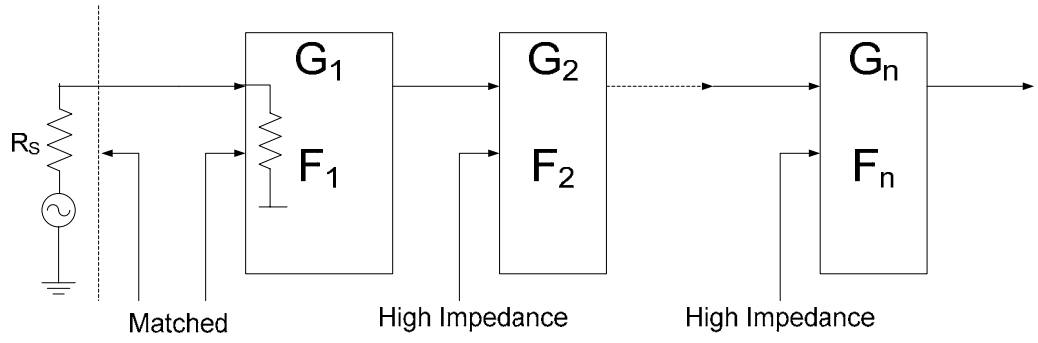


Figure 6.7 Cascaded stages of receiver system.

It can be shown that the inter-modulation grows and accumulates through the cascades, and could be described,

$$\frac{1}{IIP3_{cascade}} \cong \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \cdots \tag{6.1}$$

where $IIP3_n$ is the *IIP3* of the *n*-th stage and numeric value, G_n is the power gain of *n*-th stage.

As for the noise of a cascaded system, assuming the first input stage of the cascade is matching to a source impedance of R_S, and the following stages all have high input impedance and NF of each stage is calculated with respect to the source impedance driving that stage, the cascaded noise factor can be expressed as,

$$F_{cascade} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{\Pi_n^{N-1} G_n} \tag{6.2}$$

where G_n and F_n is the power gain and noise factor of *n*-th stage, respectively. Here, we assume that the individual stage's characterization can be directly used to derive the

overall system performance. Namely, the loading from subsequent stage will not alter the noise and gain performance of the previous stage. This is a reasonable assumption in this work since the inter-stage loadings are capacitive and can be treated as high impedance. It also can be found from the above equations, increasing the gain in early stages improves the total *NF*, but at the cost of worse *IIP3*. Since in this work there is no *IIP3* or *IIP2* problem we could try to pursue the gain of LNA as high as possible with low noise figure.

6.4 Receiver Implementation Requirements

To satisfy the stringent power requirement, it is necessary to properly specify and optimize the receiver specifications. Unlike other wireless communications systems, the GPS requirements were not well defined and specified in the literature until recently [42]. There are three noticeable differences between GPS and a conventional wireless standard. Firstly, GPS has only one RF channel in each band. Secondly, there is no strong in-band interferer as is common in a cellular system. All these differences offer a good opportunity to build a low-power GPS receiver. In the following section the receiver specifications are derived.

6.4.1 Noise Figure

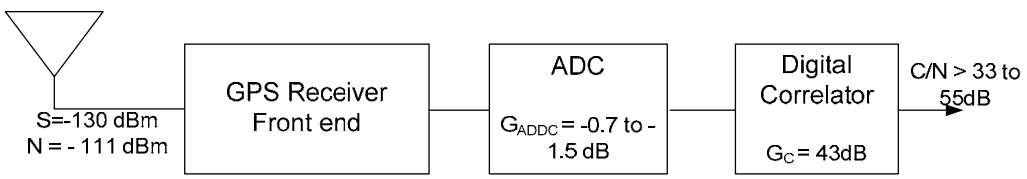


Figure 6.8 Block diagram of the GPS receiver.

In this work, a CMOS GPS receiver front-end is followed by an ADC and digital correlator, as shown in Figure 6.8. The purpose of a GPS receiver is to extract the accurate position and time information from the weak satellite signal. There also exist various source of position error. Some of the errors are from the satellite and propagation delay. The others are from the receiver impairments, such as noise. In order to account for the radio impairment, an important signal quality metric, the signal-to-noise ratio (SNR) will be reviewed next. However, the SNR of direct sequence spread spectrum (DSSS) scheme is function of the position in the receiver under consideration. The precorrelation SNRs are negative, whereas postcorrelation SNRs are positive. It is convenient to normalize the SNR to 1-Hz bandwidth. This achieves a ratio of signal and noise which is bandwidth-independent. It is referred to as the "carrier-to-noise density" ratio [46]. The carrier-to-noise density can be readily converted into SNR (S/N) or bit error rate (E_b/N_o),

$$\frac{C}{N_o} = \left(\frac{S}{N}\right) B = \left(\frac{E_b}{N_o}\right) R_b \tag{6.3}$$

where B is the bandwidth (in Hz) of that stage of receiver, R_b is a raw data rate of 50 b/s for L1 C/A band. This equation is converted into decibels

$$C/N_0\left[dB - Hz\right] = 10\log_{10}\left[\left(SNR\right)(B)\right] \tag{6.4}$$

From the above equation, it can be found that C/N_0 is a nominal figure. Received satellite signal power varies with user antenna gain, satellite elevation angle, and satellite age [47]. Typical C/N_o range from 35-55 dB-Hz.

Once the minimum required C/N_o is presented or processed by a digital correlator to maintain the wanted tracking or acquisition performance, the receiver sensitivity is uniquely determined by (6.5) without any confusion caused by the bandwidth ambiguity.

$$Sensitivity\left[dBm\right] = \left(\frac{C}{N_o}\right)_{\min}\left[dB-Hz\right] + N_o\left[\frac{dBm}{Hz}\right] + NF\left[dB\right] \tag{6.5a}$$

$$Sensitivity\left[dBm\right] = \left(\frac{C}{N_o}\right)_{\min}\left[dB-Hz\right] + N_o\left[\frac{dBm}{Hz}\right] + NF\left[dB\right] \tag{6.5b}$$

where N_o is the thermal noise power density at the antenna port which is equal to -174 dBm/Hz at typical room temperature and NF is the noise figure of the receiver. Assuming that a digital correlator requires a $(C/N_o)_{min}$ of 35 dB-Hz and the receiver sensitivity requires -133 dBm. Assuming a 2-bit ADC the NF can be calculated to be 6 dB from equation (6.5). This NF includes both receiver front end and A/D converter (ADC)'s NF. As we know, both single-bit and multi-bit ADC are currently used in GPS receiver. Most low-cost commercial receivers employ 1-bit sampling in narrow (i.e., 2 MHz) bandwidth. High-end receivers typically use anywhere from 1.5-bit (3 level) to 3-bit (8 level) sampling in bandwidth ranging from 2-20 MHz. Finite-bit quantization degrades the signal [48]. The degradations of different bit ADC are listed in Table 6.1.

Table 6.1 Signal degradation due to finite quantization in the ADC.

	1-bit ADC	2-bit ADC	3-bit ADC
Narrow IF bandwidth	3.5 dB	1.2 dB	0.7 dB

6.4.2 Phase Noise

In previous section the carrier-to-noise ratio (C/N_o) has been used as a figure of merit for the GPS receiver front-end performance. There are several factors degrading C/N_o, such as finite image rejection ratio (IMRR), phase noise, filter bandwidth and ADC bit resolution. Since in this work we only emphasize on LNA, VCO and mixer design, the effects from IMRR, filter bandwidth and ADC bit resolution are also not considered. The relationship between phase noise and C/N_o is reviewed. The goal is to find the maximum tolerable phase noise for minimal C/N_o degradation.

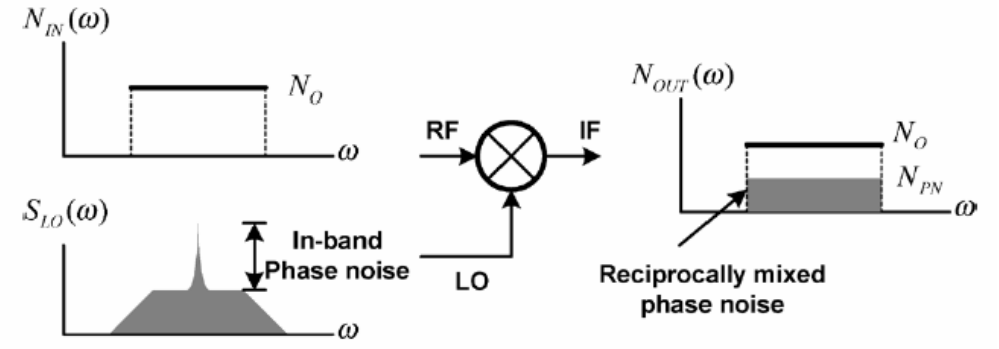


Figure 6.9 Reciprocal mixing of the in-band thermal noise and phase noise [42].

The phase noise requirement comes from the reciprocal mixing of the phase noise spectrum by the in-band thermal noise itself, as seen in Figure 6.9. Multiplication in the time domain corresponds to convolution in the frequency domain, and hence the added noise density due to the phase noise is calculated by [42]

$$N_{PN}(\omega) = N_{IN}(\omega) * S_{LO}(\omega) = \int_{-\infty}^{\infty} N_{IN}(\omega) S_{LO}(\omega - \omega') d\omega' = N_o \int_{-\infty}^{\infty} S_{LO}(\omega) d\omega \qquad (6.6)$$

where $S_{LO}(\omega)$ is the phase noise of LO. The last integral term represents the absolute rms jitter of the local oscillator, normalized to its period,

$$\frac{N_{PN}}{N_o} = \int_{-\infty}^{\infty} S_{LO}(\omega) d\omega \approx \left(\frac{\Delta T_{LO,rms}}{T_{LO}} \right)^2 \equiv {\sigma_{rms}}^2 \qquad (6.7)$$

The effective C/N_o at the mixer output can be written by

$$\left(\frac{C}{N_o}\right)_{out} = \frac{C}{N_o + N_{PN}} = \left(\frac{C}{N_o}\right)_{in} \cdot \left(\frac{1}{1+\int S_{LO}(\omega)d\omega}\right) = \left(\frac{C}{N_o}\right)_{in} \cdot \left(\frac{1}{1+\sigma_{rms}{}^2}\right) \quad (6.8)$$

In order to obtain less than 0.1 dB loss on C/N_o, the averaged phase noise should be lower than -80 dBc/Hz [42]. From this limit, it can be inferred that small-sized ring voltage controlled oscillator (VCO) is promising low cost solution, as presented in [49]. However, when considering power consumption, the LC tank VCO is still advantageous since it uses fewer active devices.

6.4.3 Summary

Based on the previous discussion, we can conclude the design specifications in Table 6.2. And the gain and noise distribution is summarized in Table 6.3. The parameters in tables will be updated along with the design.

Table 6.2 Summary for GPS receiver front-end requirements.

Parameters	Specification	Note
Sensitivity	-130 dBm	At antenna
Noise Figure	< 9 dB	From input of LNA to output of mixer
Phase Noise @	< - 80 dBc/Hz	For VCO.
C/N_o	35 dB	For whole GPS receiver front-end
ADC	2-bit	1.2 dB signal loss
Current	< 4.5 mA	Limited to LNA, VCO and mixers
Power	< 4.5 mW	Limited to LNA, VCO and

		mixers

Chapter 7

Ultra-Low Power Low Noise Amplifier (LNA) Design

7.1 Introduction

The first stage of a RF receiver is a Low-noise amplifier (LNA), whose main purpose is to provide enough gain to overcome the noise of subsequent stages (such as mixer) and linearity while not degrading the signal-to-noise ratio. Much valuable research on CMOS LNA design in submicron technologies has been done in recent years: from the topology investigation [50, [51, [52], and the design guidelines [53], to various new ideas on design improvement for low noise figure [54, [55, [56], high power gain [54], low power consumption [55], and high linearity [57]. The frequency range of these CMOS LNA designs is from 900 MHz to 5.2 GHz [58, [59], and the technologies in use is as small as 0.18 um or less.

In this chapter, an ultra-low power LNA is implemented using SOI deep-submicron (SOIDSM) 80 nm FinFET technologies. As described in Chapter 5, the double-gate MOSFET (FinFET) is considered as one of the most attractive devices to succeed the planar MOSFET. With two gates controlling the channel, the short-channel effects are greatly suppressed. The transition frequency of the characterized FinFET transistors is 42 GHz when working in velocity saturation region, and 20 GHz when working in moderate inversion.

With the FinFET transistors operating in moderate inversion, the operation current will be several times smaller than that in saturation for a given transconductance.

As a result, the FinFET transistors open the door to realize micro-power front-end applications.

In chapter 6 the GPS receiver architecture, design methodologies, and implementation requirements were discussed. All of those are optimized to meet the low power requirement. In this chapter, the LNA topology choice is illustrated first. Then the ultra-low power LNA is proposed. Finally, the performance is presented and compared with previous designs.

7.2 LNA Topology Choice

The four most widely used topologies, shown in Figure 7.1, are reviewed. One will be selected for use in the low power GPS receiver.

The first topology shown in Figure 7.1(a) uses resistive termination of the input port to provide 50 Ω impedance. The drawback of using of real resistors is that the added resistor contributes its own noise comparable to that of the source resistance [60]. According to the calculation [60], the noise figure will be above 6 dB. It does not satisfy our system requirement for noise figure.

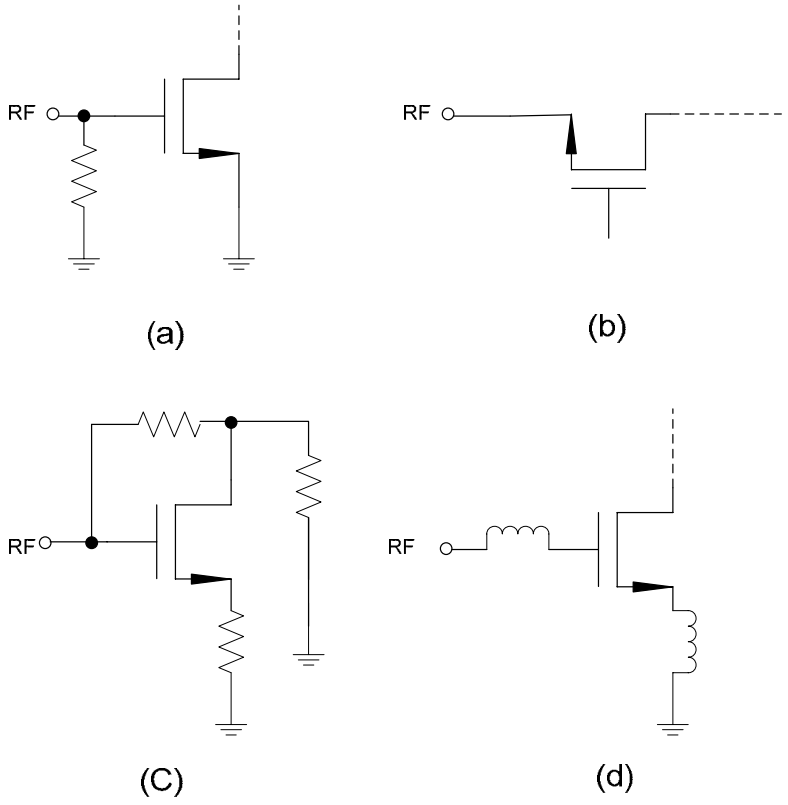


Figure 7.1 Common LNA topologies. (a) Resistive termination, (b) $1/g_m$ termination, (c) shunt-series feed back, and (d) inductive degeneration.

Figure 7.1 (b) shows the second topology which uses the source of MOSFET in a common-gate (CG) configuration as the input termination. CG topology has good high frequency performance. The minimum theoretically achievable noise figures tends to be around 3 dB or greater in practice. Input impedance is determined by $1/g_m$.

Figure 7.1 (c) represents another topology, which utilizes shunt and series feedback to set the input and output impedances of the LNA [61]. It is a broadband amplifier, but it has very high power dissipation compared to others with similar noise performance. For a GPS receiver, a broadband front end is not required and it is desirable to use narrowband technology to save power and reduce interferers.

Figure 7.1 (d) employs inductive source degeneration to generate a real term in the input impedance. At the operational frequency, the source inductor provides a stable 50 Ω input impedance. It is the most prevalent topology used for LNA design. And it offers the possibility of achieving the best noise performance of any architecture [50].

Based on above analysis, it seems that the common-gate LNA (CGLNA) and common-source LNA (CSLNA) topology is good candidate for GPS receiver. The detailed analysis and comparison of CGLNA and CSLNA is reviewed below.

7.2.1 Common-source LNA (CSLNA)

The CSLNA is based on the common-source with source inductive degeneration amplifier. Figure 7.2 shows the schematic of a popular cascade single-ended CSLNA. At the operation frequency, the input inductors L_s provides stable 50 Ω input impedance. The input inductors L_g, L_s and input device gate-to-source capacitance, C_{gs} provide the operational frequency for CSLNA.

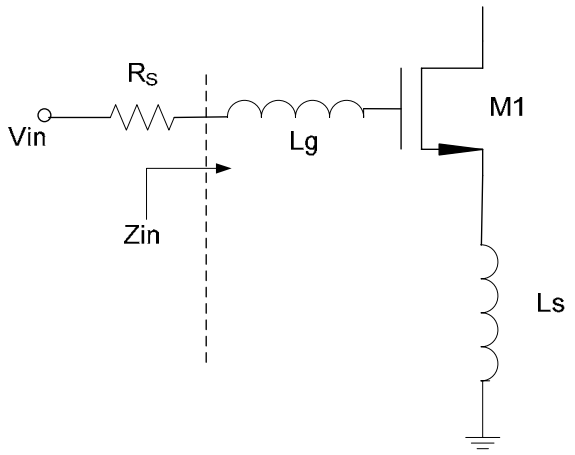


Figure 7.2 CSLNA Schematic Diagram.

A simple analysis of the circuit depicted in Figure 7.2 shows that the input impedance of the circuit is given by (7.1) when neglecting the M1 drain-gate overlap

capacitance, and the inductor parasitic elements toward the substrate (C_{ox}, R_{si} and C_{si} in Figure 3.3(a))

$$Z_{in} = j\omega\left(L_g + L_s\right) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s + R_g + R_{Lg} + R_{Ls} \tag{7.1}$$

where C_{gs} amd g_m are respectively the gate-source capacitance and the transconductance of M1 and R_g the gate resistance of M1. R_{Lg} and R_{Ls} represent the parasitic series resistance of L_g and L_s, respectively.

At resonance, the imaginary term of Z_{in} will be zero, which gives

$$\omega\left(L_g + L_s\right) - \frac{1}{\omega C_{gs}} = 0 \tag{7.2}$$

From (7.2) the center frequency can be derived,

$$\omega_o = \sqrt{\frac{1}{\left(L_g + L_s\right) C_{gs}}} \tag{7.3}$$

The real part of the input impedance is

$$Z_{in,real} = R_g + R_{Lg} + R_{Ls} + \frac{g_m}{C_{gs}} L_s \approx R_g + R_{Lg} + R_{Ls} + \omega_T Ls \approx \omega_T Ls \tag{7.4}$$

where ω_T is an approximation of the transition frequency of M1. Using (7.4) the inductance of source inductor can be determined. Once L_s has been determined L_g can be calculated by (7.3).

One of the most attractive advantages of this topology is that the inductor used to match the input impedance is noiseless, unlike the topology shown in Figure 7.1 (a), which employs a noisy resistor in the signal path to provide the 50 Ω termination resistance. This explains the low noise performance and popularity of the inductively degenerated CSLNA.

The effective small-signal transconductance of the input transistor is a parameter which accounts for the transconductance for input transistor and input matching network.

$$G_m = g_m Q = \frac{g_m}{\omega_o C_{gs}\left(R_s + \omega_T L_s\right)} = \frac{\omega_T}{\omega_o R_s\left(1 + \frac{\omega_T L_s}{R_s}\right)} \tag{7.5}$$

Note that the input matching circuit is a pure series RLC resonant circuit. At resonance the voltage across *Cgs* is enhanced by *Q* times, where *Q* is the quality factor of input matching RLC network. In other words, the *Q* enhancement mechanism provides a *free gain* of *Q* for both the input signal and the noise from the source resistance *Rs*. The added gain from the input matching circuit helps to suppress channel noise. If the input is matched to R_s, we have

$$G_m = \frac{1}{2R_s}\left(\frac{\omega_T}{\omega_o}\right) \tag{7.6}$$

It is worth noting that the effective transconductance G_m is only related to the ratio of ω_T to ω_o and is independent on the MOSFET small-signal transconductance g_m.

The gate-to-drain capacitance C_{gd} provides a feedthrough path from input to output, decreasing the reverse isolation. In addition, the miller effect of C_{gd} provides a shunt current branch at the input, which further complicates the input matching. One should add a cascode stage to mitigate the Miller effect of C_{gd} and improve reverse isolation.

Next, the noise performance of CSLNA is analyzed. Starting with the noise model of a MOSFET, as shown in Figure 7.3, we surmise that their main noise sources are the thermal channel noise and the induced gate noise.

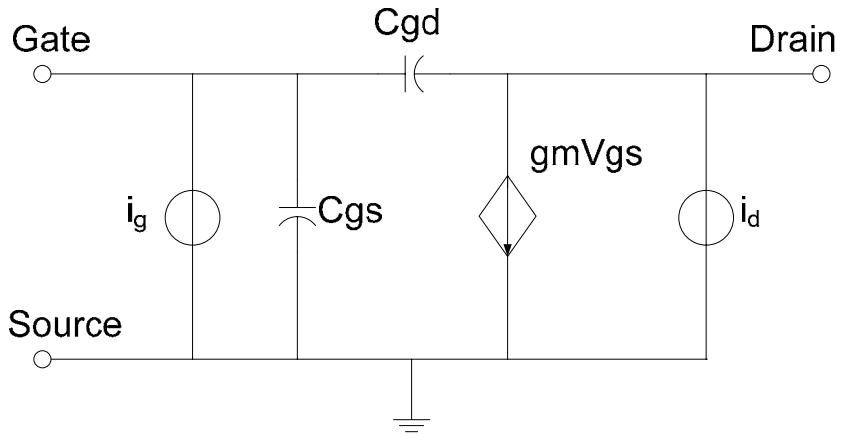


Figure 7.3 MOSFET equivalent noise model.

The channel thermal noise i_d shows a white power spectral density described by

$$\overline{i_d^2} = 4kT\gamma g_{d0}\Delta f \tag{7.7}$$

where k is Boltzmann's constant, g_{d0} is the zero-bias drain conductance, Δf is the bandwidth of interest and γ is a bias-dependent factor that, for long channel devices, satisfies the inequality

$$\frac{2}{3} \le \gamma \le 1 \tag{7.8}$$

the value of 2/3 holds when the device is in saturation mode and the value of one is valid when the drain-source voltage is zero. For short-channel devices, however, γ is much greater than 2/3 for devices operating in saturation [50]. For the present there is no standard γ value for devices operating in moderate inversion.

In addition to channel thermal noise i_d, a companion noise current i_g at the gate of the MOSFET, which is known as induced gate noise, has been observed in both theory and experiment,

$$\overline{i_g^2} = 4kT\delta g_g \Delta f \tag{7.9}$$

$$g_g = \frac{\left(\omega C_{gs}\right)^2}{5 g_{d0}} \tag{7.10}$$

where δ is another bias-dependent empirical parameter, classically equal to 4/3 for long-channel devices. Unlike the white noise spectrum of the channel thermal noise, induced via the gate noise has *blue* spectrum frequency. The gate noise is partially correlated with the drain noise, with a correlation coefficient given by [62]

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}} \approx 0.395\, j \tag{7.11}$$

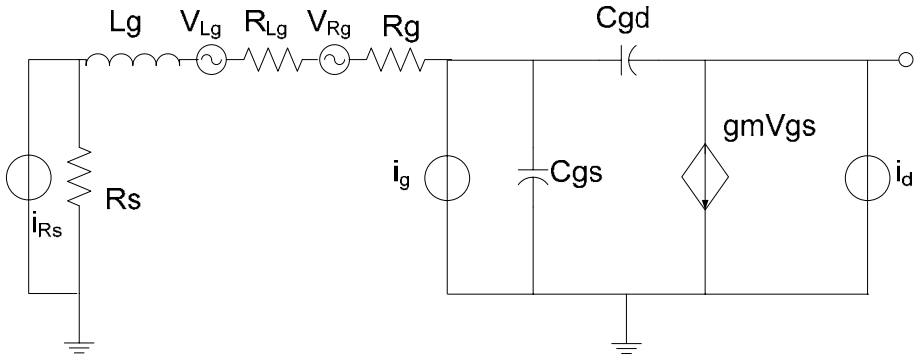


Figure 7.4 Small-signal model for noise calculation of CSLNA.

After determining the noise source of MOSFET, we will derive the noise factor of the CSLNA. To obtain the expression for noise factor, it is instructive to calculate the transfer functions of the different noise source in the CSLNA [63]. The small-signal circuit used in the computation is shown in Figure 7.4. In this CSLNA noise model five noise sources are considered, input impedance noise, series resistance noise from gate inductor, gate resistance noise from input MOS device, channel thermal noise of MOS device and induced gate current noise. The noise factor is derived according to its definition, that is, the ratio of total output noise power to the output noise power due to input source impedance, as shown

$$F = 1 + \frac{R_{Lg}}{Rs} + \frac{R_g}{Rs} + \frac{\gamma}{\alpha}\frac{1}{Q}\left(\frac{\omega}{\omega_T}\right)\left[1 + \frac{\delta\alpha^2}{5\gamma}\left(1+Q^2\right) + 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right] \tag{7.12}$$

where

$$\alpha \approx \frac{g_m}{g_{d0}} \tag{7.13}$$

For long-channel device, $\alpha = 1$. For short-channel device, $\alpha \le 1$.

7.2.2 Common-gate LNA (CGLNA)

Figure 7.5 shows a CGLNA where the gate terminal is shorted to an AC ground and the input signal is injected at the source terminal. The resistance looking into the source terminal is about $1/g_m$, which provides the input 50 Ω match. Unlike CSLNA, there is no Miller effect associated with C_{gd} in CGLNA, which results better reverse isolation.

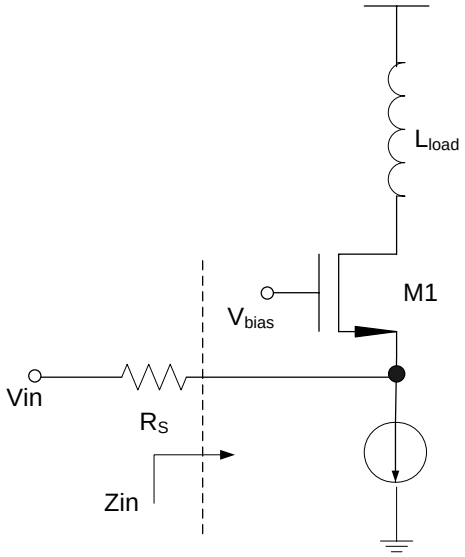


Figure 7.5 the CGLNA schematic diagram.

The effective small-signal transcondance of the input transistor of CGLNA is

$$G_m = \frac{1}{2R_s} \tag{7.14}$$

However, the CGLNA suffers from the presence of a noisy channel conductance in the signal path, which attenuates the noise performance. It can be shown that under perfect input matching, the CGLNA has the following noise factor [60]

$$F = 1 + \frac{\gamma}{\alpha} + \frac{\delta\alpha}{5}\left(\frac{\omega}{\omega_T}\right)^2 \tag{7.15}$$

In the above equation, the third term is from the contribution of the induced gate noise, which is negligible compared to contribution of channel noise. Neglecting gate noise for a CGLNA is reasonable approximation since the gate noise is not amplified, unlike it in CSLNA. Therefore, the noise factor of CGLNA is approximated by

$$F = 1 + \frac{\gamma}{\alpha} \tag{7.16}$$

In CSLNA we can not make this approximation since the gate noise is amplified and becomes comparable to channel noise.

7.2.3 Comparisons of CSLNA and CGLNA

Based on the above discussion, the detailed comparison is listed in Table 7.1.

Table 7.1 The comparison between CSLNA and CGLNA ("+" indicates better, "-" indicates worse).

	CSLNA	CGLNA	Comments
Gain	+	–	$G_{CSLNA} = \frac{1}{2R_s}\left(\frac{\omega_T}{\omega_0}\right) > G_{CGLNA} = \frac{1}{2R_s}$
Noise Figure	+	–	Discussed above
Input matching	–	+	CGLNA has lower Q parallel resonant network.
Reverse isolation	–	+	C_{gd} in CSLNA provides a feed-forward path between input and output.

In this work the NF for receiver front-end requirement is less than 6 dB in order to obtain the desired GPS receiver sensitivity, as discussed in Chapter 6. So the topology CSLNA is used to achieve low noise and low power GPS receiver front end. Once selecting the CSLNA topology, the next question is to take either a single-ended or differential architecture. The signal-ended LNA architecture has at least one important shortcoming, and that is sensitivity to parasitic ground inductance. There are several advantages in using a differential LNAs. Firstly, the use of Gilbert mixers and the low-IF architecture requires a differential feed source. If the single-ended is taken we need to add a Balun to generate the differential signal. The Balun itself has about 0.5 dB loss. Secondly, the virtual ground formed at the tail removes the sensitivity to parasitic ground inductance, which makes the real part of the input impedance purely controlled by the source degeneration inductance (L_s). Thirdly, the differential amplification of signal ensures attenuation of the common mode signal. But for equal total power consumption, the noise figure of differential LNA is higher than its single-ended counterpart. Specifically, the power consumed is twice that of a single-ended LNA to achieve the same noise figure. Since it is hard to tell which architecture is better for this application, both architectures will be taken to implement the ultra-low power GPS receiver front-end circuits.

Next the ultra-low power FinFET differential LNA design is described. The single-ended LNA is just the half circuit of differential LNA. It has the same NF but only consume half power of differential LNA.

7.3 Circuit Design

The LNA design starts from noise optimization because of the tight noise requirement. The input devices are required to work in moderate inversion region to reduce amplifier drain current with the exception of the tail current source. All the formula used to estimate the noise is for MOSFET apply in moderate inversion. Starting from the noise analysis, we found the minimal transcondance to achieve the lowest noise figure. Once gm is found to be 20 mS, the drain current can be determined by referring the inversion coefficient curve with IC equal 0.1 to 1 in Figure 7.6. The curve in Figure 7.6 is drawn for 80 nm FinFET transistors with the description in 2.3.1. The g_m/I_D of around 20 to 40 is achievable in this range. Taking the average value 30, we can get $I_D = g_m/30 = 666\,\text{uA}$. The tail current will be twice the I_D, 1.3 mA. The aspect ration of M1 and M2 can be calculated by choosing bias current:

$$\frac{W}{L} = \frac{I_D}{I_t(IC)} \tag{7.17}$$

where *IC* is the desired inversion coefficient, which is about 0.15. I_t is specific current,

$$I_t = 2n\mu_n C_{ox} U_T^2 \tag{7.18}$$

which is about 1.46 uA for 80 nm device. The W/L is determined about 3000. Knowing channel length equal to 80 nm the width of input device is determined to be 240 um.

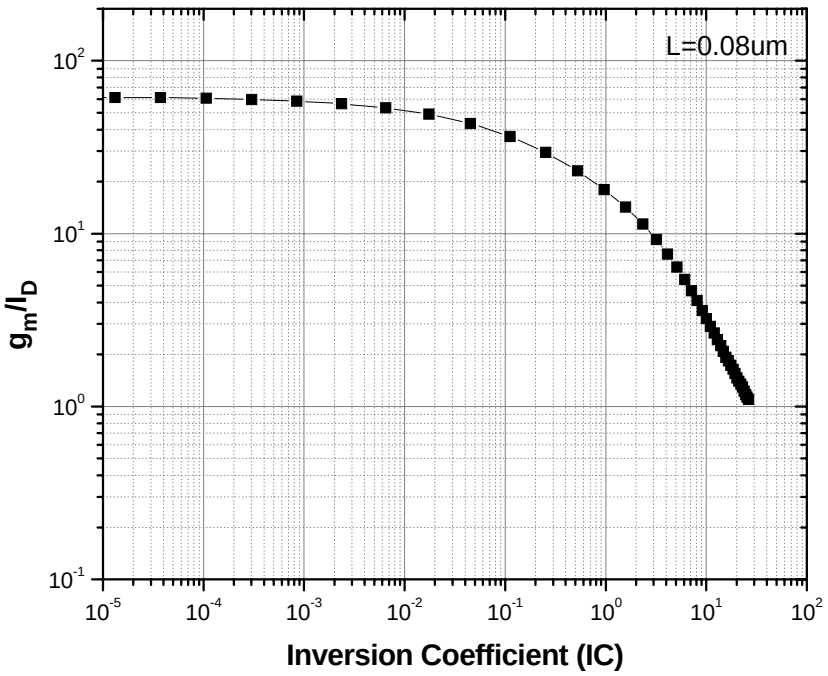


Figure 7.6 g_m/I_D versus inversion coefficient curve.

Knowing g_m, device size and C_{gs}, the transition frequency of input device is

$$\omega_T \approx \frac{g_m}{C_{gs}} \tag{7.19}$$

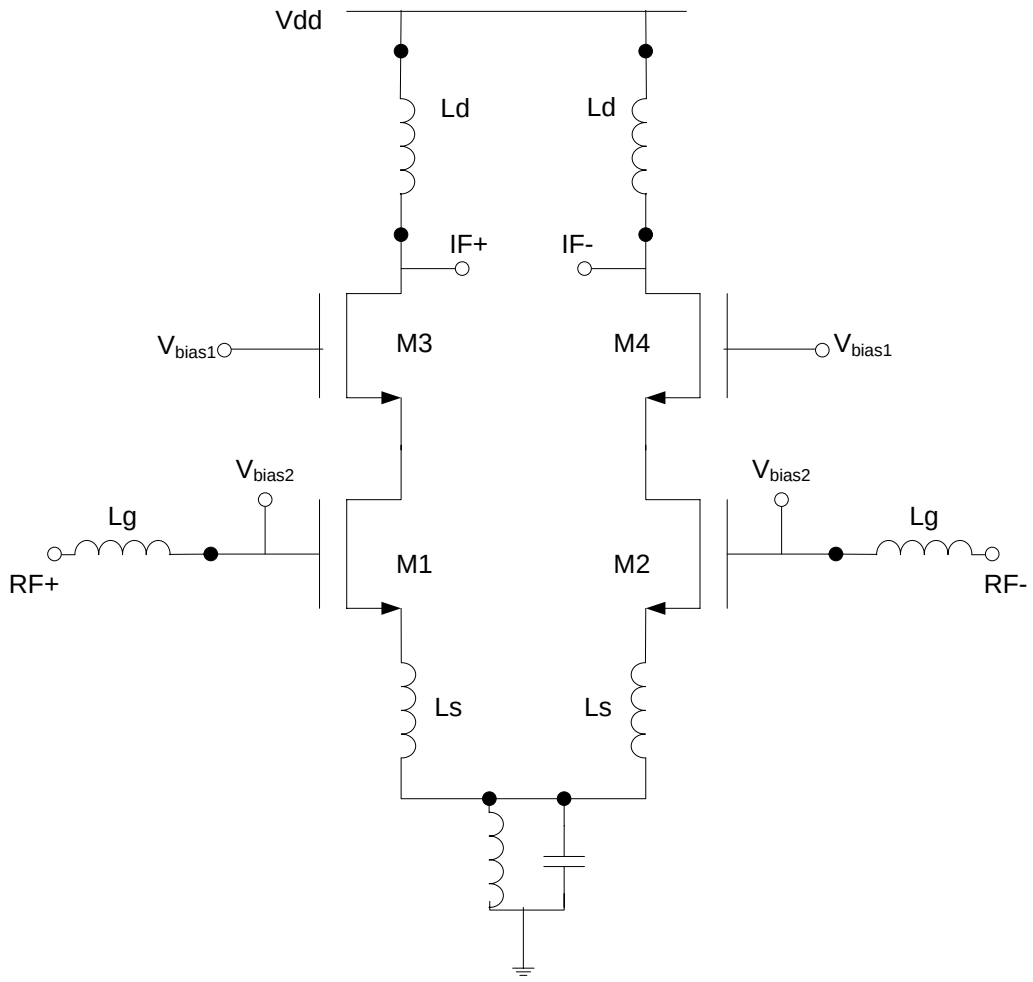


Figure 7.7 Proposed differential LNA schematic.

The source inductance can be determined once the source resistance R_s is set to 50 Ω.

$$L_s = \frac{R_s}{\omega_T} \tag{7.20}$$

L_g can be determined by

$$L_g = \frac{1}{C_{gs}\omega_0^2} - L_s \tag{7.21}$$

Where ω_0 is the center frequency of GPS L1 band.

The complete LNA schematic is shown in Figure 7.7. All passive components values in design are summarized in Table 7.2. All active devices are summarized in table 7.3.

Table 7.2 Differential LNA passive components values.

Ls	Lg	Ld
100 pH	20 nH	15 nH

Table 7.3 Differential LNA active components values.

Devices	Threshold voltage	Sizing (um/um)	IC	Overdrive Voltage
M1- M4	0.33 V	250/0.08	0.12	- 15 mV

7.4 LNA Performance

Periodic Steady-State (PSS) and S-Parameter (SP) simulation are adopted to measure the gain, noise and linearity performance separately.

In SP simulation, the voltage gain of LNA is determined by plotting S21 versus frequency. Figure 7.8 shows the maximum voltage is 21 dB at 1.57 GHz. And the S12, S11 and S22 are -30 dB, -15 dB and -4 dB, respectively, as shown in Figure 7.9 and Figure 7.10. The noise performance is measured by NF shown in Figure 7.11, which is about 2.6 dB at 1.57 GHz. If the gate induced noise is counted it will reach 3.4 dB which is dependent on device model used. Stability measurement of LNA is presented in Figure 7.12.

The LNA's linearity can be measured by 1-dB compression point, as shown in Figure 7.13. The 1-dB compression point is -35 dBm. The performance summary for proposed LNA is listed in Table 7.4.

Compared with the differential LNA designs previously published, the resulting LNA consumes only 1.08 mW with 1 V supply voltage.

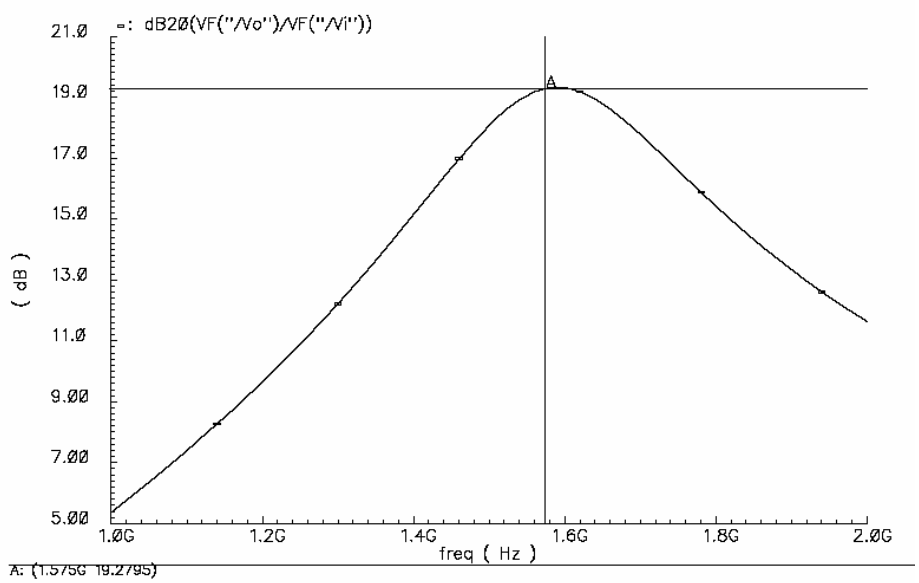


Figure 7.8 Voltage gain of differential LNA.

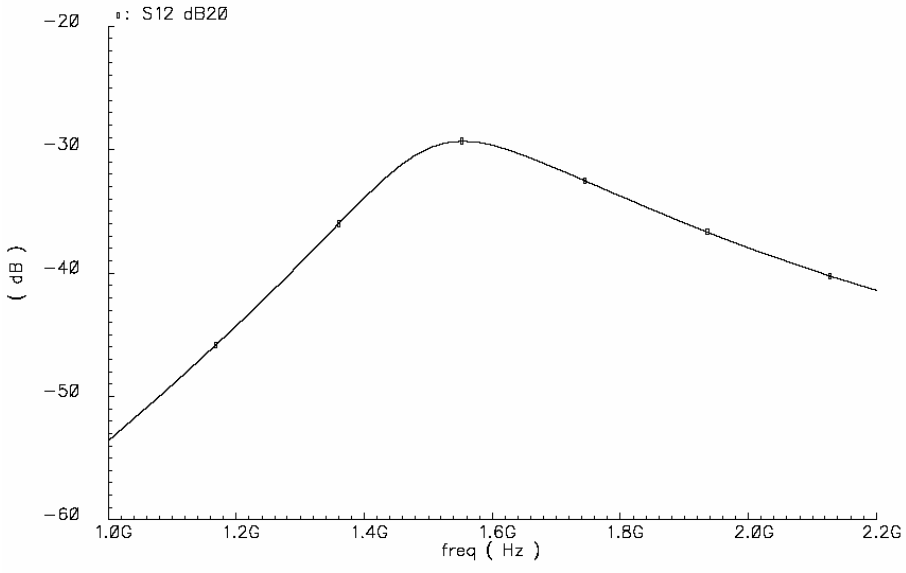


Figure 7.9 S12 of differential LNA.

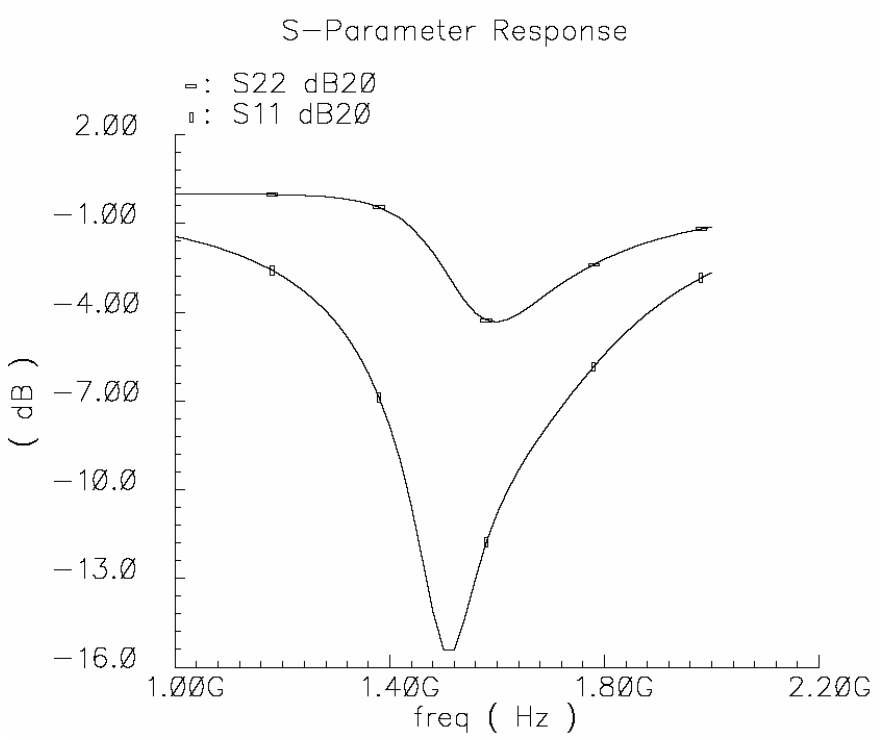


Figure 7.10 S11 and S22 of LNA.

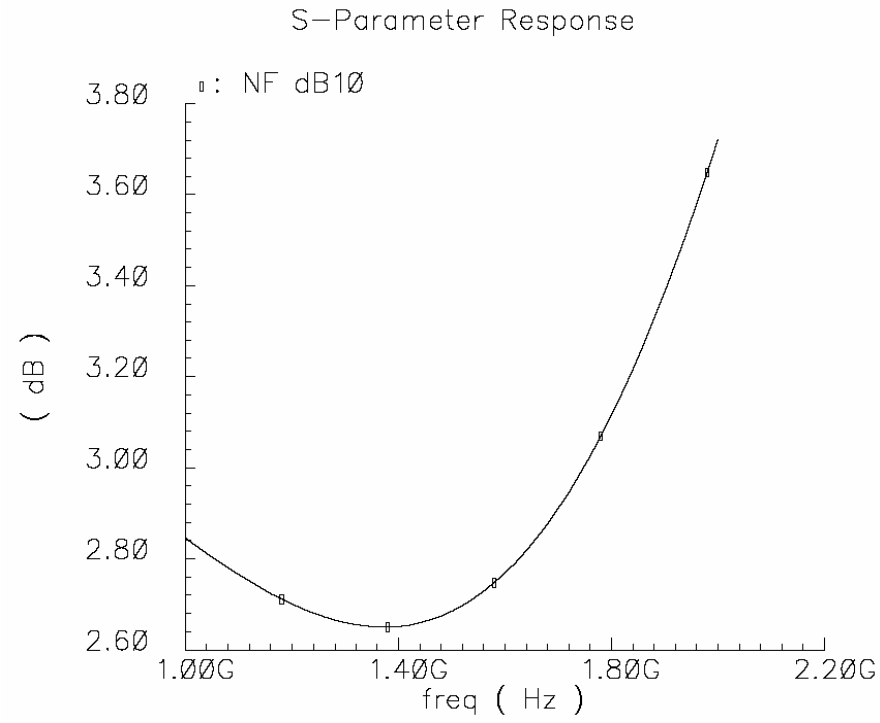


Figure 7.11 Noise Figure of LNA.

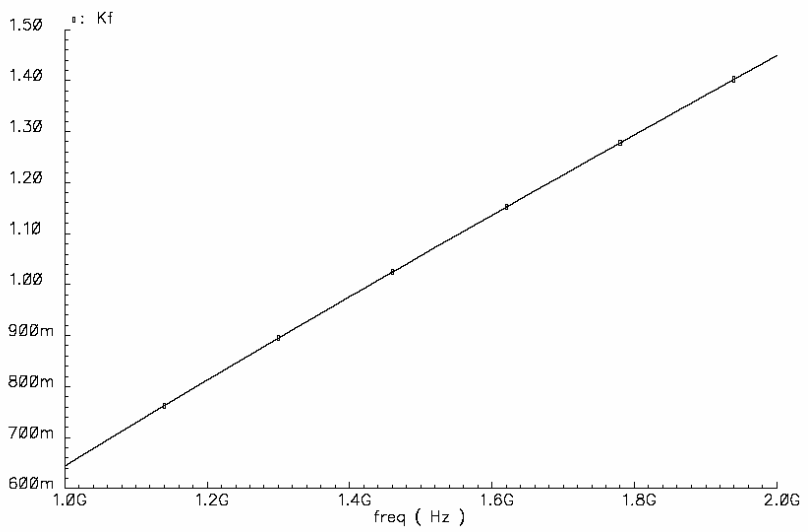


Figure 7.12 Stability measurement of LNA

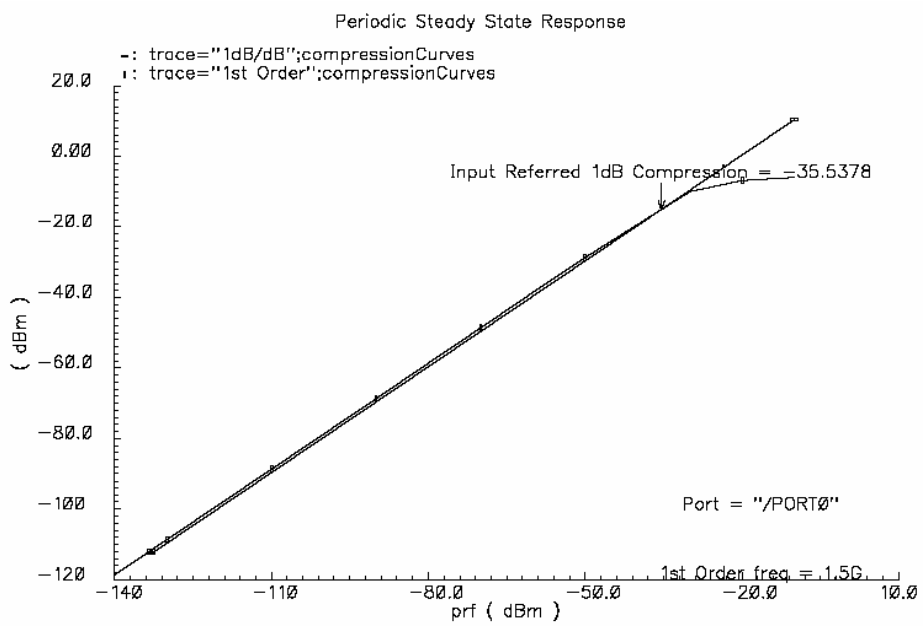


Figure 7.13 1-dB compression point measurement of LNA

Table 7.4 Ultra-low power LNA performance summary

Technology	0.08 um FinFET
Supply Voltage (Vdd)	1 V
DC Current	1.44 mA
Power Consumption	1.44 mW
Threshold Voltage	0.33 V
Transition frequency	18 GHz
Operation Frequency	1.57 GHz
S21, S11, S22	20 dB, -15 dB, -4 dB
Noise Figure	3.4 dB
1-dB compression	-35 dBm
Power Consumption	1.44 mW

Chapter 8

Micro-power RF Voltage Controlled Oscillator Design

8.1 Introduction

Voltage controlled oscillators (VCOs) are essential building blocks of modern communication systems and are worked with other building blocks to establish phase lock loop (PLL) to generate stable local oscillation signal, which is provided to the ports of mixer in a typical transceiver architecture to translate data between baseband and frequencies suitable for wireless transmission. In a PLL, all building blocks such as VCO, phase detector and loop filter contribute phase noise at the output. For a well designed PLL, the phase noise of VCO is the dominant source of phase noise [64]. Therefore, in the following discussion, the phase noise of VCO is emphasized. The basic LC oscillator topology is widely used in RF receiver design due to its superior phase noise performance. Consequently, we focus our discussion on LC oscillators.

In this chapter, following the oscillation fundamental of oscillator, the topologies of oscillators are compared. Then the proposed VCO design procedures are presented. Finally, the performance of VCO is shown in figures and summarized in table.

8.2 Oscillators Fundamental

8.2.1 Feedback Oscillator Model

An oscillator can be viewed as a feedback system as shown in Figure 8.1 where the transfer function from $V_{in}(s)$ to $V_{out}(s)$ is

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{H(s)}{1+H(s)} \tag{8.1}$$

For the oscillation to begin, a loop gain of unity or greater is necessary. Oscillation occurs for the condition $|H(j\omega_0)| = 1$. Even without an input, i.e., $V_{in}(s) = 0$, the oscillation is self-sustained. To maintain constant amplitude, there are two necessary conditions that must be met at ω_0.

$$\begin{aligned} &|H(j\omega_0)| = 1 \\ &\angle H(j\omega_0) = 180^o \end{aligned} \tag{8.2}$$

Known as Barkhausen's criteria, these conditions are necessary but not sufficient [65]. In order to ensure oscillation in the presence of temperature and process variations, we typically choose the loop gain to be at least twice or three times the required value.

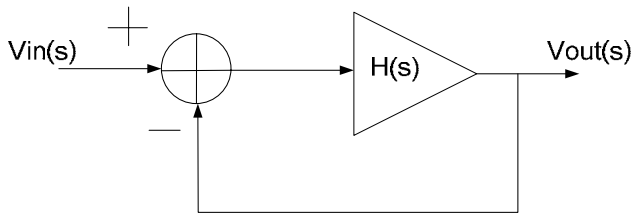


Figure 8.1 oscillator viewed as feedback system.

An LC resonant tank is an integral component of LC oscillator circuit in Figure 8.1. It functions as a frequency selective network to eliminate high-order harmonics and thus to stabilize the oscillation frequency, as shown in Figure 8.2.

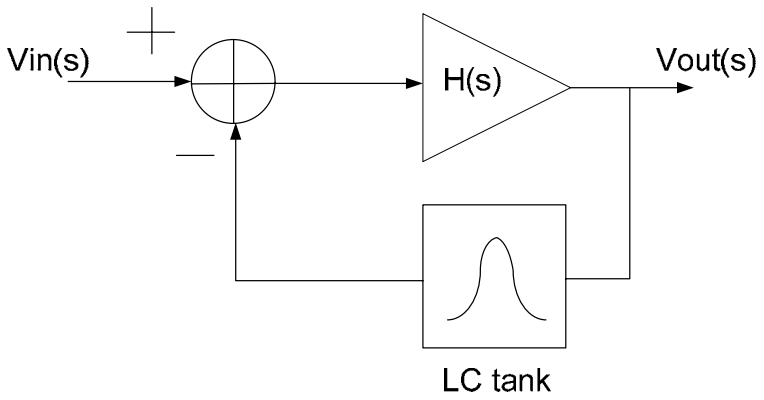


Figure 8.2 Feedback model for oscillator with LC resonant tank.

8.2.2 One-Port Oscillator Model

Most oscillators employed in RF applications use LC resonators. They are known to provide high spectral purity and lower phase noise than other types such as ring oscillators, etc. [66]. Monolithic inductors have gradually appeared in bipolar and CMOS technologies in the last decade, which makes it possible to design oscillators based on passive resonant circuits.

As shown in Figure 8.3. An inductor *L* placed in parallel with a capacitor *C*, building a parallel resonance LC tank, which resonates at a frequency

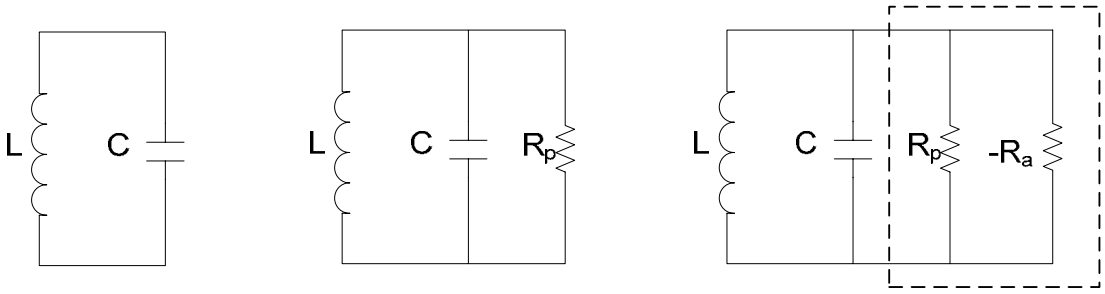
$$\omega = \frac{1}{\sqrt{LC}} \tag{8.3}$$

Since the LC tank network is composed only of reactive components, the oscillating signal ideally maintains its oscillation amplitude without attenuation. The energy in the LC resonator transfers back and forth between the inductor and the capacitor in the form of the magnetic and electric energy without loss due to power dissipation. In practice, however, the quality factors of the inductor and the capacitor are

finite. As a result, this leads to a practical parallel RLC network as shown in Figure 8.3(b). Quality factor Q of this network is defined as:

$$Q = \frac{R}{\omega_0 L} = R\omega_0 C \tag{8.4}$$

At this frequency, the impedance of the inductor, $j\omega L$, and the capacitor, $1/(j\omega C)$, are equal and opposite, thereby, yielding an infinite impedance, in theory. The circuit in Figure 8.3 (a) has an infinite quality factor, Q. In practice, inductors (and capacitors) suffer from resistive component, R_p. In order to sustain the oscillation, a practical tank network needs an active circuit that provides a negative resistance, $-R_a$, to cancel out the positive loss resistance of the tank. Such a topology is called one-port oscillator.



(a) ideal (b)practical (c) negative R

Figure 8.3 LC tank.

8.3 Oscillator Topology Comparison

In this section, several oscillator topologies will be compared with an emphasis on their phase noise and power consumption.

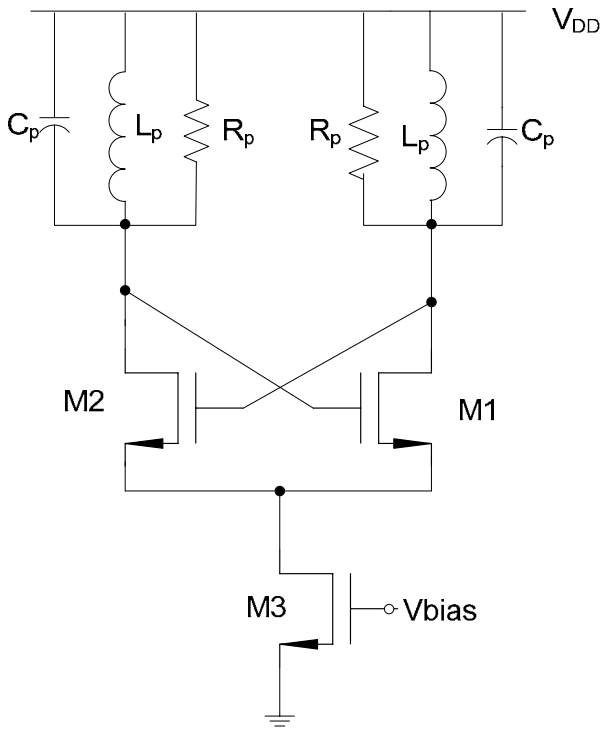


Figure 8.4 the typical cross-couple oscillator.

Figure 8.4 shows the NMOS-only cross-coupled oscillator topology, widely used in high-frequency integrated circuits due to the ease of implementation and differential operation [67, [68, [69]. It can be shown that the small-signal impedance looking into the drains of M1 and M2 is $-2/g_m$ assuming the parasitic capacitance is neglected. To enable oscillation, the negative small-signal conductance added by the cross-coupled transistor pair should overcome the loss in Rp, that is

$$g_m > \frac{1}{R_p}$$

or $$g_m R_p > 1 \qquad (8.5)$$

Figure 8.5 shows the complementary version using both NMOS and PMOS transistors. This topology provides a larger tank amplitude for a given tail current in the current limited regime defined in [68]. Since the PMOS is used in this topology, the

oscillation frequency is limited by the PMOS. In this work p-channel FinFET transistors can not provide enough bandwidth in moderate inversion. Thus this topology is not considered.

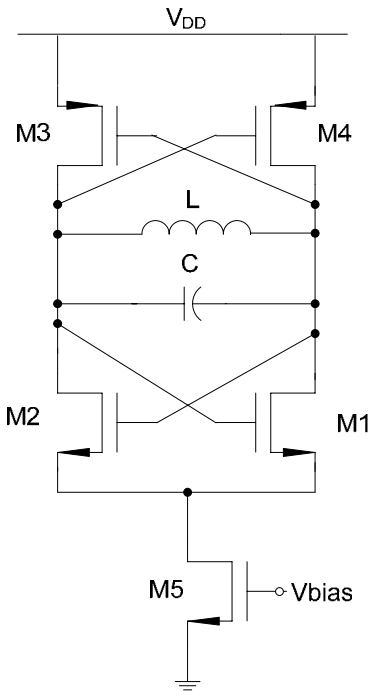


Figure 8.5 The complementary cross-coupled oscillator.

Figure 8.6 depicts the single-ended Colpitts oscillator topology. Compared to cross-coupled VCO, the Colpitts topology features superior phase noise because noise current from the active devices is injected into the LC tank during the tank voltage when the impulse sensitivity is low [70, [71].

The negative conductance is formed using transistor M1 and capacitive divider C_1 and C_2 in a positive feedback arrangement. Its small-signal impedance looking into the drain of M1 is calculated using test voltage divided by test current. It can be shown that the negative conductance loading the tank is $-\frac{g_m C_1 C_2}{(C_1 + C_2)^2}$. Therefore, the startup condition for Colpitts oscillator is

$$\frac{g_m C_1 C_2}{(C_1 + C_2)^2} > \frac{1}{R_p}$$

or $$g_m R_p > \frac{(C_1 + C_2)^2}{C_1 C_2} \tag{8.6}$$

For a typical case, $C_2 = C_1$ (8.6) becomes $g_m R_p > 4$. Comparing to (8.5), we conclude that Colpitts oscillator has more difficult start-up condition than the conventional cross-coupled LC oscillator for a given transconductance, i.e., higher power consumption is needed to ensure reliable start-up in the presence of process, voltage or temperature variations. And the lack of differential outputs needed to suppress common-mode coupling has hindered its usage in CMOS.

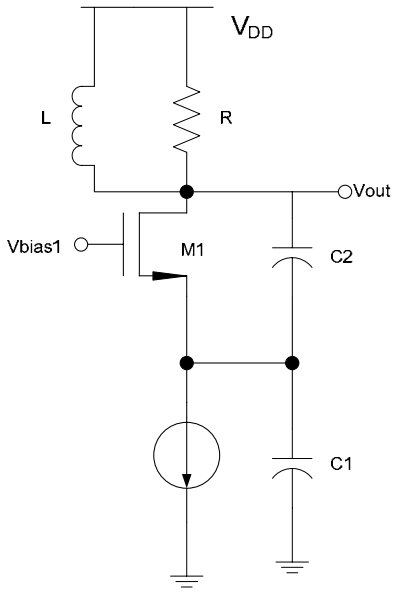


Figure 8.6 The typical Colpitts oscillator.

Figure 8.7 shows a differential Colpitts VCO. With a small-signal analysis, the start-up condition for the differential Colpitts oscillator is given by

$$g_m R_p > \frac{(C_1 + C_2)^2}{2 C_1 C_2} \tag{8.7}$$

Compared to (8.6), the effective small-signal transcondance is doubled, the start-up condition is also relaxed by a factor of two. In a conventional Colpitts oscillator, the tail current is always ON. To reduce power consumption, a switching current source can be employed [72]. Power consumptions is reduced at the expense of added noise from the tail device. The idea is that since in a Colpitts oscillator the MOSFET is on for less than half of a cycle, two switches can be used to steer one current source to the two MOSFETs while sustaining oscillation, shown in Figure 8.8 [73].

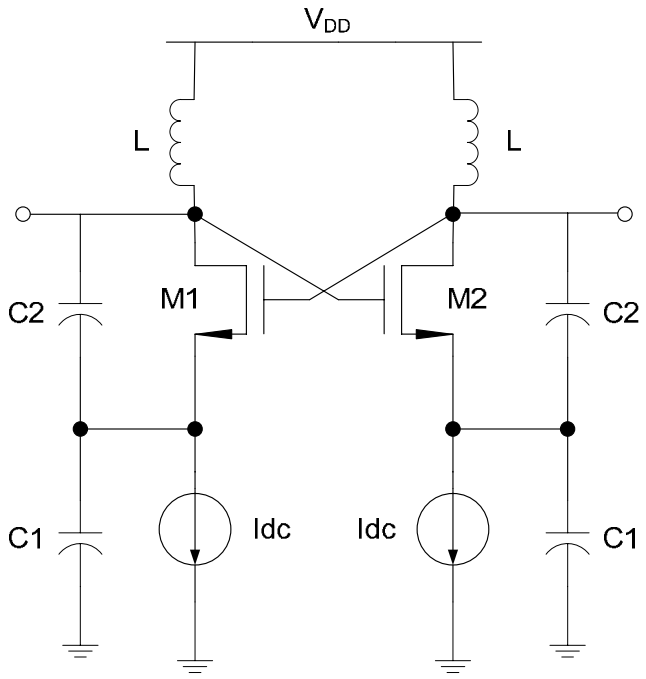


Figure 8.7 The typical differential Colpitts oscillator.

Although differential Colpitts oscillator has superior phase noise performance than cross-couple differential, it has greater power than cross-couple differential oscillator [72]. Since in this work low power consumption is our research goal and the cross-coupled oscillator already supplies enough phase noise and cost less power than differential Colpitts oscillator, the cross-coupled oscillator is taken to implement the ultra-low power VCO.

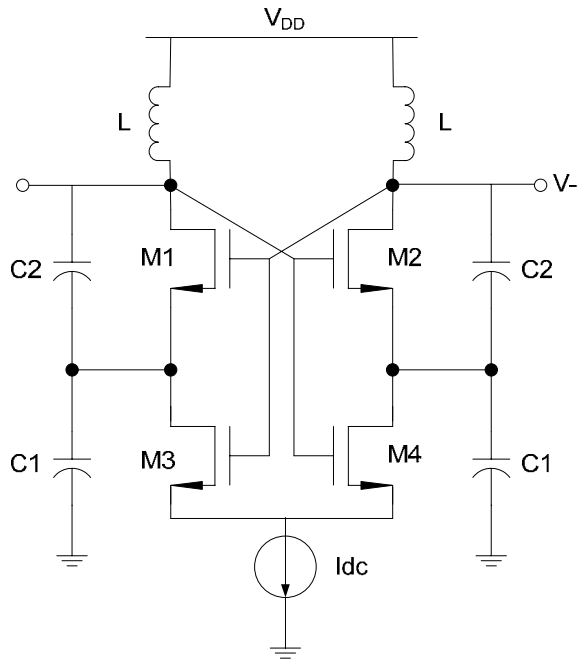


Figure 8.8 The differential Colpitts oscillator with current-switching technique.

8.4 Oscillator Circuit Design

With the VCO topology selected, the design procedures are described in this section. The proposed VCO schematic diagram is shown in Figure 8. 10. Starting with the oscillation frequency equation given in (8.1), we take 1.57 GHz as the target frequency. In Chapter 3, a monolithic model was developed for the on-chip inductor with substrate removed. The model is valid for the number of turns as large as 4.5. In this design we will use the complete inductor model for accuracy, where all substrate losses are taken into account. As described in Section 8.2, the cross-coupled pair must provide enough negative resistance to cancel the tank losses and allow oscillation to start up. This negative resistance equals $-1/g_{m1,2}$ for half cross-coupled pair.

The required g_m for startup sets a lower limit on the current consumption of oscillator. To determine the necessary g_m for startup, the tank losses (R_P) must be calculated from the inductor model. In Chapter 3, the calculated Q_L was shown to be

approximately 10 at 1.5 GHz for an inductor with a substrate. At the resonant frequency, the LC tank may be modeled as depicted in Figure 8.3, where the tank losses are included in the resistance R_p. The equivalent parallel resistance at resonance may be calculated by taking the capacitor as lossless and calculating the parallel resistance R_p for an inductor with finite Q given by the overall tank quality factor,

$$R_p \approx Q_L^2 R_s \tag{8.8}$$

The g_m required for startup is

$$g_m \geq \frac{1}{R_p} \tag{8.9}$$

For a given operating frequency, it is desirable to use the inductor in the LC tank which has largest R_p value. The Table 8.1 shows the inductance, series resistance and Q of inductors with different number of turns at 1.5 GHz.

Table 8.1 On-chip inductors specifications at 1.5 GHz.

No. turns	L (nH)	Rs (Ω)	Q
1.5	1.34	1.8	7.28
2.5	2.83	3.34	8.39
3.5	6.4	6.15	10.36
4.5	11.52	9.65	11.88

With Table 8.1, the 4.5 turn inductor is taken since it has largest R_P value. In practice, the size of the inductor is usually limited by the difficulty of implementing large spiral coils on-chip. On the other hand, the critical transconductance is inversely proportional to tank

quality factor, so an improvement in inductor *Q* reduces startup current requirements and lowers power consumption.

As described in Chapter 3, inductors large than 12 nH are not normally integrated on chip. R_P is approximately 1000 Ohm at 1.57 GHz for 4.5 turns inductor. Therefore, the minimal requirement of g_m is approximately 1 mS. In order to ensure reliable startup, the transconductance is set to 2 mS.

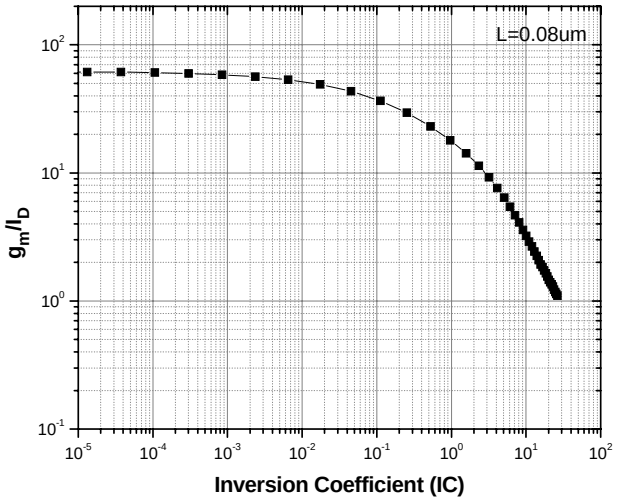


Figure 8.9 Inversion coefficient for L=80 nm FinFET transistor.

To optimize the transcondance for minimal bias current, devices M1 and M2 are designed to operate with inversion coefficient between 0.1 and 1. This is the moderate inversion for transistors. Referring to Figure 8.9, g_m/I_D of around 20 to 40 is achievable in this range. Taking the average value 30, we can get $I_D = g_m/30 = 66$ uA. The tail current will be twice the I_D, or 132 uA. The aspect ration of M1 and M2 can be calculated by choosing bias current:

$$\frac{W}{L} = \frac{I_D}{I_t(IC)} \tag{8.10}$$

where *IC* is the desired inversion coefficient, which is about 0.15. I_t is specific current, which is about 1.46 uA for 80 nm device. So the W/L ratio is determined around 350. The total bias current sourced by M3 is approximately 130 uA. In order to maintain stable tail current a long-channel device is chosen and operation in saturation region is selected for accuracy. The width of M3 is calculated to be about 20 um. All the devices sizing and IC is shown in table 8.2.

Table 8.2 Device sizing and IC for oscillator transistor.

Device	Threshold voltage	Sizing (um/um)	IC	Overdrive voltage
M1, M2	0.33 V	30/0.08	0.12	-25 mV
M3	0.5 V	20/1	10	0.2 V

Next, the voltage controlled capacitor design is selected. In this work, the FinFET varactors are used to achieve frequency sweep. All the varactors are n-channel FinFET transistors that have a step-like C-V characteristic. Referring to Figure C.3 in Appendix C: "CV characteristic of FinFET", the FinFET capacitance changes from 2 fF/um^2 to 13 fF/um^2 with gate voltage swept from -0.5 V to 0.5 V. In order to center the oscillation frequency at 1.57 GHz two varactors are connected in parallel which has width 45 um and length 1um. Its capacitance at zero bias is around 470 fF, and its swept capacitance ratio is 6.5.

8.4 VCO Performance

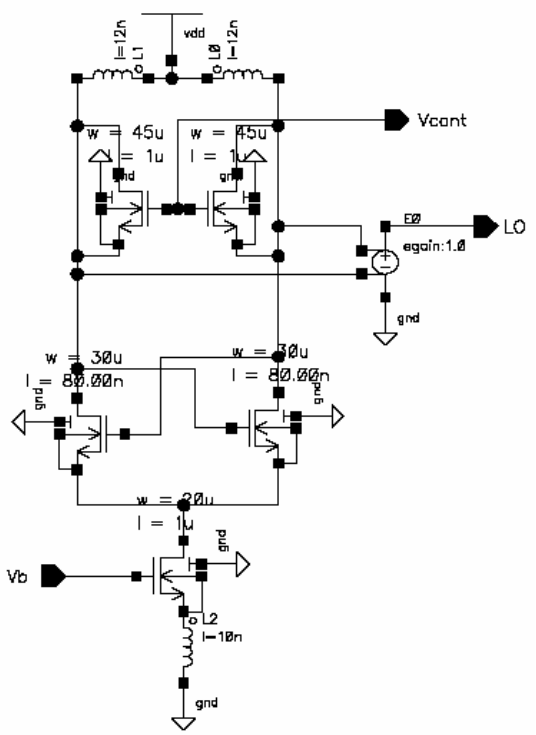


Figure 8.10 Micro-power VCO schematics.

The completed VCO design is shown in Figure 8.10. Its tuning range is 720 MHz wide around the center frequency of 1.57 GHz (i.e., 45.7%) without considering process, voltage and temperature (PVT) variation, as shown in Figure 8.11. Figure 8.12 shows that the differential output oscillation signal amplitude is around 700 mV, that is, around 350 mV peak-to-peaks for single end output. With power supply voltage of 1 V, the phase noise of the VCO is -112 dBc at 1 MHz offset from 1.57 GHz, shown in Figure 8.13.

Compared with the VCO design published before, this VCO consumes only 128 uW with 1 supply voltage.

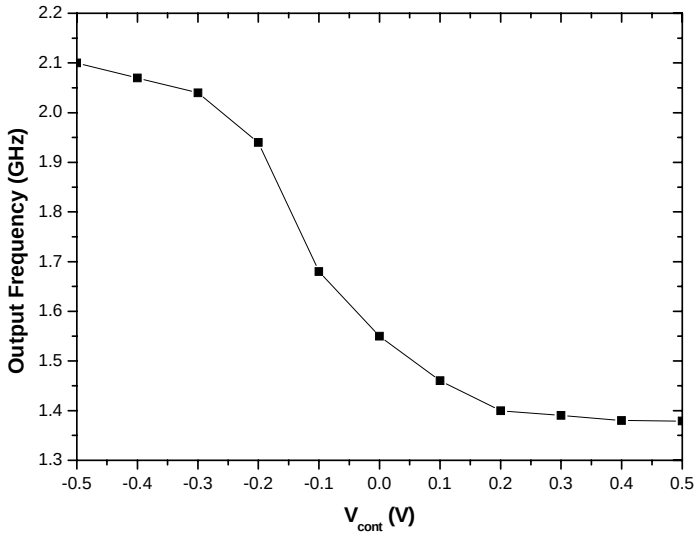


Figure 8.11 Simulated tuning characteristics of the VCO.

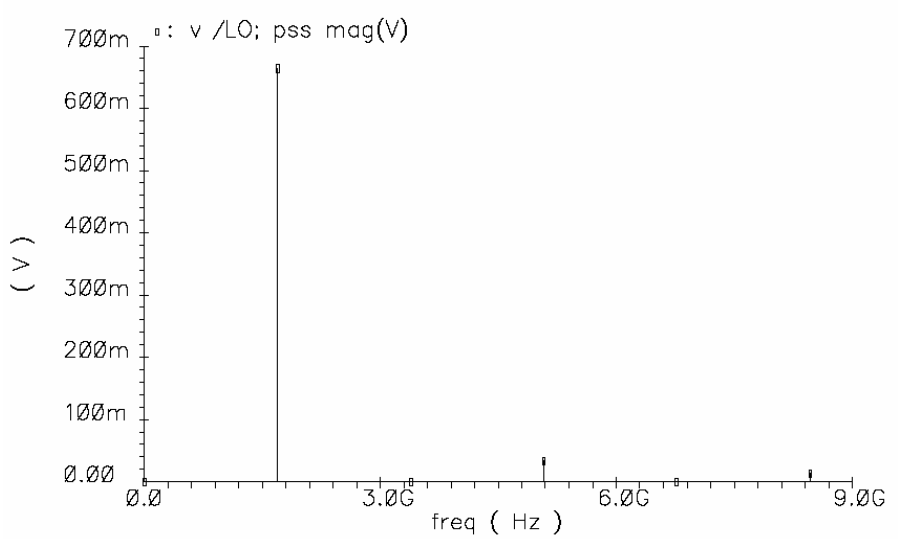


Figure 8.12 Output LO signal magnitude versus frequency.

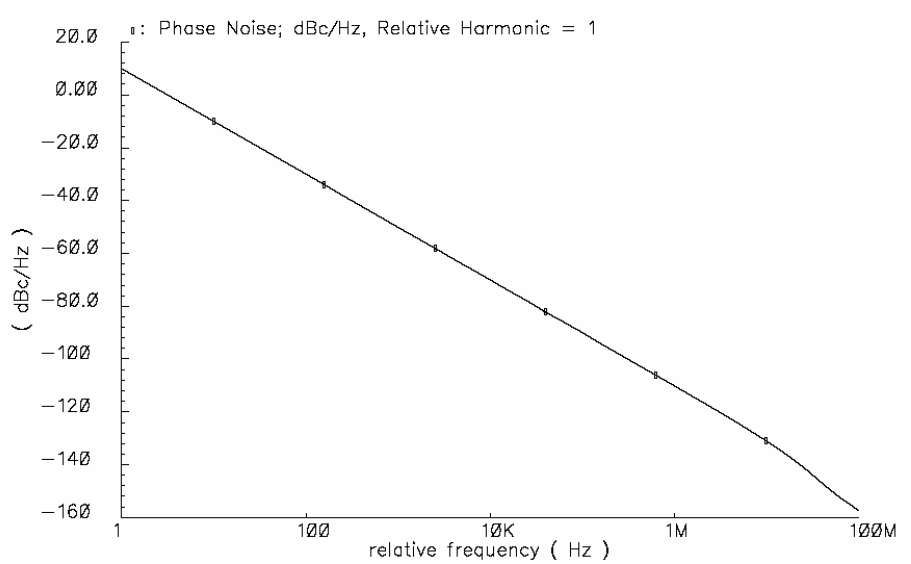


Figure 8.13 VCO Phase noise versus frequency.

Table 8.3 Summary of VCO performance.

Parameters	Value
Supply voltage	1 V
Power Consumption	128 uW
Frequency tuning range	1.38-2.1 GHz
LO Vpp	350 mV
Phase Noise	-111 dBc/Hz @1 MHz offset

Chapter 9

Ultra-low Power Mixer Design

9.1 Introduction

The rapid growth of portable wireless communication systems, such as wireless (cordless and cellular) phones, GPS, wireless local area network (LAN), etc., has increased the demand for low-cost and high performance front-end receivers. Mixers are used for frequency conversion and are the critical components in modern radio frequency (RF) systems which are commonly used to down convert frequencies to achieve frequency translation. The motivation for this translation stems from the fact that filtering out a particular RF signal channel centered among many densely populated, narrowly spaced neighboring channels would require extremely high Q filters. A mixer converts an RF signal at a high frequency into a signal at lower frequency to make signal processing easier and less power consumptive. One of the best known architectures is the downconversion heterodyne receiver, schematically depicted in Figure. 9.1. Here the received RF signal after preamplification in a low-noise amplifier is supplied to a mixer. It is then mixed with local oscillator (LO) frequency f_{LO}. The signal obtained after the mixer contains the frequencies $f_{RF} \pm f_{LO}$, as well as the input signals at f_{RF} and f_{LO}.

With a low-pass filter (LPF) or band-pass filter (BPF), the lower frequency component $f_{RF} - f_{LO}$, known as the intermediate frequency (IF), is selected for further processing.

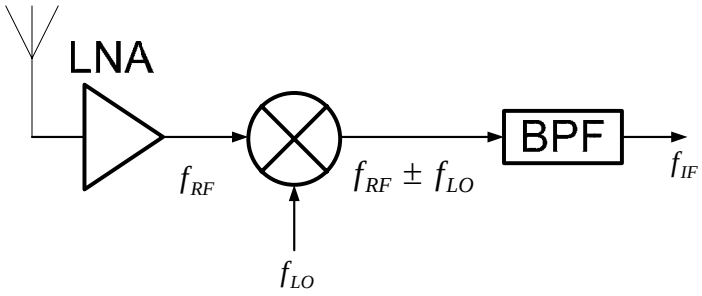


Figure 9.1 The heterodyne receiver system with a mixer.

In this chapter, following the fundamentals of mixing, the mixer topology choice is made based on our application. Then the design procedure is discussed to achieve low-power consumption. Finally, the proposed mixer performance is presented.

9.2 Mixer Fundamentals

The ideal mixer is a device which multiplies two input signals. If the inputs are sinusoids, the ideal mixer output is a signal that contains both the sum and difference frequencies given by

$$(A\cos\omega_{RF}t)(B\cos\omega_{LO}t) = \frac{AB}{2}\left[\cos\left(\omega_{RF} - \omega_{LO}\right)t + \cos\left(\omega_{RF} + \omega_{LO}\right)t\right] \tag{9.1}$$

Typically, either the sum or the difference frequency is removed with a filter. If the LO amplitude is constant, any amplitude modulation in the RF signal is also transferred to the IF signal. Having recognized the fundamental role of multiplication, the most important characteristics of mixers are discussed next.

9.2.1 Conversion Gain

The gain of mixers must be carefully defined to avoid confusion. The voltage conversion gain of a mixer is defined as the ratio of the root mean square (rms) voltage of the IF signal to the rms voltage of the RF signal. The power conversion gain of a mixer is defined as the IF power delivered to the load divided by the available RF power from the source. If the input impedance and the load impedance of the mixer are both equal to the source impedance, then the voltage conversion gain is equal to power conversion gain in decibels. In this work the LNA output impedance is not matched to source impedance. Thus, the voltage conversion gain is adopted instead of power conversion gain.

In terms of conversion gain, mixers can generally be categorized into passive and active mixers. Passive mixers, such as diode mixers and passive field-effect transistor (FET) mixers, have no conversion gain but a conversion loss. On the other hand, active mixers have conversion gain that can reduce the noise contribution from the IF stages but consume considerable more power.

9.2.2 SSB and DSB Noise Figure

Noise figure is defined as the signal-to-noise ratio (SNR) at the input (RF) port divided by the SNR at the output (IF) port. In a typical mixer, there are actually two input frequency that will generate a given intermediate frequency. One is the desired RF signal, and the other is called the image signal. Those two signals are frequently referred as sidebands. The existence of an image frequency complicates noise figure calculation, because noise generation in both the desired and image frequencies contributes IF noise. In the usual case where the desired signal exists at only one frequency, the noise figure is called the single-sideband (SSB) noise figure. In the rarer case, where both the RF and image signal contain useful information, leads to a double sideband (DSB) noise figure.

In summary, the SSB noise figure of a mixer is 3 dB higher than the DSB noise, since the SSB noise figure only count the RF power on one side only.

Noise figures for mixer are considerably higher than those for amplifier because noise from frequencies other than at the desired RF can mix down to the IF. The typical values for SSB noise figure range from 10 dB to 15 dB or more [50].

9.2.3 Isolation and Linearity

The isolation between two ports of a mixer is critical. The LO-RF feedthrough results in LO leakage to the LNA and eventually the antenna, whereas the RF-LO feedthrough allows strong interferers in the RF path to interact with the local oscillator driving the mixer. The LO-IF feedthrough makes the substantial LO signal exists at the IF output, which desensitizes the following stage. Finally, the fraction of the signal in the RF path that appears in the IF is determined by RF-IF isolation. The required isolation levels depend on the environment in which the mixer is used.

Linearity is an important requirement for mixer, and the IF output is expected to be proportional to the RF input signal amplitude. It is in this manner in which linearity is interpreted in the mixer. Like amplifiers, beyond a certain input limit the signal from the mixer distort or clip or have a nonlinear relationship with the input signal. The compression point is the value of RF signal at which a calibrated departure from the ideal curve occurs. Usually, a 1-dB compression point is specified.

9.3 Mixer Topology Comparison

During mixer design, the noise, power consumption, conversion gain, linearity and port isolation have to be considered. Since mixer is not the only component in

circuits, we need to make compromises to simplify the design of LNA and VCO. For multiplier-based mixers, there are two types of them, passive and active mixers. Making a decision on which topology of mixer to use is dependent on the requirement from the application.

9.3.1 Passive Mixer

Figure 9.2 shows the passive double-balanced mixer, which consists of four switches in a bridge configuration. The switches are driven by LO signals in anti-phase, so that only one diagonal pair is conducting at any given time. The IF output is therefore the multiplication of the RF and the LO signal. It is readily seen that this mixer consumes zero DC power because of the passive operation. However, the mixer provides negative conversion gain, which depends on the LO waveform shape. For example, the mixer has a voltage conversion gain of $2/\pi$ (-3.9 dB) for square-wave LO signal, and $\pi/4$ (-2.1 dB) for sinusoidal LO signal.

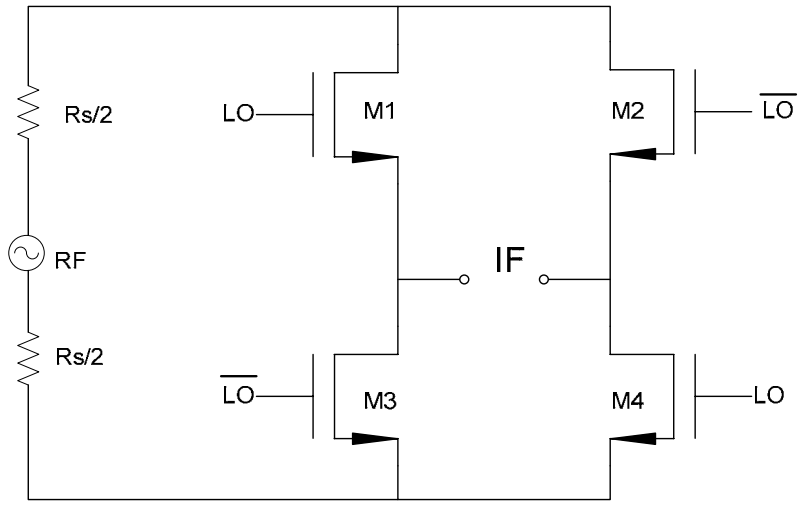


Figure 9.2 Simple double-balanced passive mixer.

The passive mixer shows good linearity if the switches are driven by a square-wave or large-amplitude sinusoidal LO signal. Because with large and sharp LO signals,

the switch on-resistance only depends on the input signal very weakly, thus minimizing non-linearity. However, if the LO amplitude is limited due to low-power (or low-voltage) design requirements, this linearity advantage diminishes. On the other hand, passive mixer does not have good isolation between LO and RF signals, and the LO to RF feedthrough may happen easily.

9.3.2 Active Mixer

Based on the above analysis the active mixer is taken to realize the ultra-low power GPS receiver design. Figure 9.3 shows a typical active double-balanced mixer, which consists of two single-balanced circuits. The two single-balanced mixers are connected in antiparallel as far as the LO is concerned but in parallel for the RF signal. Therefore, the LO terms sums to zero in the output, whereas the converted RF signal is doubled in the output. Thus it provides a high degree of LO-IF isolation, making the filter requirements at the output easier. If layout is carefully taken, IC realizations of this circuits could provide 40 dB LO-IF isolation [50]. Compared with passive mixers active mixers have much higher conversion gain,

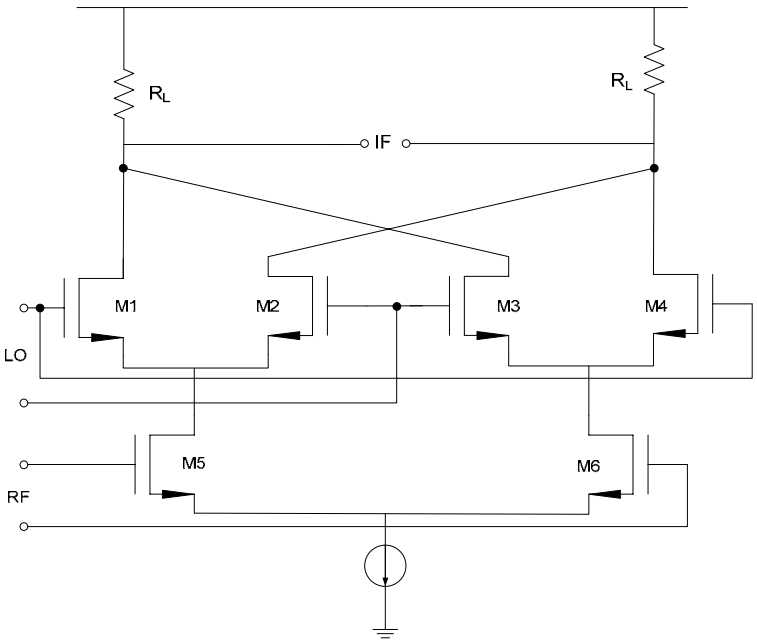


Figure 9.3 A active double-balanced mixer.

$$A_V = \frac{2}{\pi} g_m R_L \tag{9.2}$$

which is typically 10 dB in most reported results. It may add variable gain amplifier (VGA) capability. Despite these advantages, it also has some drawback in this configuration. Firstly it consumes power; secondly it has worse flick noise than passive mixers. One noise source is the transconductor itself, and its noise figure sets a lower bound on the mixer noise figure. The switching pair transistors also degrade noise performance in a number of ways. One noise contribution arises from imperfect switching, which results in attenuation of the signal current. Another NF contributor is the interval of time in which both transistors conduct current and hence generate noise. The mixer noise can be predicted by the following equation [74],

$$\overline{V_{o,n}^2} = 8kTR_L\left(1 + \gamma\frac{2R_L I}{\pi A} + \gamma g_m R_L\right) \tag{9.3a}$$

$$\overline{V_{o,n}^2} = g_m\left(\frac{1}{8kTR_L} + \gamma\frac{I}{4kT\pi A} + \frac{\gamma}{8kT}\right) \tag{9.3b}$$

This equation clearly shows how mixer output noise varies with different circuit parameters, such as LO amplitude (A) and mixer DC bias current in each side of the mixer (I).

Other mixer topologies include the sub-sampling mixer [50] and those implemented from complex signal processing [75]. Both kinds of mixers can achieve good linearity but suffer high noise figures. Such circuits require high-gain preceding LNAs, thus posing more constraints on the overall receiver implementation.

9.4 Circuit Design

Since active and passive mixers have their own characteristics, it is difficult to tell which one is more fitting to this work till this point. In the conclusion chapter, system simulation is done with active and passive mixers, respectively. In this section, only the active double-balanced mixer design is presented since passive mixer design is pretty straightforward.

The mixer topology used for this work is shown in Figure 9.4. In order to make the mixer work under low supply voltage, a parallel LC tank is used to replace the DC current source to create a zero-headroom AC current source. The resonant frequency of the tank is chosen to provide rejection of the RF common-mode component.

The input devices work in the moderate inversion such that the lowest current could be reached for a given transconductance. In Chapter 7, the noise figure of LNA is approximately 3.4 dB. In order to keep the NF of the system less than 6 dB, the NF of

mixer has to be less than 20 dB. Here tradeoff between gain and NF is made to satisfy the NF requirement and the gain requirement together. Considering equations (9.2) and (9.3) we found the transconductance is approximately 6 mS to pursue 10 dB gain at output with NF less than 20 dB. Referring to inversion coefficient curves of Figure 8.8 in Chapter 8 we can determine the drain current and W/L ratio of 150 uA and 1200, respectively.

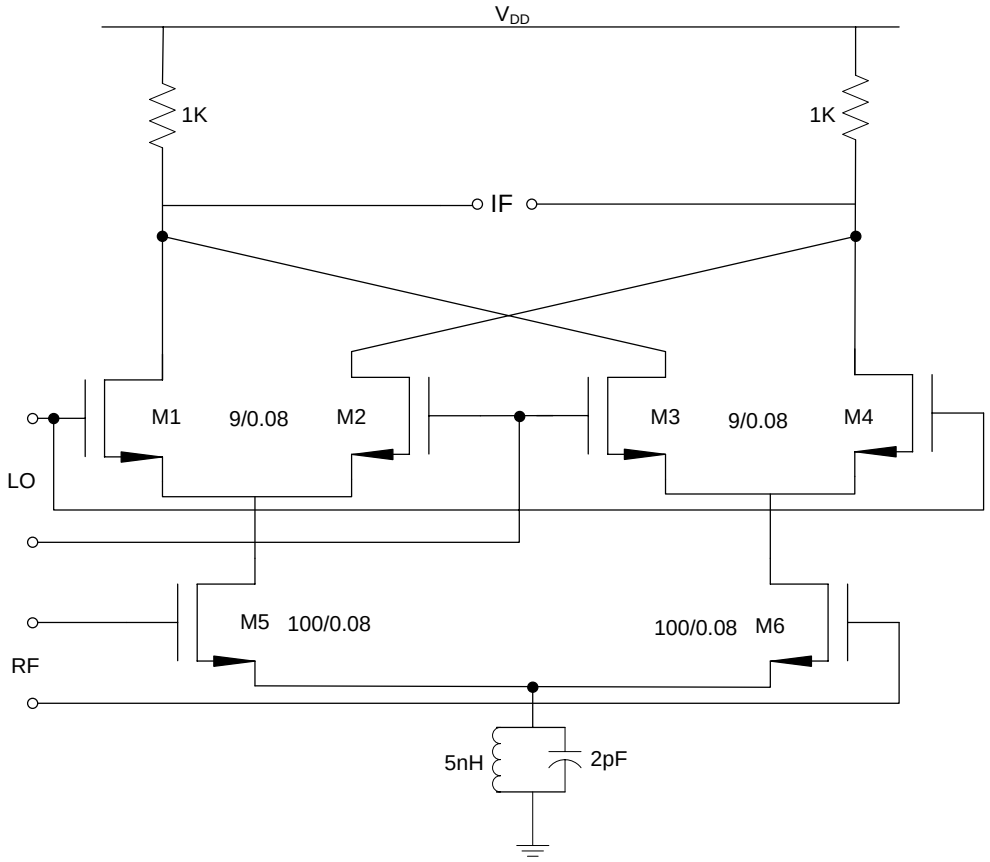


Figure 9.4 Minimum supply-headroom double-balanced mixer.

It turns out to be 150 uA for single balanced mixer. The total current consumption will be 300 uA for double balanced mixer. The shortest channel length is taken for input device to permit the mixer to have sufficient bandwidth. The input device is calculated to be 100/0.08 um and the transistor overdrive voltage is at around -10 mV.

9.5 Mixer Performance

The ultra-low power mixer is simulated in Cadence SpectreRF simulator.

1. Combining PSS analysis with a periodic small-signal transfer function PXF analysis, the conversion gain of the down converter can be determined. At 1.57 GHz, it is 8.3 dB, as shown in Figure 9.5.

2. Combining a PSS analysis with a small-signal Pnoise analysis, the noise figure can be determined. It is found to be about 13.25 dB at 1 MHz IF output, as shown in Figure 9.6.

3. A swept PSS analysis determines the 1dB compression. Figure 9.7 shows the input 1-dB compression is -19.4 dBm.

4. Sweeping PSS analysis with a Periodic AC (PAC) analysis is adopted to produce data for an IP3 plot. The IIP3 is found to be -9.37 dBm , as shown in Figure 9.8.

The final results are summarized in Table 9.1.

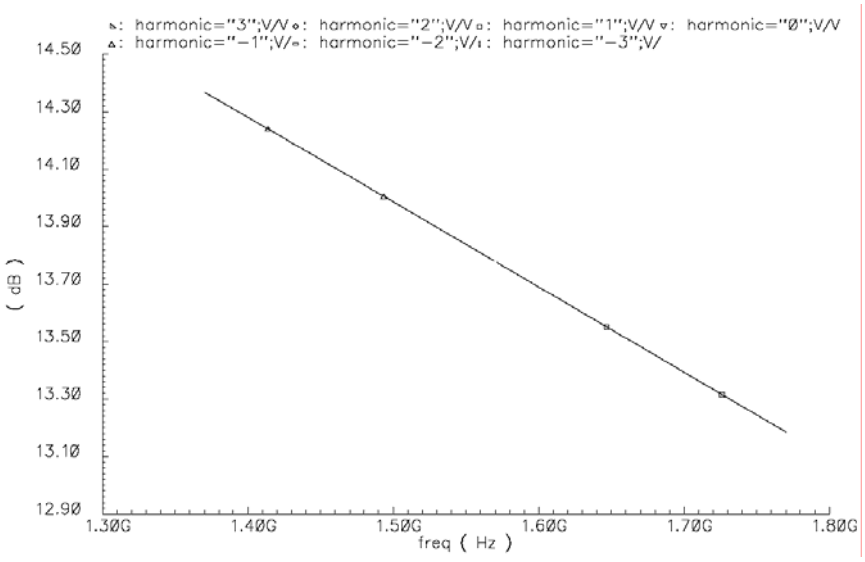


Figure 9.5 Conversion gain versus frequency.

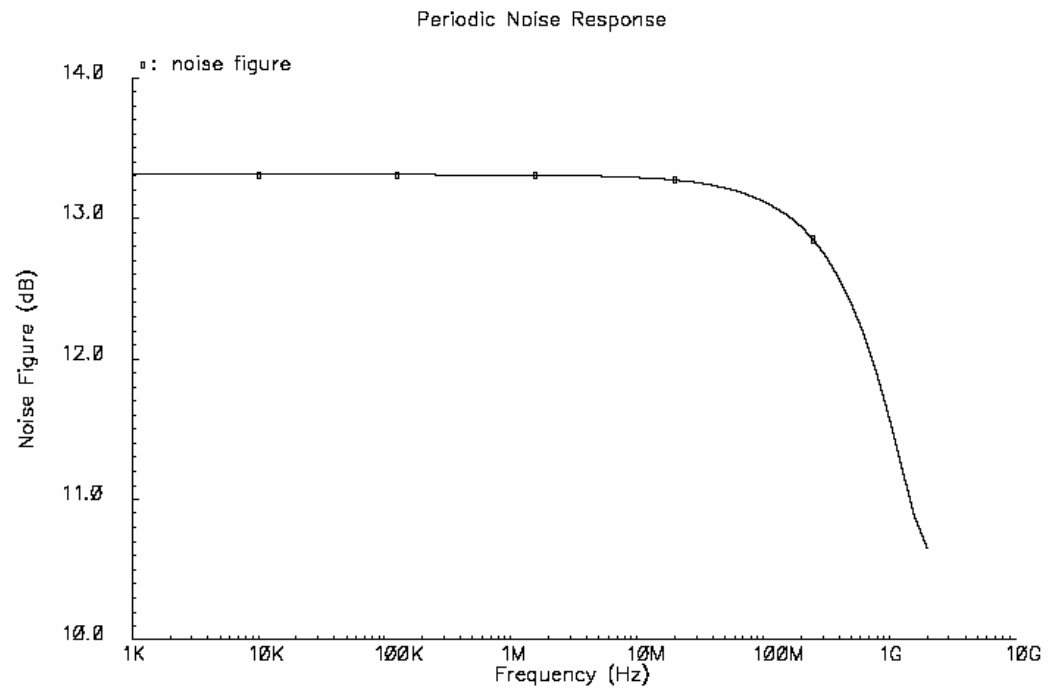


Figure 9.6 Noise figure versus frequency.

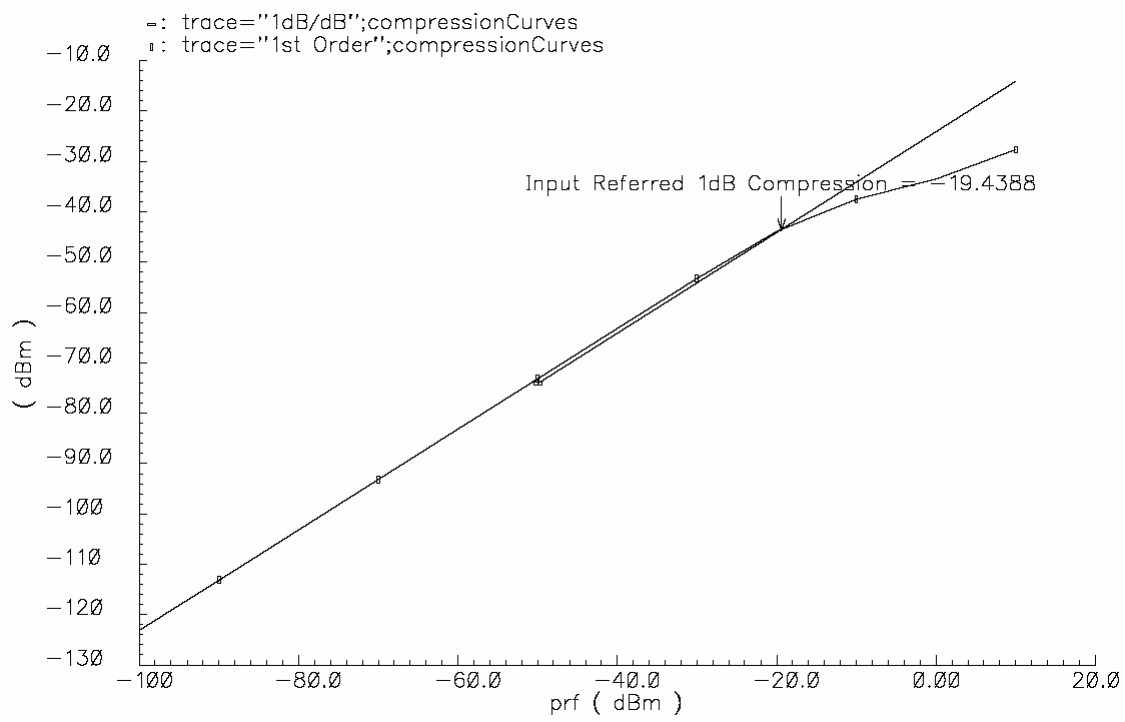


Figure 9.7 1-dB compression point of mixer.

Table 9.1 Active double-balanced mixer performance summary.

Parameter	Value
Supply voltage	1 V
Power dissipation (Vdd=0.5 V)	452 uW
Conversion gain	13.77 dB
Noise figure at 2 MHz (SSB, 50 Ω)	13 dB
Input referred 1-dB compression point	-19 dBm

Chapter 10

Conclusions

10.1 Research Summary

In this research, design approaches and methodologies were presented to realize the ultra-low power RF receiver front-end circuits. Moderate inversion operation was explored as a possible method of reducing power consumption along with the use of low supply voltage. The research is firstly concentrated on passive and active devices modeling. One of the most commonly used passive devices is on-chip inductor. On-chip spiral inductor model was developed firstly. Compared to the model developed by others, this model can predict the behavior of the inductors with different structural parameters over a board frequency range (from 0.1 to 10 GHz). Then the SOI varactor model was developed based on our measurement and extraction.

Besides the passive devices modeling, a new most promising MOSFET candidate, FinFET, was characterized at GHz frequency range. Based on the measurement results, we found the FinFET transistors have superior performance over bulk-Si CMOS technology. And an RF circuit model of FinFET was developed followed that. It provides the basic idea about how to model this new structure MOSFET.

Based on the passive and active device models developed, Global Positioning System (GPS) receiver front end circuits were designed. There are two system designs summarized in this work. We call them called plan A and plan B. The difference is that different types of mixers are used. Plan A uses a differential LNA designed, an active

double-balanced mixer and a VCO. Plan B employs a differential LNA, a passive double-balanced mixer and a VCO. Both system designs are summarized in Figure 10.1.

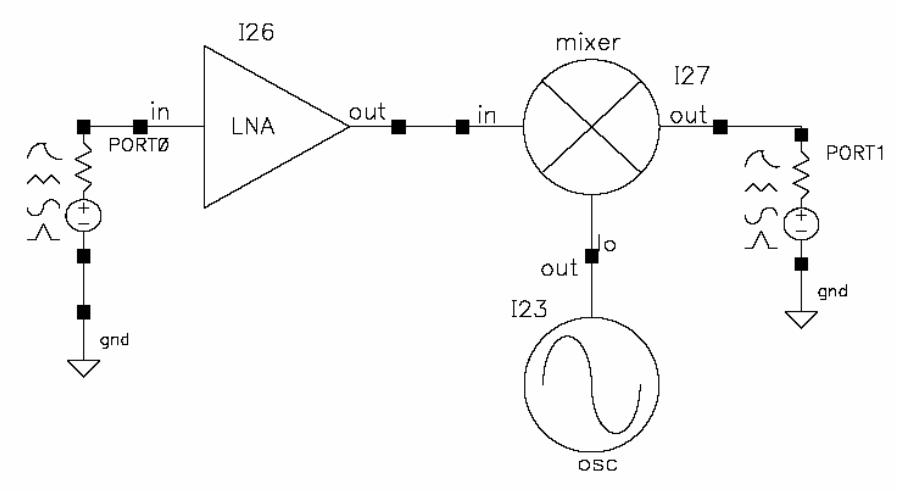


Figure 10.1 The diagram of system simulation of GPS receiver front-end sub-blocking circuits.

In practice we can not really simulate a VCO, mixer and LNA together. During simulation PSS needs to find the beat frequency of VCO frequency. But the beat frequency could change enormously with a tiny change in the VCO frequency. In other words, the combination is chaotic. A fraction of hertz change in the VCO could cause the beat frequency to change from 100 MHz to 0.00001 Hz in a moment [76]. In Figure 10.1 the VCO is an oscillator model in rfLib. The VCO performance is characterized using PSS/PNOISE. The summary of GPS receiver front-end sub-blocking circuits of plan A is shown in Table 10.1.

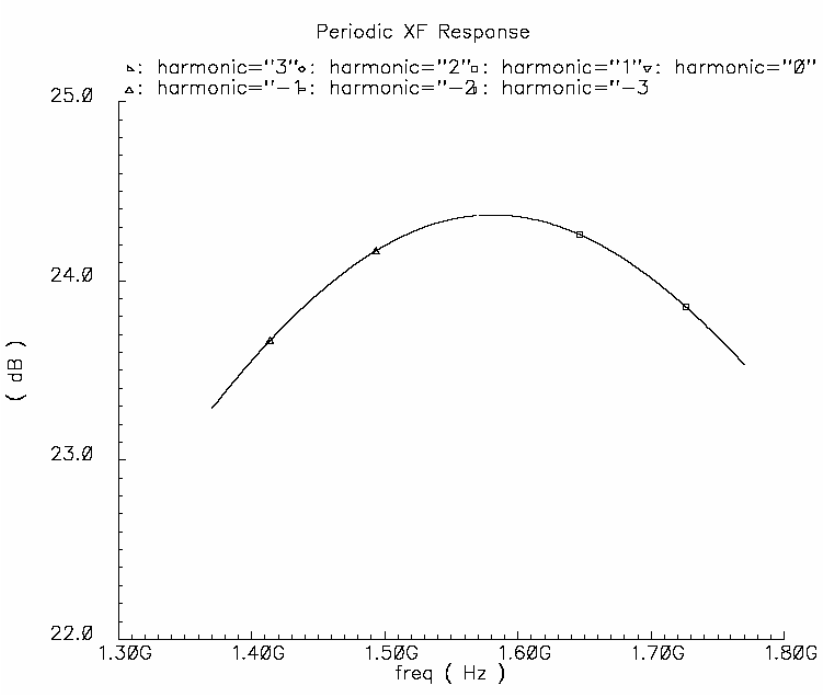


Figure 10.2 The gain of plan A.

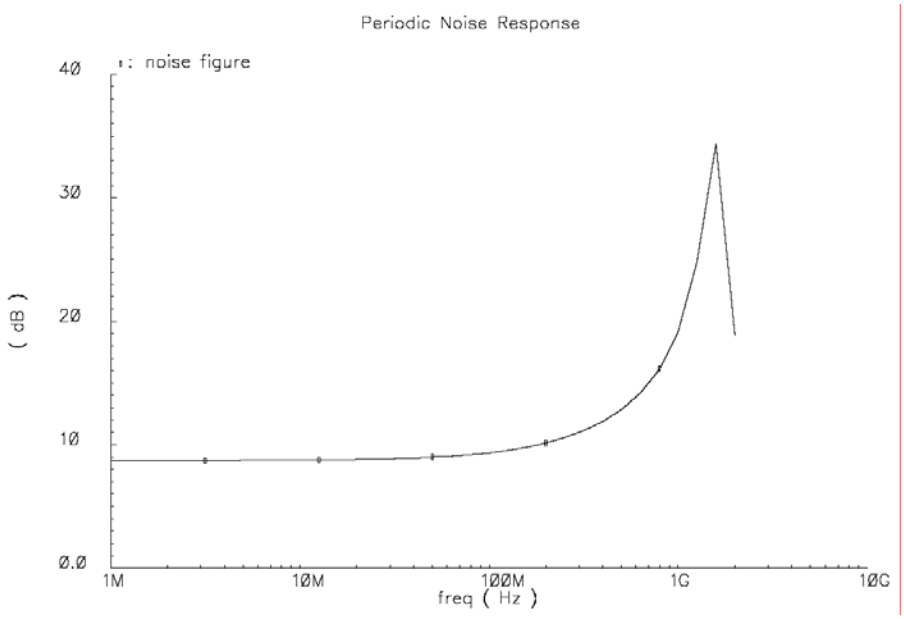


Figure 10.3 The noise figure of plan A.

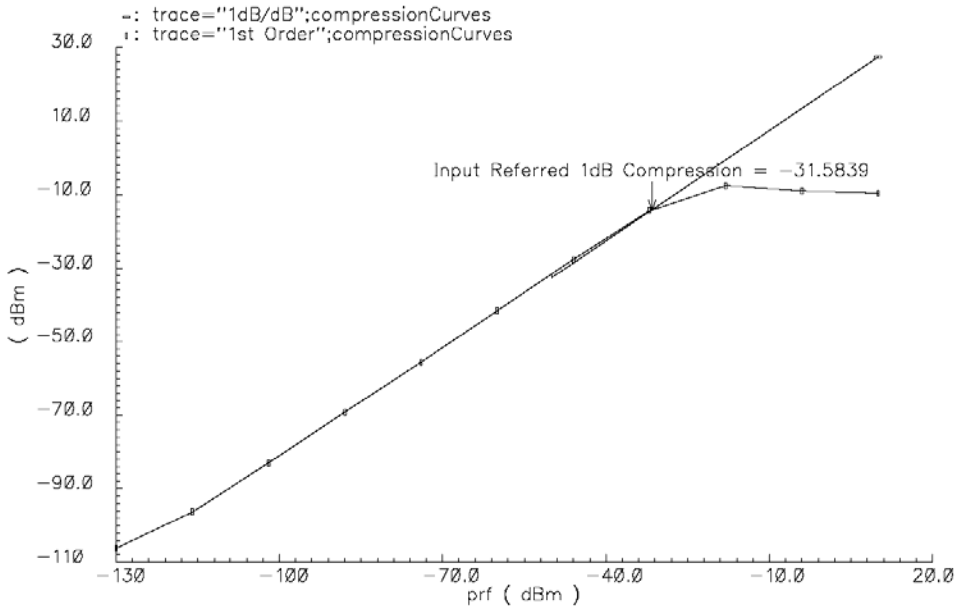


Figure 10.4 The 1-dB compression point of plan A.

Table 10.1 Summary of GPS receiver front-end sub-blocking circuits of plan A.

Parameter	Value
Supply Voltage	1 V
Power Consumption	1.9 mW
Voltage Gain	24.3 dB
NF	8.7 dB
1-dB Compression	-31.6 dBm

The summary of GPS receiver front-end sub blocking circuits of plan B is shown in Table 10.2.

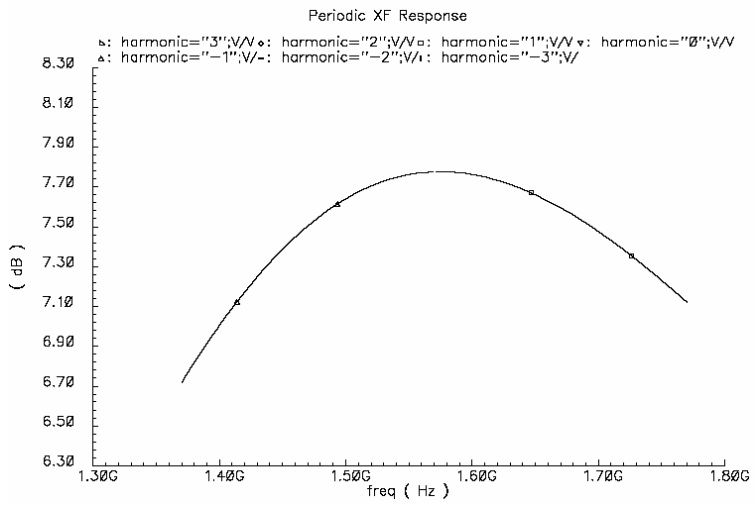


Figure 10.5 The gain of plan B.

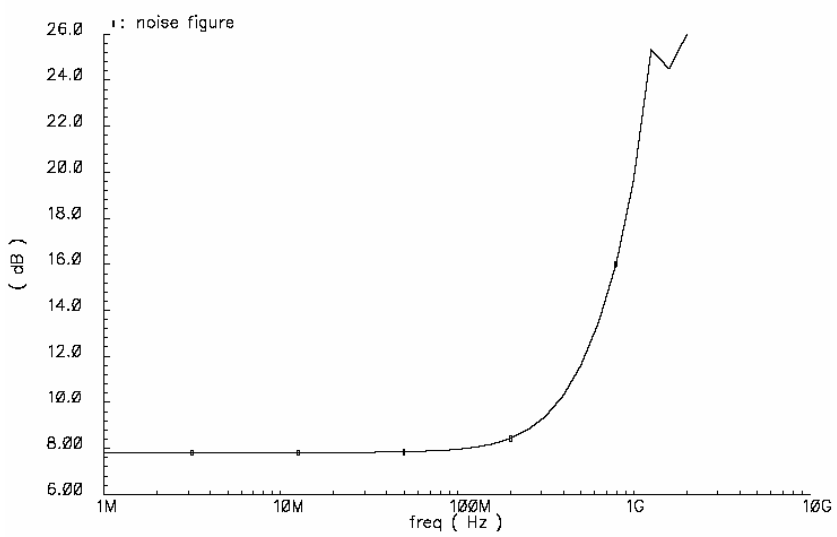


Figure 10.6 The NF of plan B.

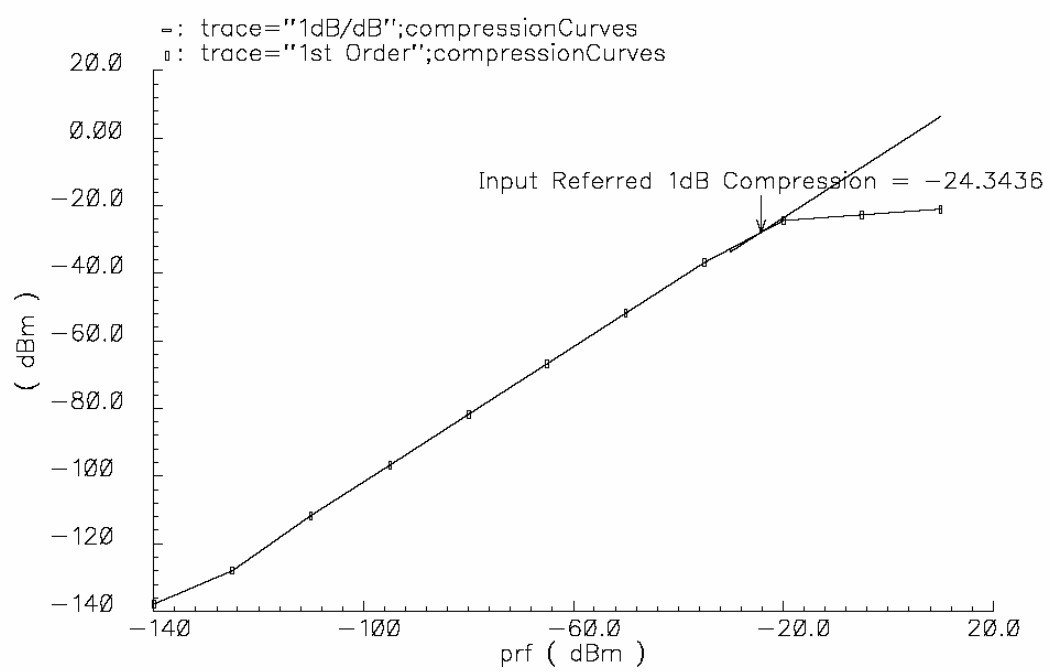


Figure 10.7 The 1-dB compression point of plan B.

Table 10.2 Summary of GPS receiver front-end sub-blocking circuits of plan B.

Parameter	Value
Supply Voltage	1 V
Power Consumption	1.5 mW
Voltage Gain	7.9 dB
NF	7.8 dB
1-dB Compression	-24.3 dBm

Comparing to the previous designs with the same constrains, the ultra-low power GPS receiver building block circuits in this research are a factor of 5 times better than the best design published resuts to date [42], as shown in Table 10.3. A new parameter,

gain/power, is introduced here to evaluate the performance improvement. In this work, 1 mW power can generate 2 to 6 times more gain.

Table 10.3 Comparison of GPS receiver sub-blocking circuit performance.

Authors	Technology	Supply Voltage (V)	Voltage Gain (dB)*	Power (mW)	Gain/power (dB/mW)	Year
[44]	0.5um CMOS	2.5	12	60	0.2	1998
[77]	0.25um CMOS	2	30	35	0.85	2002
[42]	0.18um CMOS	1.8	28	12	2.3	2005
Plan A	0.08um FinFET	1	24.3	1.9	12	After 2006
Plan B	0.08um FinFET	1	7.9	1.5	5.3	After 2006

10.2 Future Work

In the RF transceivers, passive inductors are frequently employed in various circuit blocks, such as in LNA, VCO and mixer, as well as matching network. The current trend is to integrate all passive and active devices on one chip, so that the cost of product can be reduced. However, most commercial RF communication products are still using external high-Q inductors. For low power design, the selection of integrated on-chip passive components or discrete off-chip ones plays an important role in receiver implementation. The following example explains the reason.

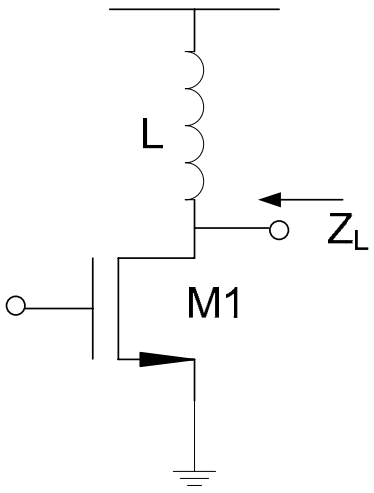


Figure 10.8 A typical common-source amplifier with inductor load.

For a simple inductor loaded common-source amplifiers, as shown in Figure 10.8, assume the inductor Q determines the output impedance of amplifier. The amplifier's voltage gain is expressed as,

$$A_v = -g_m Z_L \tag{10.1}$$

where Z_L is the equivalent output resistance in parallel with the inductor. It can be described as,

$$Z_L = Q\omega_0 L \tag{10.2}$$

when transistor M1 works in saturation region, which can be estimated as,

$$g_m = 2I_D/(V_{GS} - V_t) = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \tag{10.3}$$

Combine equation (10.1)-(10.3), we get

$$A_V = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}\cdot Q\omega_0 L \tag{10.4}$$

It can be observed that the required biasing current ($\sqrt{I_D}$) is inversely proportional to Q, in order to maintain a desired A_v. For instance, if the Q is increased from 5 (typical on-chip CMOS spiral inductor) to 50 (off-chip inductor), the biasing current is reduced by

100 times. If in both cases the same power supply are used the total power consumption will be reduced by 100 times too.

Based on the above analyses, both on-chip and off-chip inductors may be employed for power saving purpose. The monolithic spiral inductors are lossy and have quality factors less than 10 (for 3 metal layers process). And they also suffer from substrate eddy current losses, reduced self-resonant frequency, and the possible requirements for non-standard wafer processing. The performance of on-chip inductors is described in Chapter 3. For high power application, these low-Q circuits are compatible for broad band systems. In contrast, for narrowband wireless application, the high-Q passive devices could be used. The off-chip inductors may increase the total cost, but the cost can be traded off by some advantages of off-chip component integration. First, by moving the passive components from the chip onto the low cost substrate, the fabrication cost associated with large silicon chip area for the monolithic inductors can be saved. Second, removing the passive components from the lossy silicon substrate dramatically reduces the power consumption to achieve low power application. Therefore the high system cost associated with batteries is reduced.

The use of thin film bulk acoustic-wave resonators in transceiver circuits is one way for future exploration, as these components may help to reduce power consumption by eliminating the dependence of low Q on-chip passive devices.

Appendix A

Integrated Differential Inductors and Transformers

Differential inductors offer a greater Q factor and a broader range of operating frequency. Two different topologies of differential inductors are shown in Figure A.1.

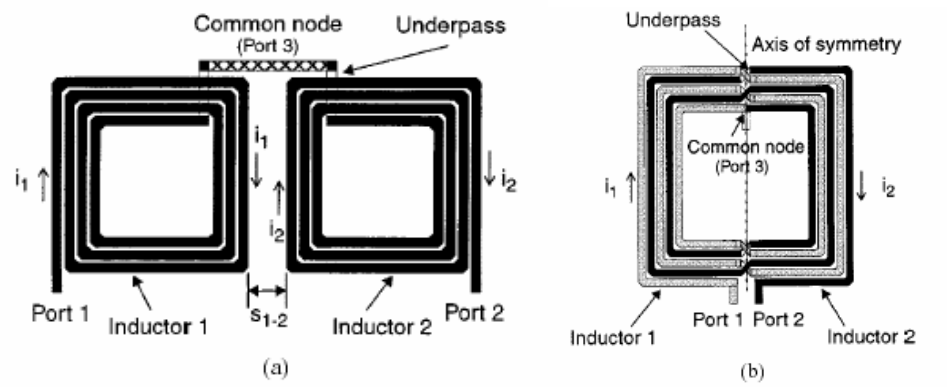
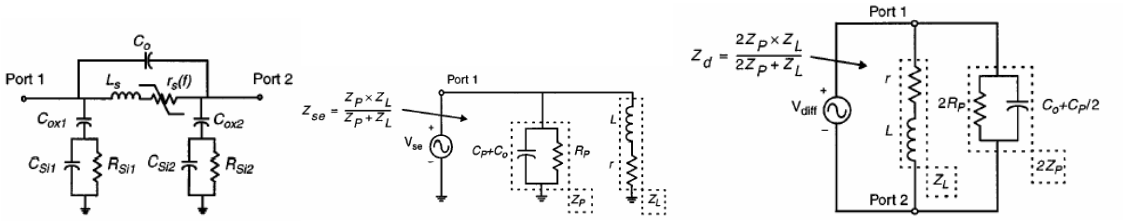


Figure A.1 Microstrip inductor physical layouts for differential inputs [78]. (a) Two asymmetric spiral conductors. (b) Symmetrical microstrip inductor.

The Advantages to employed differential inductor in the layout are: 1) the inductor quality factor (Q) is enhanced by ~50% compared with an equivalent single-ended configuration. 2) Increase self-resonance frequency.

The Figure A.2 has been used to illustrate the reason of how Q and self-resonance has been increase.



(a) (b) (c)

Figure A.2 (a) Lumped equivalent-circuit model of a microstrip inductor, and circuit equivalents for (b) single-ended (port 2 grounded) and (c) differential excitation.

The Figure A.2 (a) shows the lumped equivalent-circuit model of a microstrip inductor. For single-ended excitation, the inductor is connected as a one-port network, as shown in Figure A.2 (b).

Parallel LRC resonance frequency is given

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{A.1}$$

The Q at the resonance is

$$Q = \frac{R}{\sqrt{L/C}} \tag{A.2}$$

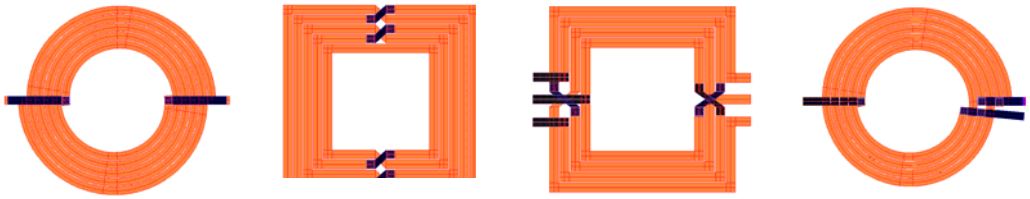
The ratio of the differential to the single-ended is

$$\frac{Q_d}{Q_{se}} = \frac{2R_P \| R_L}{R_P \| R_L} \sqrt{\frac{C_P/2 + C_0}{C_P + C_0}} \tag{A.3}$$

Monolithic microstrip transformers are used to perform coupling, biasing and filtering functions in RF front-end application. The coupling and biasing technique offers important advantages over the traditional stacked transistor biasing arrangement. Foremost among these is a reduction in required operating voltage. Additionally, the

topology allows the designer to easily adjust the bias current present in the input transistors, while bias currents in the other portions of the circuit are unaffected.

The layouts of differential inductors and transformers have been submitted. Below is a snap shot of the layout, as shown in Figure A.3.



(a) (b) (c) (d)

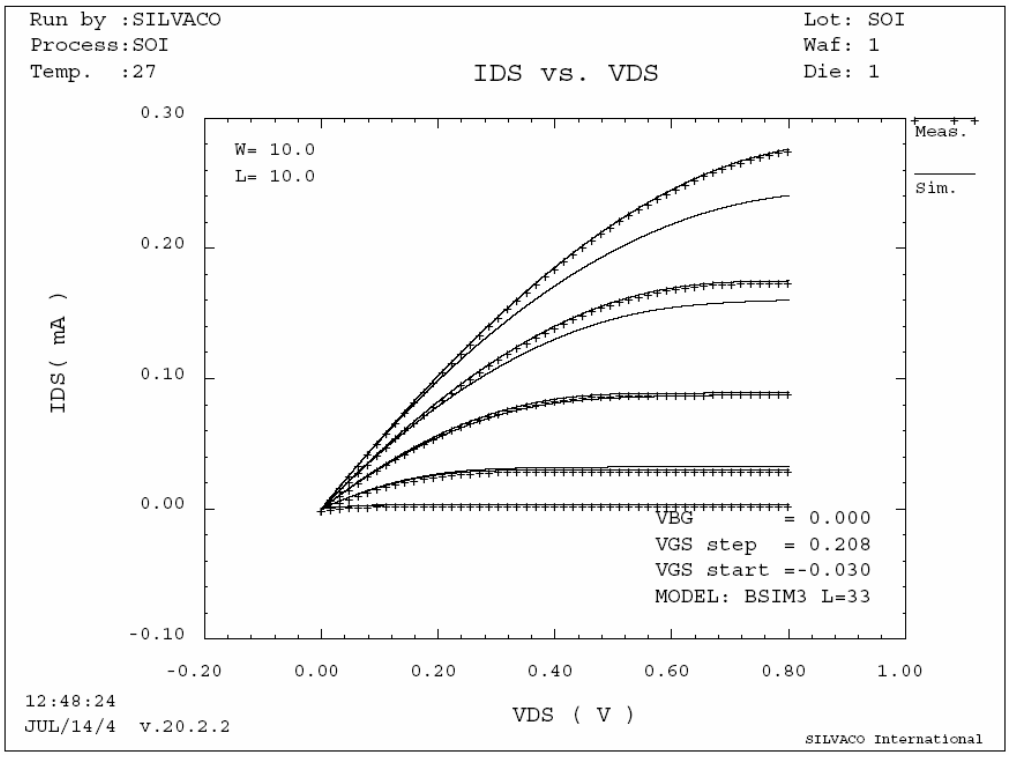
Figure A.3 The test structures of differential inductors and transformers [79]. (a) 1:1 transformer. (b) differential inductor. (c) Rabjon Balun. (d) 1:2.5 transformer.

Scalable physical models were constructed that predict the behavior of transformers, baluns, differential Inductors over a broad range of parameters: frequency from 0.1 to 15 GHz, widths from 15 μm to 35 μm, inner and outer radius ratios from 0.3 to 0.6, Q from 15 to 25 and High Self resonance 3 to 12 GHz.

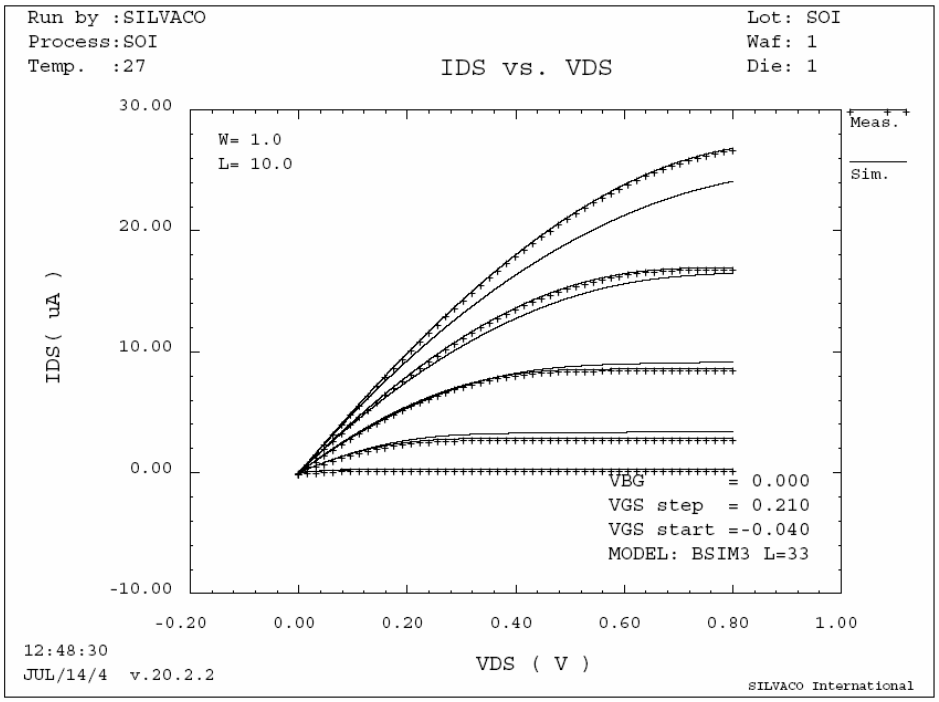
Appendix B

FinFET BSIMSOI Model Extraction

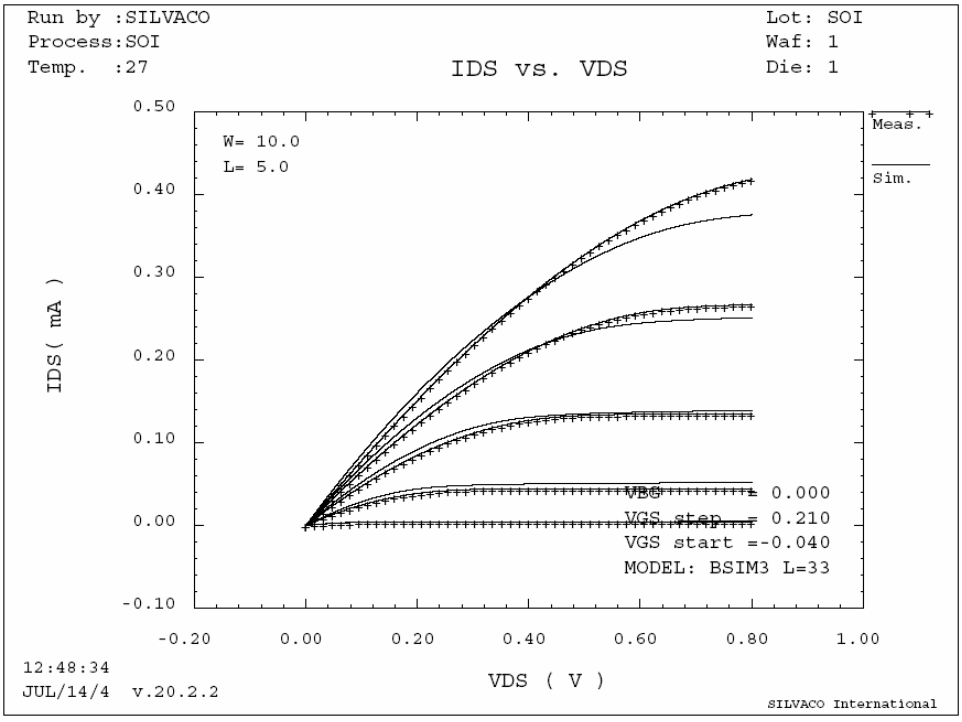
The measured the data and the simulated data compared as below. The model parameters are attached behind.



Max error 12.84%, Ave error 5.175%, RMS error 6.109%



Max error 18.98%, Ave error 6.579%, RMS error 8.111%



Max error 16.47%, Ave error 7.147%, RMS error

```
.MODEL FinFETN bsimsoi type=n (
+TNOM = 27 VERSION = 3 TOX = 2.8E-9
+TSI = 2E-8 TBOX = 4E-7 XJ = 1E-8
+NCH = 4.467859E14 NSUB = 2.589165E14 VTH0 = -0.098271
+K1 = 0.0744173 K2 = -2.098137E-3 K3 = 1E-3
+K3B = 22.2319452 K1W1 = 0 K1W2 = 1E-3
+KB1 = 1.438668E-3 W0 = 3.817179E-5 NLX = 1E-6
+DVT0W = 0 AGIDL = 0 BGIDL = 0
+NGIDL = 1.2 DVT1W = 0 DVT2W = -0.032
+DVT0 = 0.0099948 DVT1 = 0.9493336 DVT2 = -5.29687E-11
+VBM = -10 U0 = 347.1962197 UA = 2.35143E-10
+UB = 1.00001E-18 UC = -1E-10 VSAT = 1E4
+A0 = 0.1 AGS = 0.2739092 B0 = -1E-5
+B1 = -1E-7 FBJTII = 0 ESATII = 1E7
+SII0 = 0.5 SII1 = 0.1 SII2 = 0
+SIID = 0 KETA = 0 KETAS = 0
+RTH0 = 0 A1 = 0 A2 = 0.1
+RDSW = 3E3 PRWG = 0.1 PRWB = -5E-3
+WR = 1 WINT = -5.64676E-9 LINT = -3.009477E-7
+DWG = 1E-7 DWB = 9.770558E-8 DWBC = 0
+VOFF = -0.1794607 NFACTOR = 0.0106298 CIT = 0
+CDSCD = 0 CDSCB = 0 BETA0 = 0
+BETA1 = 0 BETA2 = 0.1 ETA0 = 1E-3
+ETAB = 0 PDIBLC1 = 1E-3 PDIBLC2 = 1E-5
+PDIBLCB = 0 PVAG = 0.01 DELTA = 0.0113262
+ALPHA0 = 0 VDSATII0= 0.9 MOBMOD = 1
```

+TII = 0 PRT = 0 UTE = -1.5

+KT1 = 0 KT1L = 0 LII = 0

+KT2 = 0 UA1 = 4.31E-9 UB1 = -7.61E-18

+UC1 = -5.6E-11 AT = 3.3E4 WL = 0

+WLN = 1 WW = 0 WWN = 1

+WWL = 0 LL = 0 LLN = 1

+LW = 0 LWN = 1 LWL = 0

+CAPMOD = 2 XPART = 0 CSDESW = 0

+SHMOD = 1 RBODY = 0 RBSH = 0

+NDIODE = 1 NTUN = 10 VTUN0 = 0

+ISBJT = 1E-6 NBJT = 1 LBJT0 = 2E-7

+VABJT = 10 AELY = 0 AHLI = 0

+ISDIF = 0 ISREC = 1E-5 ISTUN = 0

+XBJT = 1 XDIF = 1 XREC = 1

+XTUN = 0 NTRECF = 0 NTRECR = 0

+LN = 2E-6 NRECF0 = 2 NRECR0 = 10

+VREC0 = 0 ASD = 0.3 DLCB = 0

+DLBG = 0 DELVT = 0 FBODY = 1

+ACDE = 1 MOIN = 15 LDIF0 = 1

+NDIF = -1 SOIMOD = 0 VBSA = -2.846956E-8

+NOFFFD = 1 VOFFFD = 0 K1B = 0

+K2B = 0 DK2B = 0 DVBD0 = 0

+DVDB1 = 0 MOINFD = 1E3)

.END

Appendix C

Gate-Channel Capacitance Characteristics in Nano-Scale FinFET

C.1 C-V MEASUREMENT

A three-dimensional structure of FinFET is shown in Figure C.1, where the channels are formed in the vertical *Si* fins controlled by self-aligned dual gates. The FinFET under test was fabricated in SPAWAR System Center with the following parameters: T_{si}= 20 nm, H_{fin}= 50 nm, S_{fin}= 750 nm, T_{box}= 400 nm, t_{ox}= 2 nm, and L = 5 μm,. Each fin contributes two channels, which has an equivalent gate width of 100 nm. There are 200 fins in this FinFET, which give the gate width W= 20 μm.

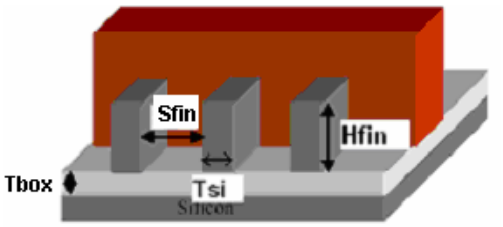


Figure C.1 The 3-D FinFET structure.

Figure C.2 illustrates the scheme of characterization with an n-channel FinFET. Measurements were performed on a Keithley 590 CV-meter and Keithley 4200 semiconductor characterization system. During the test the chip was put in a dark chamber, so that the interference from the light-generated carriers can be avoided. For the measurement at equilibrium the following procedures are followed: 1) after initially applying voltage to the device, allow an adequate hold time before recording the capacitance; 2) after each step of voltage change, allow an adequate delay time before recording the capacitance. In order to determine what are the adequate hold and delay times, a series of C-V curves have been generated in both sweep directions (inversion→accumulation and accumulation→ inversion). We optimized the hold and delay times until the pair of curves looks essentially the same, which indicates that it is independent of the sweep directions [80]. With this approach the hold time and delay time were determined to be 5 sec and 1.5 sec, respectively; and the sweep rate limit was set as 30mV/s.

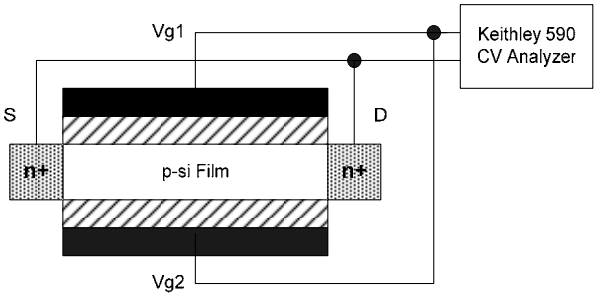


Figure C.2 Scheme of capacitance measurements for FinFET.

The gate voltage V_g was swept from -0.8V to 0.8V and back to -0.8V, while and $V_d = V_s = 0$ V. The high-frequency gate-to-channel capacitance (*hf*-C_{gc}) was measured at f = 100 KHz. Figure C.3 shows the *hf*-C_{gc} curve of an n-channel FinFET in equilibrium.

The capacitance reaches its maximum value when the channel is in strong inversion and exhibits a minimum in the accumulation region. Such a feature is different from the C-V characteristics of the conventional MOS capacitor structure. In an n-channel FinFET, the inversion minority carrier (electron) in the channel is connected electrically to a reservoir of carrier at the source and drain. Therefore, the minority carriers can response promptly to the ac gate signal. On the other hand, there is no such carrier reservoir for the majority carrier (holes), since the body of FinFET is floating [81].

For the non-equilibrium C-V measurement the gate voltage sweep rate has been increased from 60 mV/s to 140 mV/s. The C-V curves have basically the same shape as that in equilibrium, except the hysteresis in different sweep directions. With negative gate bias the C-V curve of planar single-gate SOI MOSFET changes slightly with different sweep rate [81], but this phenomenon is not observed in our measurement with FinFET.

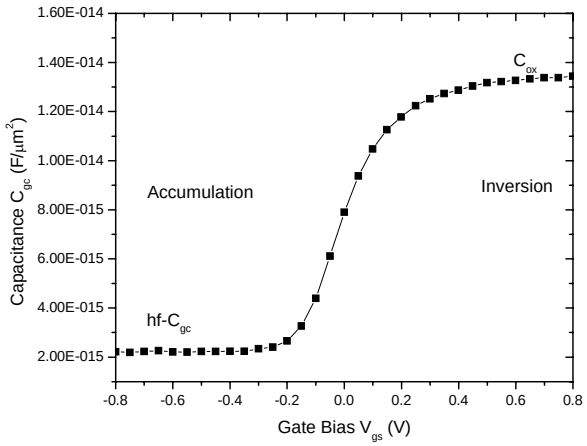


Figure C.3 Equilibrium high frequency C-V curve.

C.2 ANALYSIS AND DISCUSSION

In order to better understand the C-V characteristics, the band structure of the device should be investigated first. The C-V curve shows that at equilibrium (V_g = 0 V) it is between the inversion and accumulation regions. If the quantum confinement effect can be neglected, the band of the silicon of the FinFET can be described by the Poisson's equation with the depletion approximation [82]:

$$\frac{d^2\phi}{dx^2} = \frac{qN_a}{\varepsilon_{si}} \tag{C.1}$$

where ϕ stands for the potential and x is the distance from the symmetry plane at the center of the silicon fin, and the doping concentration, N_a, is assumed to be constant. Because the fin is very narrow, it is assumed that the entire fin is depleted and no neutral region remains. Solving the Poisson's equation with the symmetric boundary condition one can find the voltage profile as a parabola:

$$\phi(x) = \frac{qN_a}{2\varepsilon_{si}} x^2 + \phi_{s0} \tag{C.2}$$

where ϕ_{s0} is the potential at the center point. The voltage profile and the band diagram are shown in Figure C.4 (a) and (b), respectively. The electric field in the silicon fin is given by:

$$E(x) = \frac{-qN_a}{\varepsilon_{si}} x \tag{C.3}$$

When a positive gate voltage is applied, the band is pulled downwards. Before reaching the point of medium inversion

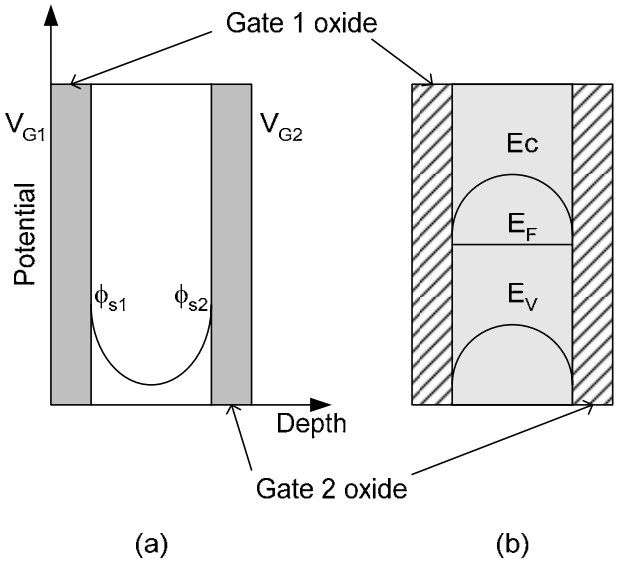


Figure C.4 (a) Potential profile and (b) band diagram of FinFET.

the shielding effect of the inversion charges can largely be neglected. In this case, the maximum electric field at the Si/SiO_2 interface (on silicon side) can be found as:

$$E_{\max} = E_{x=0.5t_{si}} = -\frac{qN_a}{2\varepsilon_{si}} t_{si} \tag{C.4}$$

Due to the limited doping concentration in the polysilicon gate, a very thin depletion region also exists there. If the trapped charges in the oxide and at the interface can also be neglected, the maximum electric field in the polysilicon gate is the same as the one derived in Eq. (4). Therefore, we can figure out the width of the depletion region in the gate as the following:

$$d_{poly} = \frac{N_a}{N_d} \frac{t_{si}}{2} \tag{C.5}$$

where N_d and N_a are the doping concentrations of the polysilicon gate and the silicon fin, respectively. The former is around 10^{20} cm^{-3}, and the latter is less than 10^{18} cm^{-3}. Therefore, the depletion region is limited to one monolayer of silicon atoms in the sample

under test. However, this approach is only an approximation, because the charge concentration at the Si/SiO_2 interface is very complicated.

In a simplified MOS capacitor model the gate capacitance reaches its maximum value with large forward gate bias, which should be ideally equal to the oxide capacitance. In this way, the oxide thickness can be easily extracted from the C-V curve. In our FinFET sample the extracted equivalent oxide thickness is 2.4 nm, which is different from the parameter (2 nm) listed in section I. Therefore, the gate depletion effect must be taken into account, and the depletion layer can be considered as an additional series capacitance [83].

The C-V measurement is a valuable diagnostic tool in MOSFET characterization. The analysis above shows that it can be employed to determine the oxide thickness. However, charges can be trapped in the gate oxide and at the Si/SiO_2 interface, which can complicate the extraction process.

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In this research, design approaches and methodologies were presented to realize the ultra-low power RF receiver front-end circuits. Moderate inversion operation was explored as a possible method of reducing power consumption along with the use of low supply voltage. The research is firstly concentrated on passive and active devices modeling. One of the most commonly used passive devices is on-chip inductor. On-chip spiral inductor model was developed firstly. Compared to the model developed by others, this model can predict the behavior of the inductors with different structural parameters over a board frequency range (from 0.1 to 10 GHz). Then the SOI varactor model was developed based on our measurement and extraction.

Besides the passive devices modeling, a new most promising MOSFET candidate, FinFET, was characterized at GHz frequency range. Based on the measurement results, we found the FinFET transistors did have superior performance over bulk-Si CMOS technology. And an RF circuit model of FinFET was developed followed that, which was published in *Electronics Letters*. To my best knowledge, this was the first RF FinFET model published world wide at that time. It provides the basic idea about how to model this new structure MOSFET.

Based on the passive and active device models developed, Global Positioning System (GPS) receiver front end circuits were designed and measured. Comparing to the previous designs with the same constrains, the ultra-low power GPS receiver building block circuits in this research have much less power consumption than the best design published before.

ADVISOR'S APPROVAL: _____