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THEORY, DESIGN, AND SIMULATION OF LINA: A PATH FORWARD FOR QCA-TYPE NANOELECTRONICS

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THEORY, DESIGN, AND SIMULATION OF LINA: A PATH FORWARD FOR QCA-TYPE NANOELECTRONICS

A DISSERTATION APPROVED FOR THE
SCHOOL OF ELECTRICAL AND COMPUTER ENGINEERING

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To Tammy, Luke, Jacob, Angel, and Sunshine –

my beautiful storm, solid rock, warm light, free river, and green valley

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Table of Contents

List of Tables

List of Figures

Abstract

The past 50 years have seen exponential advances in digital integrated circuit technologies which has facilitated an explosion of uses and functionality. Although this rate (generally referred to as “Moore’s Law”) cannot be sustained indefinitely, significant advances will remain possible even after current technologies reach fundamental limits. However if these further advances are to be realized, nanoelectronics designs must be developed that provide significant improvements over, the currently-utilized, complementary metal-oxide semiconductor (CMOS) transistor based integrated circuits. One promising nanoelectronics paradigm to fulfill this function is Quantum-dot Cellular Automata (QCA). QCA provides the possibility of THz switching, molecular scaling, and provides particular applicability for advanced logical constructs such as reversible logic and systolic arrays within the paradigm. These attributes make QCA an exciting prospect; however, current fabrication technology does not exist which allows for the fabrication of reliable electronic QCA circuits which operate at room-temperature. Furthermore, a plausible path to fabrication of circuitry on the very large scale integration (VLSI) level with QCA does not currently exist. This has caused doubts to the viability of the paradigm and questions to its future as a suitable nanoelectronic replacement to CMOS. In order to resolve these issues, research was conducted into a new design which could utilize key attributes of QCA while also providing a means

for near-term fabrication of reliable room-temperature circuits and a path forward for VLSI circuits.

The result of this research, presented in this dissertation, is the Lattice-based Integrated-signal Nanocellular Automata (LINA) nanoelectronics paradigm. LINA designs are based on QCA and provide the same basic functionality as traditional QCA. LINA also retains the key attributes of THz switching, scalability to the molecular level, and ability to utilize advanced logical constructs which are crucial to the QCA proposals. However, LINA designs also provide significant improvements over traditional QCA. For example, the continuous correction of faults, due to LINA's integrated-signal approach, provides reliability improvements to enable room-temperature operation with cells which are potentially up to 20nm and fault tolerance to layout, patterning, stray-charge, and stuck-at-faults. In terms of fabrication, LINA's lattice-based structure allows precise relative placement through the use of self-assembly techniques seen in current nanoparticle research. LINA also allows for large enough wire and logic structures to enable use of widely available photo-lithographical patterning technologies. These aspects of the LINA designs, along with power, timing, and clocking results, have been verified through the use of new and/or modified simulation tools specifically developed for this purpose. To summarize, the LINA designs and results, presented in this dissertation, provide a path to realization of QCA-type VLSI nanoelectronic circuitry. Furthermore, they offer a renewed viability of the paradigm to replace CMOS and advance computing technologies beyond the next decade.

Chapter 1

Introduction

Few would doubt the importance of the integrated circuit (IC) to the societies of the modern world. They have permeated nearly every aspect of our everyday lives and enabled unquestioned creativity, unparalleled togetherness, and the instantaneous spread of information throughout the globe. The man given most of the credit for the invention of the IC is Jack Kilby, who won the Nobel Prize for physics in 2000 for his work developing the first IC at Texas Instruments in 1958 [1]. Kilby's original ICs consisted of a single phase-shift oscillator and a digital flip flop circuit whose functionality was well known and not at all revolutionary. What was revolutionary, however, was that the logical components, passive elements, and interconnection wiring were constructed and integrated together using only a single piece of germanium. This change removed the expensive, time-consuming, and unreliable process of hand wiring and soldiering of several individual components to achieve the desired circuit function [2]. It also allowed the IC to be rapidly and effectively scaled, both up in the number of components integrated in a device (termed integration level scaling), and down in the size of the components and interconnections (termed size scaling).

These scaling advances allowed for not only the addition of functionality and efficiencies into ICs but also for decreased power per circuit element and increased circuit speed due to the underlying nature of the physics of the host semiconductors.

It could be argued, very effectively, that the ability to be scaled has been the driving force in the success of the integrated circuit, giving rise to an exponential increase in computing performance over the past 50 years. This success can clearly be seen in microprocessor ICs which have grown in complexity from around 2,300 transistors in the early 1970s to currently being distributed with billions of transistors integrated on a piece of silicon only a few square centimeters in area while running at clock speeds which allow several billion calculations to be performed per second.

However, size scaling of the current processor IC technology, complementary metal-oxide semiconductor (CMOS), is rapidly approaching practical, if not fundamental, limits [3]. This is due to the size of today's CMOS transistors which have gate widths in the lower tens of nanometers. At this size scale, quantum mechanical effects, such as tunneling, begin to affect device behavior. In fact, circuit designers are already being plagued by these small scale effects as limited per element power consumption gains are no longer able to support large increases in circuit clock speeds. In order to offset these challenges, designers are turning to more parallel multi-core designs to continue the increase in IC performance, but they are most assuredly a harbinger of other, more fundamental, difficulties to come. Therefore, if the pace of progress seen in computing over the past 50 years is to be maintained, new technologies must be developed to supplement and eventually replace CMOS transistor-based designs and provide a paradigm which can continue the scaling of electronic circuit elements into the quantum and molecular regimes.

Nanoelectronics, named after the nanometer dimensions of the field's electronic elements, contain the emerging IC implementation paradigms from which will come the next generation of computing technologies. While CMOS is itself delving into the nanometer realm for size dimensions, CMOS is not a nanoelectronics paradigm. Instead, current nanoelectronics paradigms include single electron transistors (SET) [4, 5, 6, 7], Superconducting electronics [8, 9, 10], carbon nanotube (CNT) [11, 12, 13, 14], nanowire and nano-ribbon transistors [15, 16, 17, 18], resonant tunneling devices [19, 20], spintronics [21, 22, 23, 24], and Quantum-Dot Cellular Automata (QCA) [25, 26, 27, 28]. Many of these technologies simply offer the potential to extend the life of CMOS and expand more traditional circuit design techniques to smaller scales. However, this extension will only delay the inevitable necessity of a completely new processing paradigm. In Figure 1-1, a projection of roles and timeline for several of these nanoelectronics proposals based on current industry projections [3] is shown.

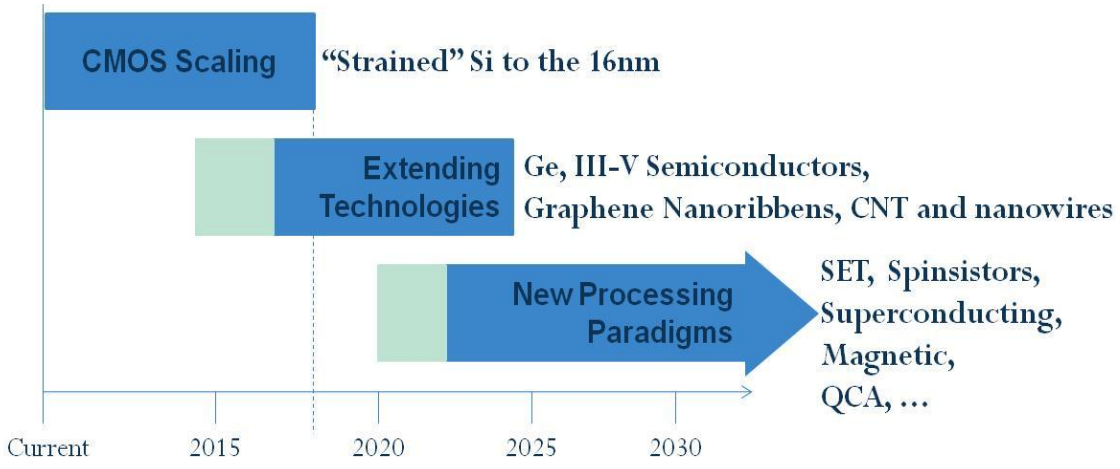


Figure 1-1. Outlook of Computing Technologies

There are certain attributes which make nanoelectronics proposals suitable candidates to replace CMOS electronics. Specifically, the particular proposal must offer a technology which exceeds current and projected CMOS abilities in areas such as: clock speed, power requirements, parallel structure, circuit area, and/or circuit robustness. Many proposals are able to exceed the abilities of current technologies in some areas, but fall short in others. For example, single electron transistors can be made much smaller than current CMOS transistors (potentially down to a single nanometer sized molecular component). Additionally, their power requirements are very low compared to CMOS. However, robust operation at room temperature has been very difficult to achieve especially at the very large scale integration (VLSI) level.

Other paradigms have similar advantages and disadvantages. For instance, QCA offers molecular scalability and low power, similar to the SET, along with the potential of THz switching speeds and an inherently parallel circuit structure. Further exploration of the potential of the QCA paradigm reveals the hope for revolutionary advancements in logic design and computing circuitry through constructs such as reversible computing [29] and/or reconfigurable systolic architectures [30]. These attributes along with the advancements in size, speed, and power have attracted many researchers to QCA, making it one of the most theoretically well-developed nanoelectronics paradigms. However, QCA have also been hampered by the inability to provide robust large scale circuits in a room temperature environment; a challenge that if left unsolved will undermine

the promising potential of QCA and the confidence of the nanoelectronics community in the paradigm.

1.1 Advancement and impact of this work

Major advancements in two areas of research must be achieved if the QCA paradigm is able to fulfill its promise as a nanoelectronic replacement to CMOS. First, an architecture which allows for robust room-temperature operation of QCA must be developed; and second, that architecture must be amenable to currently available or near term fabrication technologies. Too often, researchers in the QCA field have overlooked these two challenges and resorted to the traditional QCA cellular structure and architecture paradigm. The effect of this lack of attention has been the steady decline in confidence of the electronics community as to the theoretical predictions made for QCA [31, 32, 33][1], and thus the paradigm itself. In this work, we tackle these two pressing challenges and produce a new design which retains the promising potential in logic design methods and performance, and also provides viable implementation strategies which fit with current and near term technologies. The new design is called the Lattice-based Integrated-signal Nanocellular Automata (LINA) (example shown in Figure 1-2). LINA is a design strategy and circuit architecture that is a variant of the QCA paradigm. However, it is built around a lattice-based structure which allows for common self-assembly methods to be utilized in the deposition and

[1] These references highlight theoretical disagreements between physicists and system designers. Lack of fabrication methods has served to facilitate these disagreements and doubts.

placement phase of circuit construction. Additionally, LINA provides a dramatic increase in reliability (for a constant cell size) over traditional QCA designs by integrating several “signals” of information together in a process that continually corrects faults. The increase in reliability allows for larger cells and spacings to be used to fabricate circuitry for room-temperature operation and additional opportunities for currently available materials to be used as circuit elements. Additionally, the larger footprint of the logical and communicative elements should allow for traditional lithographic patterning methods to be used for the fabrication of LINA circuitry allowing utilization of current VLSI technologies and fabrication facilities. The LINA designs also allow for continued scaling of circuitry to the molecular level as technologies improve.

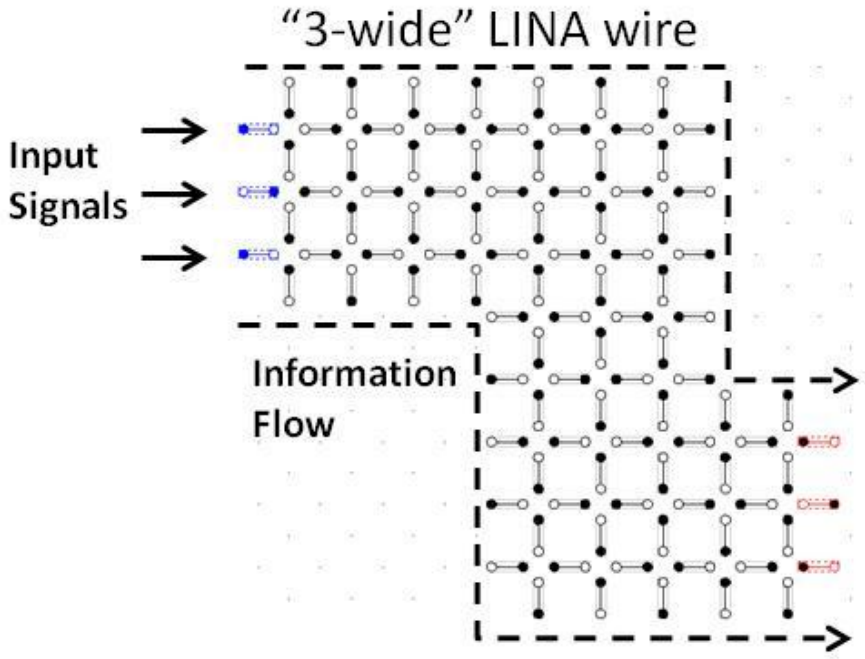


Figure 1-2. Lattice-based Integrated-signal Nanocellular Automata (LINA) wire design structure

The theories and structures which will be presented in this work have been verified using physics based simulation methods which were originally produced for traditional QCA and have been modified to also be applicable to LINA. The software provides data on timing, logical function, power, reliability, and other physical parameters whose results were checked against other commonly available simulation tools. It also provides a design tool for creating logical elements and circuitry in the LINA design framework.

In summary, QCA is one of the most theoretically well-developed nanoelectronics design paradigms. Its challenges have been with the inability to fabricate reliable room-temperature large scale circuitry. The results of the LINA research have the potential to overcome these challenges and alter the course of QCA nanoelectronics by making QCA designs more applicable to existing materials and technologies. This could then position QCA as one of the favorite candidates to replace CMOS based integrated circuitry in the coming decades and usher in a new era of electronics and computing.

1.2 Organization

This dissertation is organized as follows. Background material for the QCA paradigm is presented in Chapter 2. 2D 2-Dot QCA designs, which are the basic building block of LINA, are presented in Chapter 3. The details of the simulation engines used in the development of the 2D 2-dot QCA and LINA are given in Chapter 4. Chapter 5 details the new LINA designs and methods and presents simulation results which provide critical evidence to support its suitability. Chapter 6 provides further analysis for LINA and two LINA design

examples. The dissertation is then concluded with Chapter 7, which provides summaries and an outlook to future research on LINA.

Chapter 2

Background Material

Before a thorough discussion of LINA theory and designs can be presented, it is important that traditional QCA principles of structure, design, and fabrication must be understood. This is because LINA are based on many of these QCA principles. Additionally, a great deal of the published theoretical research is applicable to both paradigms. Therefore, this chapter provides the material necessary to this understanding, beginning with an introduction to cellular automata concepts and QCA basics. This is followed by current QCA implementation technologies and theory which provide the starting point to further advances provided in this dissertation. More complex QCA topics such as clocking and advanced logical concepts will also be discussed due to their criticality to the LINA architecture. Finally, the chapter ends with a discussion on analysis of important QCA properties which provide the motivation for further exploration of QCA as a nanoelectronics replacement for CMOS ICs.

2.1 Quantum-dot cellular automata (QCA) Basics

2.1.1 Cellular Automata (CA)

Cellular Automata (CA), first proposed by von Neumann [34], are generally n-dimensional fully populated arrays of identical cells, which may be in any one of a set of finite states. Each of these cells updates their states at discrete time intervals based on a global evolution function that is typically dependent on the states of a set of neighboring cells. Because the CA computation model obeys

physical principles of locality and invariance to shifts in time and space, many scientists have suggested a link between CA and the physics of the quantum world [35]. Additionally, the fact that many molecular structures have natural attributes demonstrating CA interaction suggests that CA may be ideal computational elements for nanoelectronics.

This suggestion is further substantiated by the fact that CA can achieve complexity and even logical completeness with very simple structure and evolution functions. This fact is exemplified in research by Wolfram, who classified and proved that elementary CA, (which are bi-state, 1-D, fully populated arrays) achieve complexity by means of a specific set of rules (here another name for the evolution function), such as rule 110 [36], which can be seen in Figure 2-1.

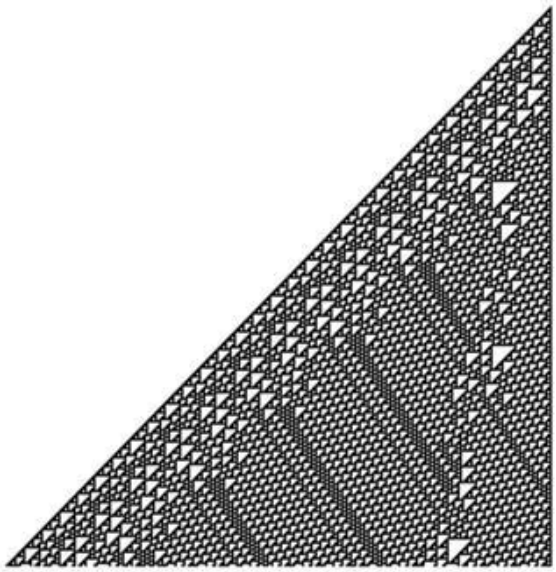


Figure 2-1. Rule 110 CA - The figure is a graphical representation of the evolution of a 1-D array of two-state cells (white depicting a "0" state and black depicting a "1" state). The CA begins with a single "1" surrounded by all "0"s which is the top of the triangle. Each row of the figure is a discrete time step of the evolution of the cells beginning at the top and progressing down [36].

2.1.2 QCA as CA

The QCA paradigm deviates from conventional CA in that QCA achieve logical completeness and complexity by selectively patterning (meaning adding or deleting) cells based in a 2-D grid and actively driving certain input cells[2]. Because of this, QCA cell patterns more closely resemble the form and function of traditional logical circuits compared to other CA types. This provides benefits in circuit design techniques but also limits inherent advantages of the QCA paradigm, such as parallelism.

QCA also deviate in that the cells' evolution functions are not based on the state of the neighboring cells at the previous time step as in conventional CA, but instead on the least energy configuration of the entire system at that time step. This means that QCA are not inherently sequential, instead the input cells are used to explicitly set the cell states of the remaining cells. In order to make QCA sequential, clocking schemes are applied to effectively lock cell states of certain neighboring cells in a cyclic fashion. This provides a more conventional CA evolution function to the QCA circuit states.

The evolution functions for both clocked and unclocked QCA are based on the summation of the electromagnetic interaction of neighboring cells. The strength and polarization of this interaction has factors of relative placement, cellular geometry, and distance; and, due to the structure of QCA cells, essentially limits the cell interaction neighborhood to a radius of two or three cell spacings.

[2] Input cells thus have evolution functions that are not dependent on neighboring cells.

Additionally, the bipolar nature of the electromagnetic interaction produces QCA cells which are two-state, allowing for simplicity, robustness, and even logical gain.

The evolution function produces a ferromagnetic[3] type of interaction for cells directly horizontal or vertically positioned to each other. Cells which are positioned diagonally relative to each other tend to produce an anti-ferromagnetic type of interaction. This produces a logical majority voter function for cells at the ferromagnetic position with similar distances, and a logical minority function for cells at the anti-ferromagnetic positions with similar distances (shown graphically in Figure 2-2). This inherent property of QCA will become a critical piece to allow logic and communication in the QCA computing architecture.

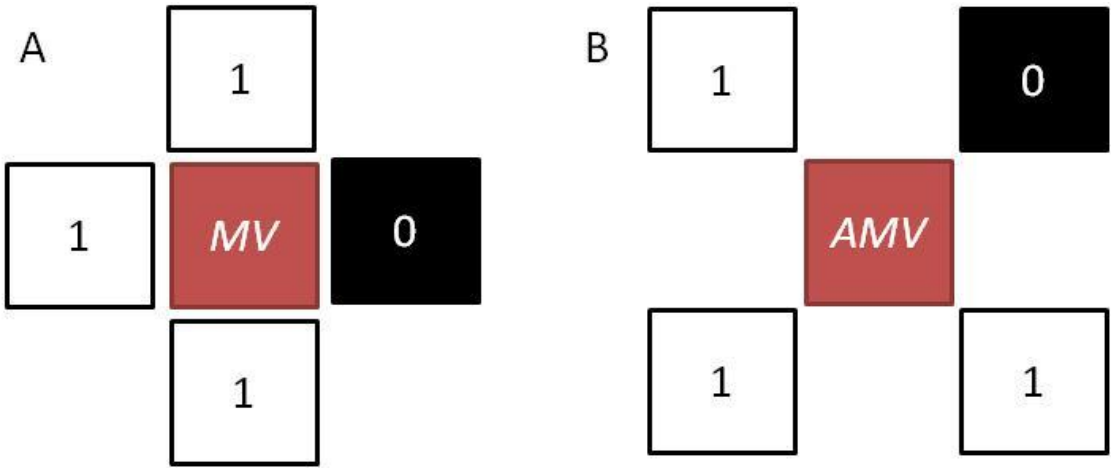


Figure 2-2. A. Configuration of cells which produce a majority voter (MV) logical function. B. Configuration of QCA cells which produces a minority (anti-majority) voter (AMV) function.

[3] Ferromagnetic is in the sense of an Ising model and does not necessarily mean magnetism

2.2 QCA Basics

2.2.1 QCA Cell Structure

Standard QCA cells are, at their most basic, a configuration of charge containers which enable the localization of a fixed number of free electrons in a way which produces a two state CA. The first “model” QCA cells were theoretical structures, proposed by Lent et al. [25], containing five quantum dots arranged in the manner shown in Figure 2-3. These quantum dots act as the charge containers for the localization of two free electrons, which because of Coulombic repulsion prefer to occupy diagonal corner quantum dot sites. Each quantum dot is electrically separated from the other dots by a potential barrier generated by the electrical properties of the surrounding material. Classically, after an electron falls into one of these dots and relaxes sufficiently, it cannot escape until it is given suitable energy to overcome the dot’s barriers. However, quantum mechanical principles allow, at some non-zero probability, electrons to travel, or “tunnel”, from one dot to another without the application of extra energy. This occurs with a frequency and likelihood dependent on properties such as the electron’s energy, applied force to the electron, and the potential energy barrier height the quantum dot provides. These properties must be precisely controlled in QCA cells allowing the design of specifically placed paths, or tunnel junctions, between specific dots internal to a single cell but not between dots of two separate cells.

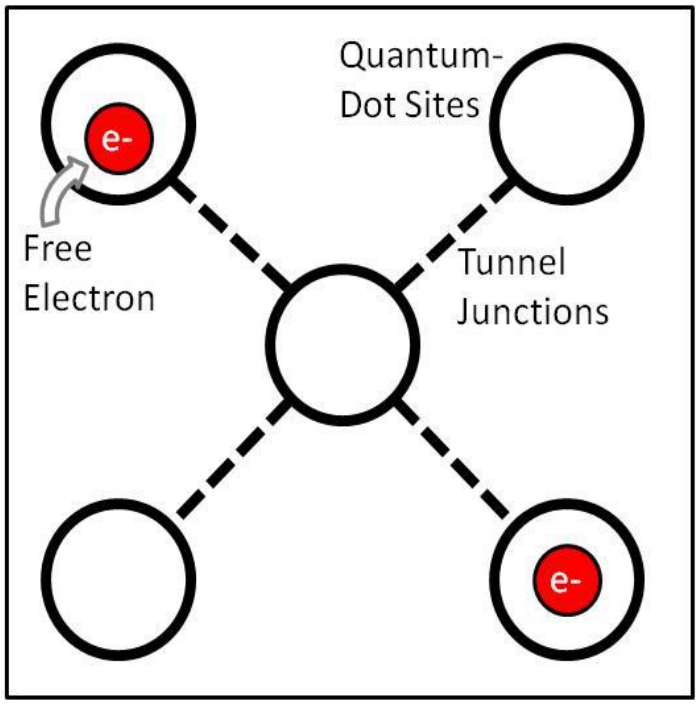


Figure 2-3. Original QCA Cell - Here shown with two free electrons completely localized on quantum dot sites.

2.2.2 Theoretical Development of a model QCA cell

The theoretical development of a physical model of a QCA cell begins with a graphical schematic of what was originally called the "standard" QCA cell [25, 37] (shown in Figure 2-4). The standard cell contains quantum dot sites which are labeled from 0 to 4, and are connected with tunnel junctions which are labeled based on the sites which they connect. It is assumed that the barriers to tunneling for any path not shown in the model are so large to effectively eliminate tunneling in them. A standard distance of a is used to denote the base measurement of this cell as given a one could determine any distance in the cell based on standard geometry.

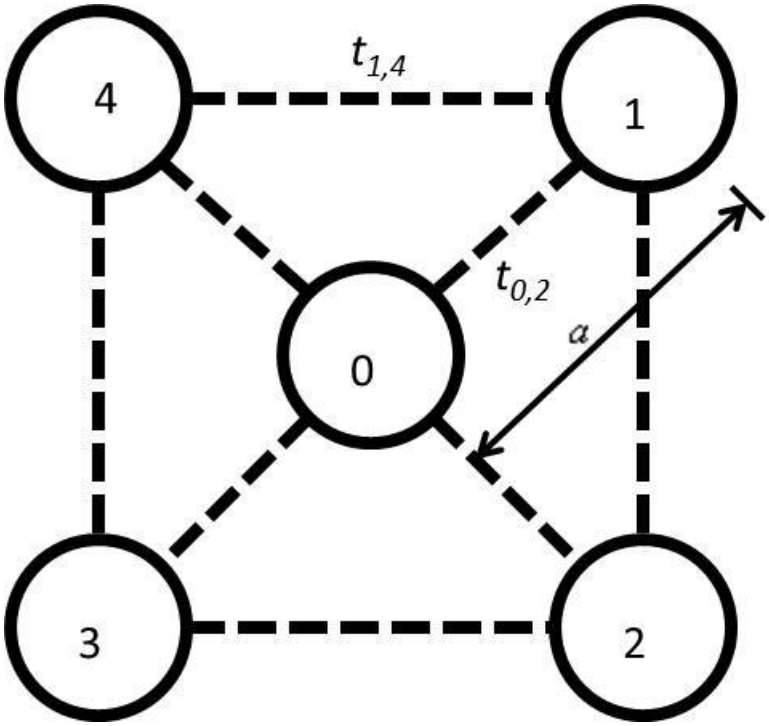


Figure 2-4. Graphical schematic of the original "standard" QCA cells with numbered quantum dot sites, tunnel junctions, and the distance measure "a"

This graphical model allows construction of a model Hamiltonian for the cell. A Hubbard-type Hamiltonian was chosen and any internal degrees of freedom to the dots of the cell were ignored. The Hamiltonian for the cell is:

$$H_0^{Cell} = \sum_{i,\sigma} E_o\, \hat{n}_{i,\sigma} + \sum_{i>j,\sigma} t_{i,j}(\hat{a}_{i,\sigma}^{\dagger}\hat{a}_{j,\sigma} + \hat{a}_{j,\sigma}^{\dagger}\hat{a}_{i,\sigma}) + \sum_{i} E_Q \hat{n}_{i,\downarrow}\hat{n}_{i,\uparrow} + \sum_{i>j,\sigma,\sigma'} V_Q \frac{\hat{n}_{i,\sigma}\hat{n}_{j,\sigma'}}{(R_i - R_i)} \quad \textbf{(2.1)}$$

In (2.1) the second quantization notation is used where $\hat{a}_{i,\sigma}^{\dagger}(\hat{a}_{i,\sigma})$ creates (annihilates) an electron at site i with spin σ. The number operator for site i with spin σ is $\hat{n}_{i,\sigma} = \hat{a}_{i,\sigma}^{\dagger}\hat{a}_{i,\sigma}$. The first term of (2.1) is the energy, E_0, associated with an electron confined on the i^{th} site. The second term is the tunneling energy

between sites i and j where $t_{i,j} = t$ for neighboring sites and $t_{i,j} = 0$ for antipodal sites. The third term is the energy cost associated with confining two electrons on the same dot and the fourth term is the Coulombic interaction between electrons at different sites. To find the stationary states of the model cell, the time-independent Schrödinger equation ((2.2) must be solved.

$$\widehat{H}^{Cell}|\psi_i\rangle = E_i|\psi_i\rangle \quad \textbf{(2.2)}$$

In (2.2), $|\psi_i\rangle$ is the i^{th} eigenstate of the Hamiltonian and E_i is the associated eigenvalue. These eigenstates are found using the many-particle site-ket basis for the five sites and two electrons of opposite spins such as seen in (2.3):

$$\begin{aligned} |\psi_0\rangle &= \left|\begin{matrix}0\ 0\ 0\ 0\ 1\\ 0\ 0\ 0\ 0\ 1\end{matrix}\right\rangle, \\ |\psi_1\rangle &= \left|\begin{matrix}0\ 0\ 0\ 0\ 1\\ 0\ 0\ 0\ 1\ 0\end{matrix}\right\rangle, \\ &\ldots, \\ |\psi_{25}\rangle &= \left|\begin{matrix}1\ 0\ 0\ 0\ 0\\ 1\ 0\ 0\ 0\ 0\end{matrix}\right\rangle, \end{aligned} \quad \textbf{(2.3)}$$

where the columns correspond to the sites and the rows to the spins (with the upper row being spin up and the lower row spin down).

Using this basis, the Hamiltonian matrix is calculated numerically as in (2.4)

$$H_{i,j} = \langle\phi_i|\widehat{H}\phi_j\rangle \quad \textbf{(2.4)}$$

and diagonalization of this 25x25 matrix leads to the calculation of the ground states of this model system.

The ground states of the model are the two preferred configurations shown in Figure 2-5 for the case of high tunneling barriers and essentially localized electrons. Tunneling barriers of this type create difficulty in fast switching which is essential in digital systems. However, as tunneling barriers are lowered the localization on the sites is reduced and the electron wavefunctions become spread out amongst the sites making the polarization of the cell weak. This is also an unsuitable situation for digital electronics due to the resultant indeterminate nature of the logic state in this situation. Therefore, a balance must be found to optimize among these two considerations.

In order to quantify the polarization of the cell in regards to the two logic states, (2.5) defines a value P (polarization) which equals -1 for the completely localized logic "0" case and +1 for the completely localized logic "1" case.

$$P \equiv \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_0 + \rho_1 + \rho_2 + \rho_3 + \rho_4} \quad \textbf{(2.5)}$$

In (2.5), ρ_i is the expectation value for the number operator for site i.

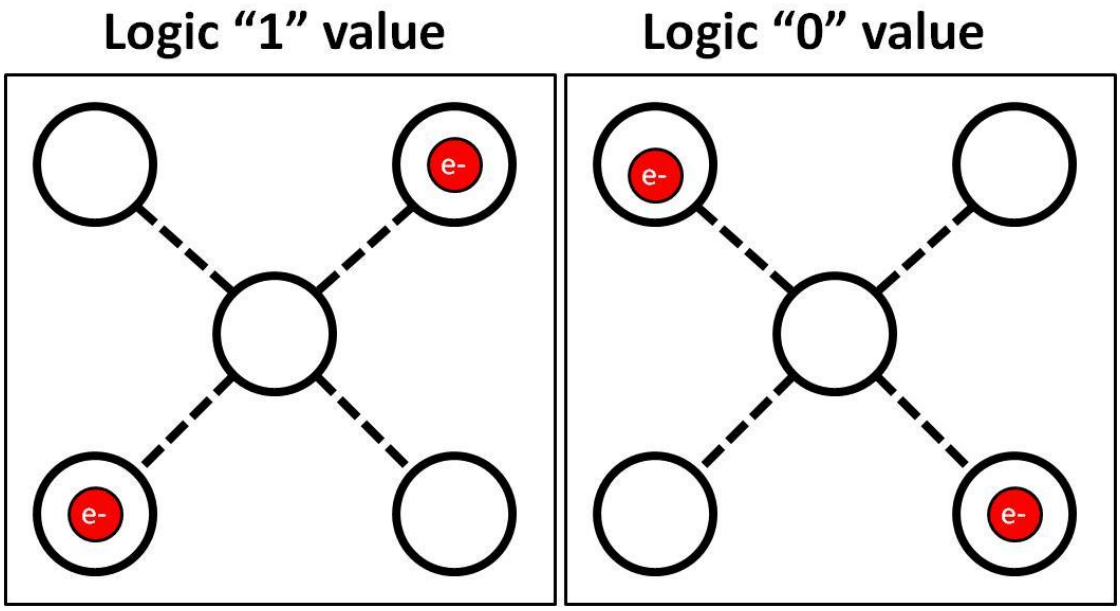


Figure 2-5. Two ground state electron configurations of the model QCA cells and the logical values associated with them.

2.2.3 Other cell configurations

Other types of QCA cells have been proposed in literature and are utilized in QCA designs including cells with four quantum dots, six quantum dots, four quantum dots rotated by 45 degrees with respect to corners of the cell, and cells composed of two dot half-cells. These different cellular configurations, which are shown in Figure 2-6, have slightly different advantages or functions than the model cell. Of particular importance, is the 6-dot configuration, shown in Figure 2-6b, due to its ability to allow for clocking in molecular or macromolecular implementations (which will be discussed later in this chapter). A common trait of all of these configurations is that they all have two free electrons and two preferred electron configurations corresponding to the binary logic values. Therefore, all cell configurations benefit from the basic research into QCA logical design and circuit layouts of the other configurations. Also,

development of the physical model and calculations of these cells utilize the same methodology and similar equations which are used for the model cell.

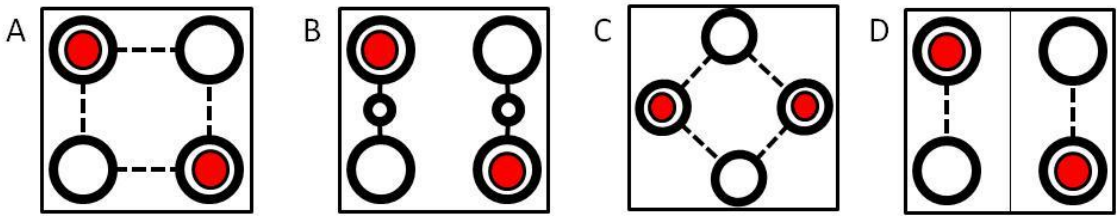


Figure 2-6. Other QCA cell configurations - A. Four-dot QCA cell configuration – B. Six-dot QCA cell configuration – C. Rotated four-dot QCA cell configuration – D. Two-half-cell QCA cell configuration

2.2.4 Cell to Cell Interaction

In order to be useful as digital communication and logic devices, the state (and subsequent binary value) of QCA cells must be highly influenced by its neighbors. A cell should also saturate at the strongest polarization value possible even in response to weak polarization of a neighboring driver cell. A measure of these properties takes the form of polarization gain in QCA, where $P_{gain} = P_{resultant}/P_{driver}$. High polarization gain provides good noise immunity to QCA circuitry and thus allows for reliable communication and computation.

In the early QCA studies [37, 38, 39], several cellular configurations were examined to determine which one produced the highest polarization gain. These studies resulted in the choice of the standard cell configuration due to its high P_{gain}around the logical transition point. This can be seen In Figure 2-7, where the cell-to-cell response function is shown for various cells and dot configurations. High P_{gain} at this point causes a large swing in polarization in

the resultant P_2 to the saturation level of +/- 1 as the polarization of the driver cell transitions from negative to positive. In cases where $P_{gain} < 1$, (polarization loss), the signal is degrading as it is communicated down the line and thus as is will not be acceptable for circuit construction. An example of this, occurs in the cell D configuration at the higher input polarization values. For this case, another mechanism (which will be discussed later in this chapter) must be used to provide signal gain.

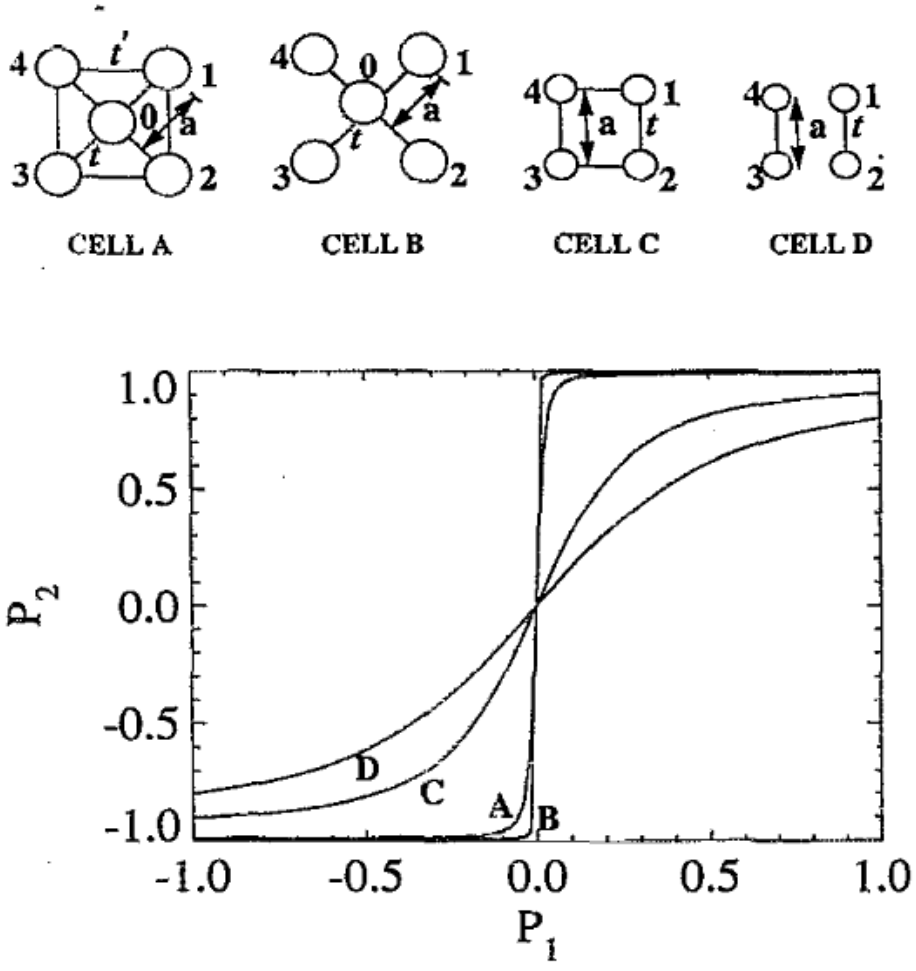


Figure 2-7. Four cell configurations and the resultant cell-to-cell response function. Here the Cell B geometry produces the best polarization gain and is thus the optimal choice based on this parameter. Taken from [37]

As has been discussed, the mechanism for producing the bistable cell-to-cell response for standard electrostatic QCA cells is the electron localization in the quantum dots and the Coulombic interaction with electrons in neighboring cells. Therefore, the configuration of the dots, intracellular tunneling barriers, and inter-cellular geometry play an important role in this interaction. The ratio of tunneling energy to the Coulombic energy is also important in determining the abruptness of the bistable response function and P_{gain} value as are factors such as temperature, dot size, and relative placement of the cells. For example, Figure 2-8 shows the change in response function with respect to a change in the tunneling energy. The extremes of this function are the cases when the tunneling energies are very high or zero. In both of these cases the polarization gain would be zero and would not allow for communication or logic.

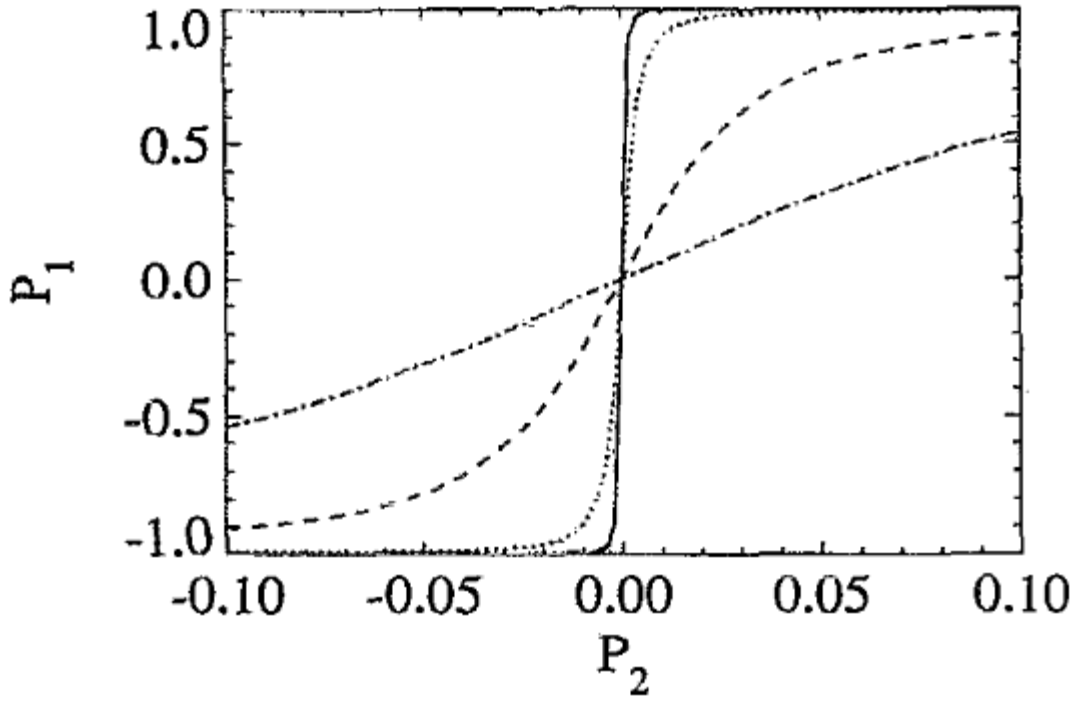


Figure 2-8. Polarization response of cell 1 to the polarization of cell 2. Tunneling energy t is modified from .2meV (solid line), .3meV (dot line), .5meV(dash line), and .7meV (dot-dash line). Taken from [37]

2.3 Logical and Communication Structures in QCA

2.3.1 The binary wire

The QCA properties that have been mentioned thus far provide a favorable base to build digital logic and communication structures with the paradigm. However, until a set of logically complete circuit elements can be constructed with QCA cells, its full use cannot be determined. A basic component of this set is a digital communication element, which for QCA, takes the form of a binary wire. The binary wire (or just wire) was designed based on the principle that the polarization of each cell tends to be equal with its neighbor when the cells are linearly aligned [40, 41]. Therefore, the wires travel in either a horizontal or

vertical line and are able to turn only 90^{o} corners. The wires are robust and are able to effectively transmit signals if the polarization gain for its cells is greater than one. In contrast, if the polarization gain value is less than 1 then the wire will eventually fail after a certain length is exceeded. Binary wires with this property are shown in Figure 2-9. The figure demonstrates indeterminate cell states resulting from a finite length wire with a low P_{gain} value.

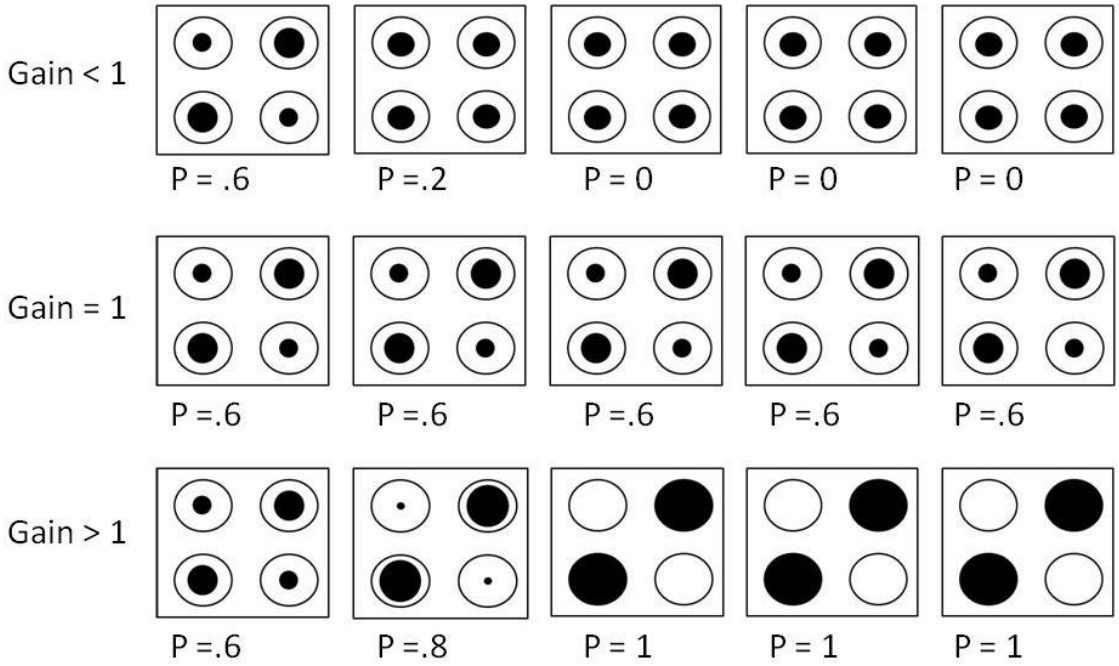


Figure 2-9. Binary wires with polarization gain less than 1, equal to 1, and greater than 1. Expectation of the number operator for each of the 4 logically interactive sites are shown as black dots. A expectation number of 1 is shown as a full black dot and of 0 as a full white dot. Expectation values between 0 and 1 are shown as dots filled to various degrees.

2.3.2 The QCA inverter

As has been discussed, if two cells are oriented in a diagonal manner with respect to each other, the resultant polarization of the driven cell is the inverse of the driver cell. This is used to create a logical gate that functions as an

inverter. In the typical QCA inverter design, shown in Figure 2-10, a single binary wire is inverted with two diagonally positioned wire segments. These segments are then condensed back down to the single wire for output of the gate. Using two segments (instead of one) makes up for the loss of polarization gain due to the increased distance between centers of diagonally oriented cells.

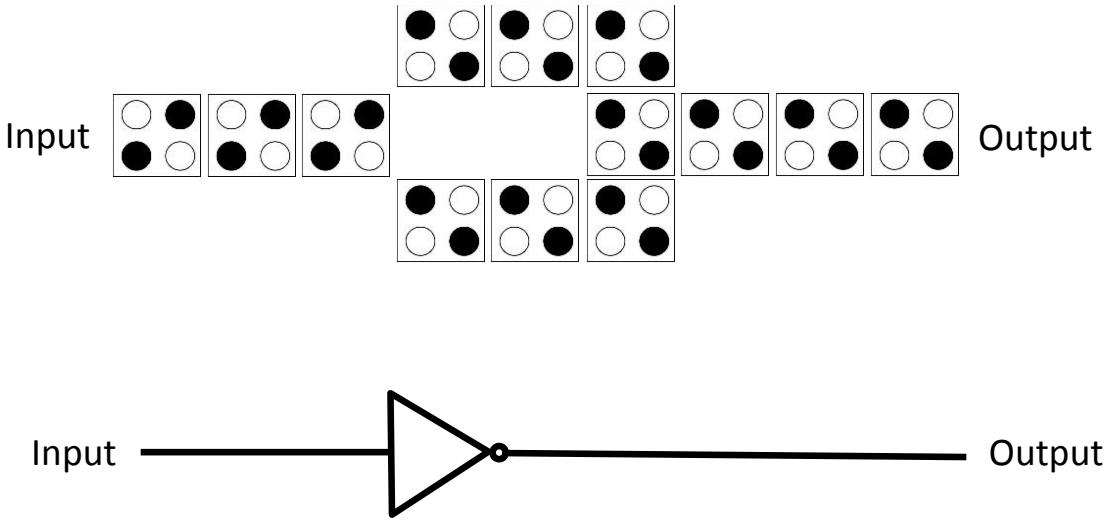


Figure 2-10. QCA inverter and associated symbol

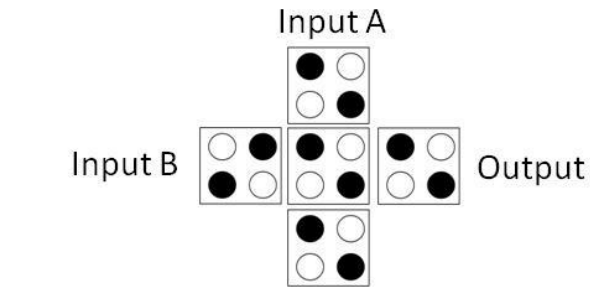
2.3.3 The majority voter

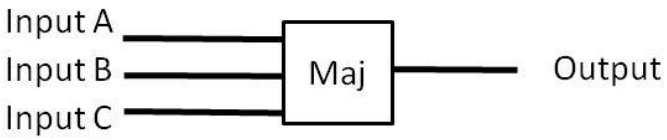
The most fundamental logic element in the QCA architecture is a direct result of the majority-type interaction of horizontally and vertically aligned cells. This element is the three-input majority gate, which has a Boolean logic equation equal to (2.6).

$$Out = AB + BC + AC \tag{2.6}$$

Its structure, shown in Figure 2-11, requires only a single QCA cell to perform the function. The gate can be used to directly perform three-input majority operations or it can be used implement more traditional two-input AND or OR

gates by adding a fixed input (0 or 1 respectively) to the gate's third input. However, while using AND-OR logic is a more traditional design method, it does not provide optimal logic minimization or circuit reduction. Therefore, research into design techniques and tools which utilize majority gate logic is an active area of interest [42, 43, 44, 45].





A	B	C	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Figure 2-11. QCA majority gate with associated symbol and truth table

2.3.4 Co-planer wire crossing

Another fundamental communication element in the QCA architecture is the coplanar wire crossing. In traditional CMOS digital logic, in plane wire crossings are not possible. Instead chips must be made with several layers so that wires can pass above or below each other. In QCA, it will be difficult to create structures which could transition to different layers and so a planer wire crossing structure is preferred. Luckily the original designs were able to create a planer wire crossing structure by using QCA cells whose quantum dot sites

were rotated 45^{o} internal to the cell. In this way two wires could intersect at a 90^{o} angle and pass through without affecting each other. The cellular structure of a planer wire crossing and its associated symbol is shown in Figure 2-12.

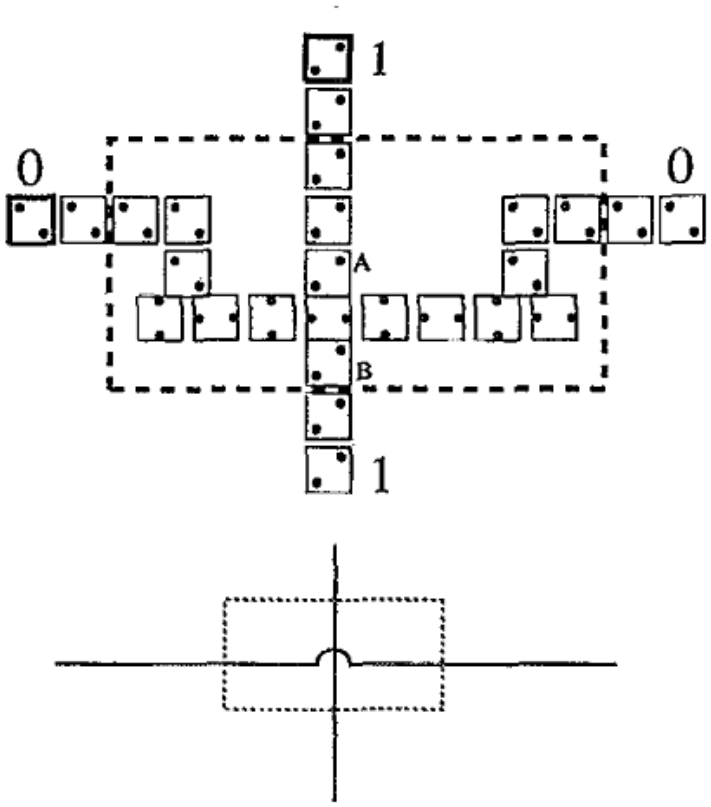


Figure 2-12. Planer wire crossing structure in QCA. Taken from [40]

With these fundamental and logically complete circuit primitives, the QCA architecture is able to produce any desired logical function. Examples of the use of QCA to produce more advanced logic can be seen in [40, 46, 47, 48].

2.4 QCA Implementation Technologies

In the early stages, the theoretical development of QCA was restricted to the original coupled quantum-dot systems which took the form of electrostatic

metal-dot implementations. However, these systems represent only a part of the experimental implementations which have been attempted or theorized for QCA to date. This is due to fact that other implementations have been found to provide the same fundamental characteristics of a local bistable cell to cell response, majority voter evolution function, and ground state computing as the original metal-dot systems. Furthermore, these new implementations are able to utilize other materials and other state variables to provide advantages in size, robustness, or fabrication concerns over traditional designs.

The new QCA implementations, along with the metal-dot realizations, can be grouped into two categories relating to the physical state variable used for computation. The first of these groups is the electrostatic QCA which contains the original designs and is the most prevalent. The second group contains magnetic QCA implementations. The electrostatic implementations can be subdivided into three additional groups: the original metal-dot QCA, semiconductor QCA, and molecular QCA. This section contains a brief description of these implementations along with their advantages and disadvantages.

2.4.1 Electrostatic Metal-Dot QCA

Early experimental fabrication of QCA cells and logical devices was accomplished through the use of cells constructed of metal quantum dots. In particular, several metal-dot QCA cells were fabricated utilizing Al dots with $Al/AlO_x/Al$ tunnel junctions [49, 50, 51, 52, 53], one example of which is shown

in Figure 2-7. These cells were shown to produce the required bi-stability of QCA devices and effectively demonstrated communication [54], majority gate logic [55], clocking of QCA cells [56], and fan out structure [57].

However, they were fabricated as more of proof of concept demonstrations and not feasible paths to large scale nanoelectronic circuitry. Thus, they were composed of relatively large cells which were difficult to fabricate except for very simple circuits. Additionally, due to the very small energies associated with their operation, they had to be operated at liquid He temperatures (<100mK) and with magnetic fields to suppress resultant superconductivity.

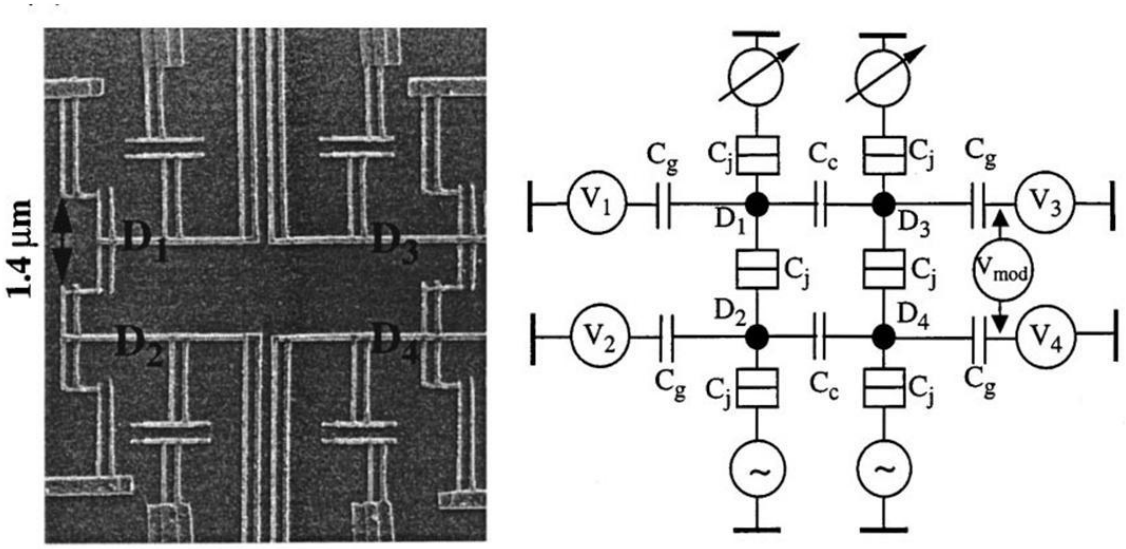


Figure 2-13. SEM image of Metal-dot QCA cell and associated schematic. From [52]

2.4.2 Electrostatic Semiconductor QCA

Due to the prevalence of semiconductor devices and technologies, QCA fabricated with semiconductor quantum-dots would potentially enable direct

integration with current CMOS and allow for an easier transition to the new paradigm. Because of this, research into a semiconductor realization of QCA has been strong, yielding QCA fabricated with GaAs/AlGaAs quantum dots [58, 59] and recently published implementation based on Silicon [26] (shown in Figure 2-14). Unfortunately, current semiconductor patterning technologies do not allow for a small enough size scale to make room temperature operation possible[4]. Therefore, semiconductor QCA suffer from the same temperature and speed limitations found with metal-dot QCA.

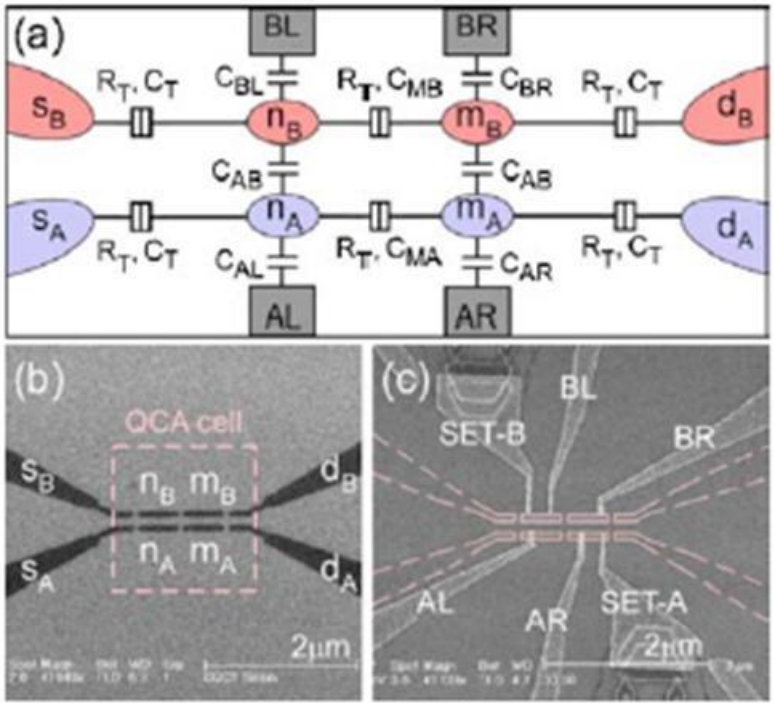


Figure 2-14. Silicon based QCA schematic and SEM images from [26]

[4] Size scale is inversely proportional to energy separation of ground and excited states, thus smaller size QCA allow for greater noise immunity, a fact which will be shown later in the dissertation.

2.4.3 Molecular QCA

In order to compete with conventional CMOS electronics circuitry in terms of speed [60], reliability, and room-temperature operation [61], projections indicate that traditional QCA will require cells on the size scale of individual molecules [27, 62]. As such, a large amount of research into potential molecular QCA implementations has been accomplished. This research can be broken down into two major fields, the placement and construction of QCA circuits and the choice of a suitable molecule which can provide the required QCA cellular attributes.

One of the more promising potential technologies for molecular QCA circuit construction involves the use of DNA rafts which are able to form templates for the self-assembly of candidate QCA molecules. The DNA rafts are positioned into lithographically defined trenches in a Si base structure [63] (shown in Figure 2-15). This technique utilizes electron beam lithography which does not scale well into VLSI level circuitry and also produces QCA cells which are slightly above the size scale required for room-temperature operation. However, the direct utilization of both self-assembly for correct relative placement of cells and lithography methods for circuit construction is sound and directly applicable to work proposed in this dissertation.

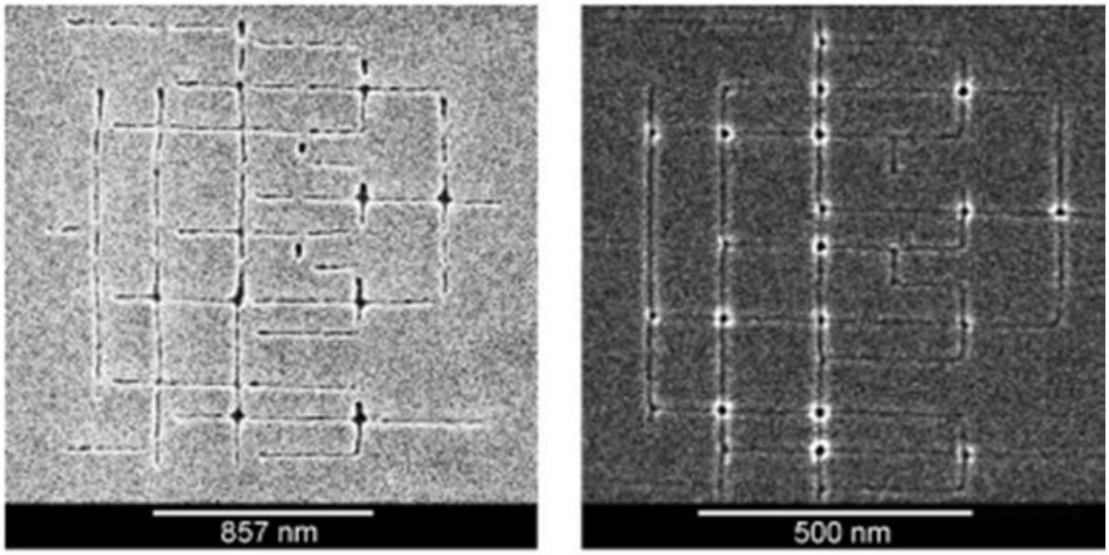


Figure 2-15. QCA full adder templates formed by electron beam lithographical patterning from [63]

Other work in molecular QCA has focused on the identification of suitable molecules for which QCA cells can be constructed. These molecules are generally mixed valence complexes with either two or four redox centers acting as the quantum dots [64, 65, 66, 67]. In these cells, electron transport between and localization in the redox centers define which molecules will be suitable for QCA. A typical molecular candidate is shown in Figure 2-16 along with *Ab Initio* simulation results for the surfaces of constant potential for each of the QCA states.

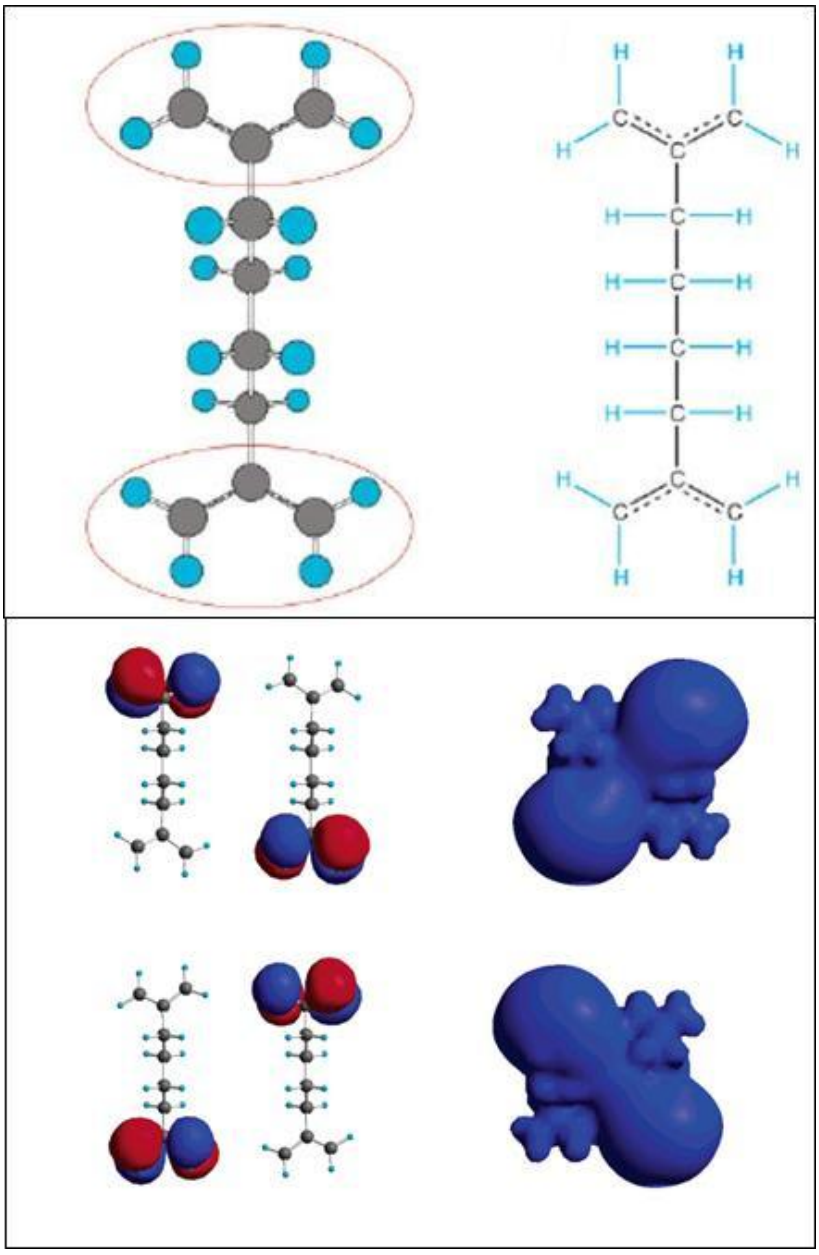


Figure 2-16. Mixed valence candidate molecular cell for QCA, along with the constant charge radiuses for the two logical QCA states, taken from [27]

2.4.4 Magnetic QCA

Implementations which utilize magnetic dipole interaction between cells have recently gained much attention due to their ability to allow for near room-

temperature operation and very low power requirements [68, 69, 70, 71]. Magnetic QCA are constructed of oblong nano-magnetic particles which form QCA half cells. Due to shape anisotropy, the magnetic dipole aligns along the longer part of the cell. Therefore, these cells can be laid out in the way shown in Figure 2-17 to produce QCA computing and communication. In several instances these cells have been laid out in a way which deviates from the square QCA cell in order to more effectively utilize their half-cell geometry especially for logic structures [28]. One instance of this can be seen in Figure 2-17 for a majority gate.

Magnetic implementations have relatively slow switching speeds, which are in the MHz range, making them unsuitable for competition with even current CMOS electronics. However, because of their robust nature and natural radiation immunity, certain specific applications may find benefit by using this implementation.

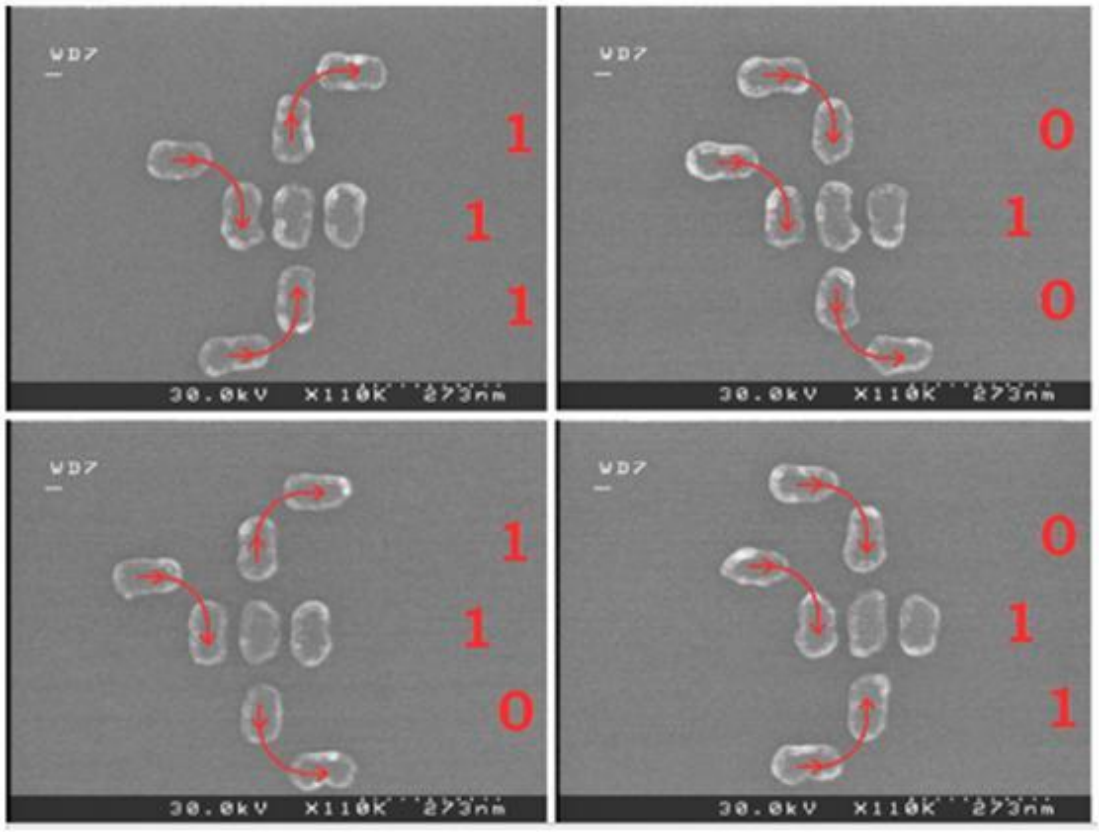


Figure 2-17. Implementations of a majority gate for magnetic quantum-dot cellular automata. From [28]

2.5 QCA Adiabatic Switching and Clocking

As has been discussed, the QCA paradigm is dependent on the state of the system being in the preferable least energy configuration based on the Hamiltonian in (2.1). However, utilizing this property for digital electronics has several difficulties which must be addressed. Most importantly, the QCA system is not isolated and thus other factors play into the system energy state other than the QCA cells themselves. Temperature for instance, may play a large role in determining system state of QCA devices. Thermal excitations may promote the QCA cells to a higher energy configuration and thus cause

errors in the digital logic. To be robust and protect against these types of excitations the lowest energy configuration must be separated from the 1st excited state by several times $k_B T$ (the Boltzmann constant multiplied by the temperature). This separation in the first energy levels of the system is dependent on several factors including the spacing between quantum dot and QCA cells and the configuration of the dots. Therefore, these properties must be determined before robust application can occur.

Another source of error in QCA is states that provide local energy minimums which may be attractive as the system switches. These states are called metastable states and can produce circuit errors if they are not overcome within the normal settling timescales. Unfortunately, the process of overcoming the barriers associated with these states is probabilistic and dependent on several factors including the barrier height and energy of the system. However, adjusting these parameters to create favorable conditions for successfully transitioning through meta-stable states will cause other problems that may lead to circuit errors.

A simple example of metastable states and their potential to cause circuit errors is seen in Figure 2-18. In this figure, a switching event occurs in a simple binary wire as the input cell is set from a logic 1 to a logic 0 state. Ideally, this switching event would move down the wire sequentially until all of the cells in the wire had the same logic value (this is the global minimum wire state). However, the process of switching is not instantaneous and therefore as the wire transitions, it is possible for a cell to be caught in a unpolarized state with

the cells to the left and right inducing equal and opposite polarizations on it. Because of this the cell would not transition out of the unpolarized state and thus the switched signal would not propagate to the end of the wire.

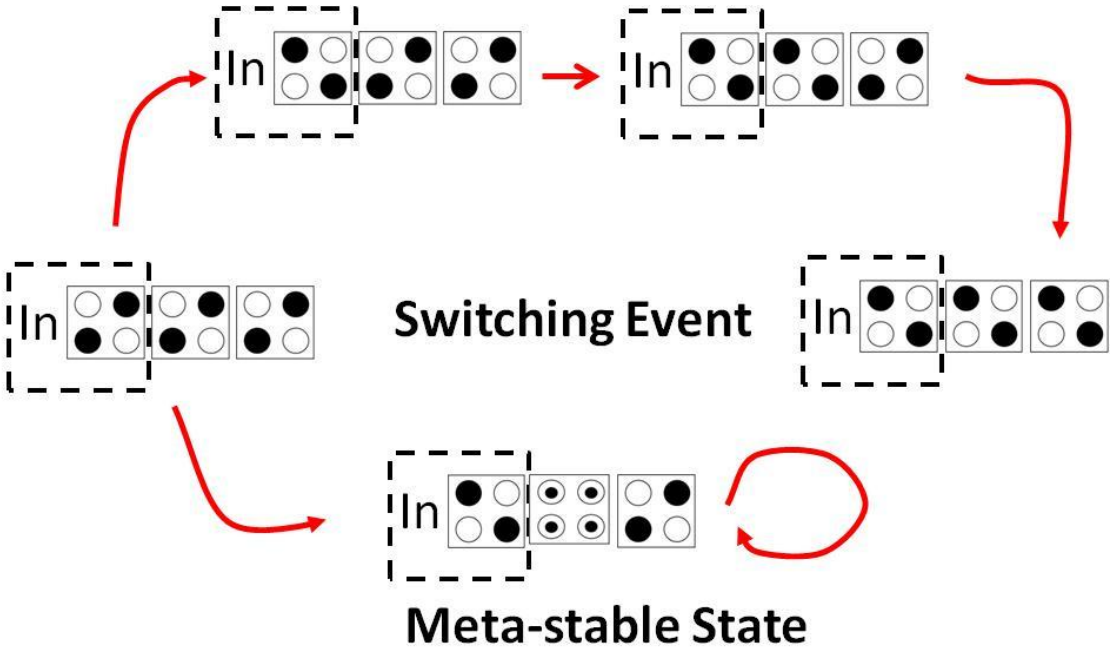


Figure 2-18. Binary wire switching event may lead to a correct output or metastable states.

The process and dynamics by which this switching happens is dependent on the coupling of the QCA to the environment and the ability of the QCA to gain and then dissipate the energy gained through the change of input. These processes also affect circuit properties such as speed and temperature in which robust operation is possible and provide a very challenging environment for optimization.

2.5.1 Adiabatic Switching of QCA

To overcome the problems of metastable states and their effects on the correctness of QCA computation and the speed at which switching may occur, an alternate mode of switching was proposed in [72] and verified in metal-dot implementations in [73]. In this method, the system is switched slowly enough to allow it to continuously remain in the lowest energy state. This adiabatic switching is accomplished through direct control of tunneling barrier heights which allow or inhibit interdot electron tunneling. The process works by lowering the tunneling energy barriers internal to the cells prior to switching inputs of the system. Then, as the cells are in a state in which the electrons are delocalized, the inputs are changed. The tunneling energy barriers are then slowly increased and the system converges to the instantaneous global ground state which corresponds to the correct logical configuration. Figure 2-19 shows an example of this process.

While adjustment of each individual cell's tunneling barriers is crucial to enable adiabatic switching, it is necessary to limit the complexity of the wiring which allows for it. If this is not accomplished, the wiring required to distribute the switching signals would easily dominate the device design and therefore improvements over modern digital circuits would not be achieved. Therefore, switching groups of QCA cells with the same wire and signal is the preferred method of laying out clocking circuitry and making implementation tractable [74, 75]. This process would resemble the functional pipelining found in modern processor circuitry and the adjusting of tunnel barriers would resemble a clock.

In fact, the process for raising and lowering tunnel barriers should be thought of this way in order to organize the circuitry to perform logical operations [76].

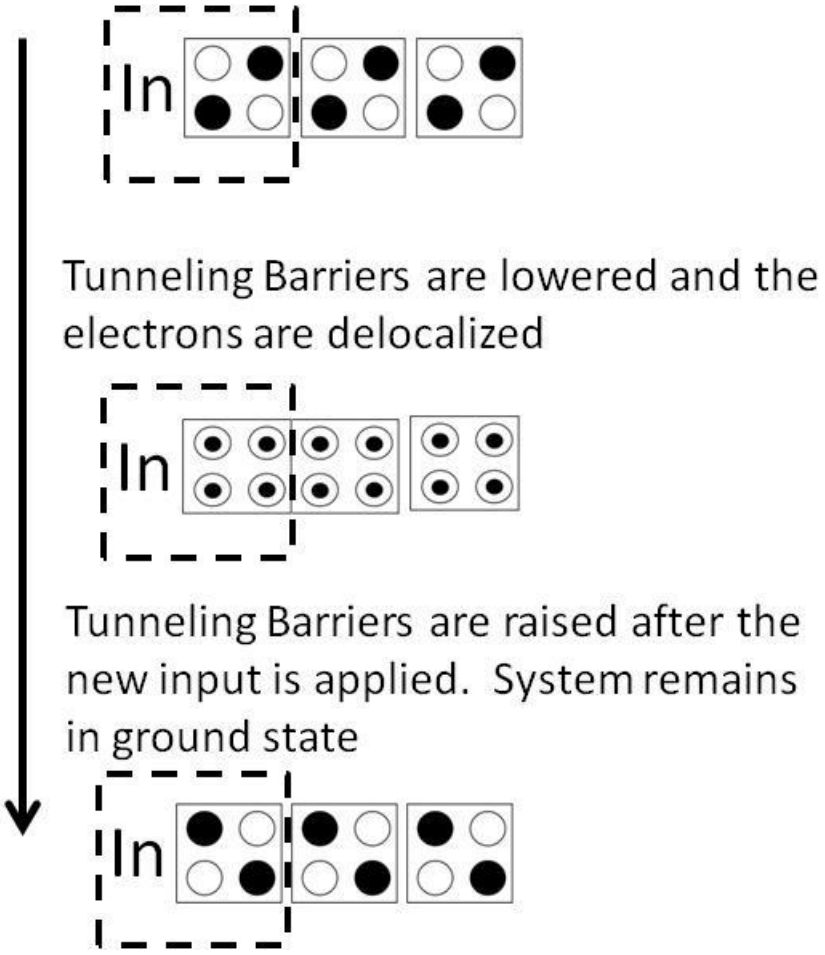


Figure 2-19. Adiabatic Switching of QCA binary wire

2.5.2 QCA clocking

The adiabatic clocking process is divided into four phases which correspond to the raising and lowering of tunnel barriers. These four phases, shown in Figure 2-20 are:

- Relax - in which the tunnel barriers are lowered and the electrons are delocalized,

- Null – in which the electrons are delocalized and the cells have no logical effect on other QCA cells,
- Switch – in which the cells tunneling barriers are raised, the cell's electrons become localized and are switched to their new ground state, and
- Hold – in which the interdot barriers are made high enough to where no switching is allowed; thus allowing for these cells to be used as inputs to other parts of the circuit without the other cells affecting their state.

The QCA clock not only allows for pipelining of QCA circuitry which allows for fast operation, but it also allows for more robust operation, higher complexity potential in circuit layouts, and important logical constructs such as feedback of signals [75, 77]. In fact, clocking has become crucial to the theoretical development of QCA electronics.

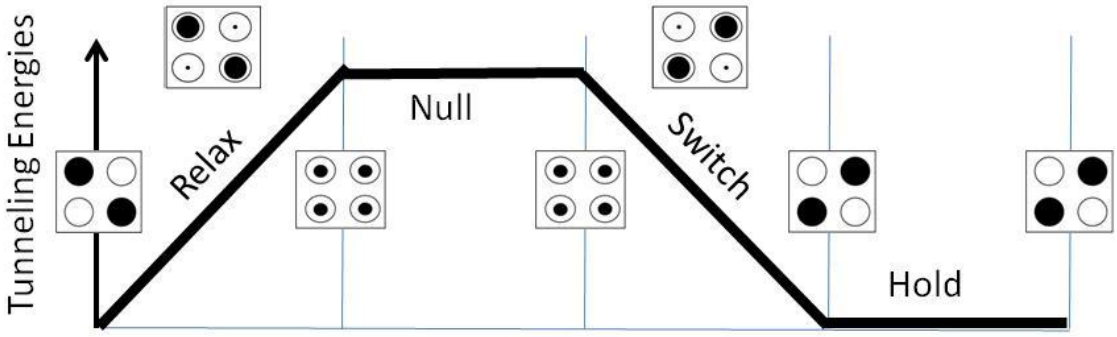


Figure 2-20. Four phases of the QCA clock

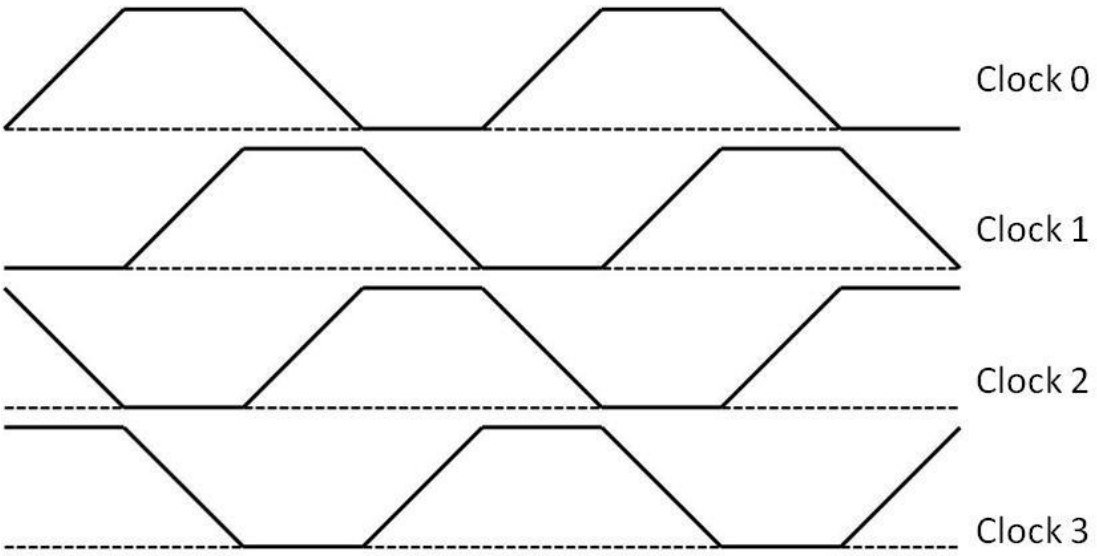


Figure 2-21.Four clocks used for QCA

In large scale QCA circuitry, it is required to have four different clocks (shown in Figure 2-21) distributed throughout the circuit. These four clocks all contain the exact same waveform and each clock is out of phase with the others on ¼ cycle intervals. This produces a single clock in each of the four QCA phases at any given instant. With this design, clocking is applied to the QCA cells so that cells in the Hold phase drive cells which are in the Switch phase. An example of a circuit with each of these four clocks being utilized is shown in Figure 2-22. In this figure, a sequential circuit element is shown (in this case a QCA memory cell) to demonstrate feedback with QCA. This clocking scheme is usually referred to as Laudaner clocking and is the basic way of pipelining throughout a circuit. Other clocking schemes such as Bennett Clocking are suitable for reversible clocking of QCA circuitry [78] and will be discussed further, later in this chapter.

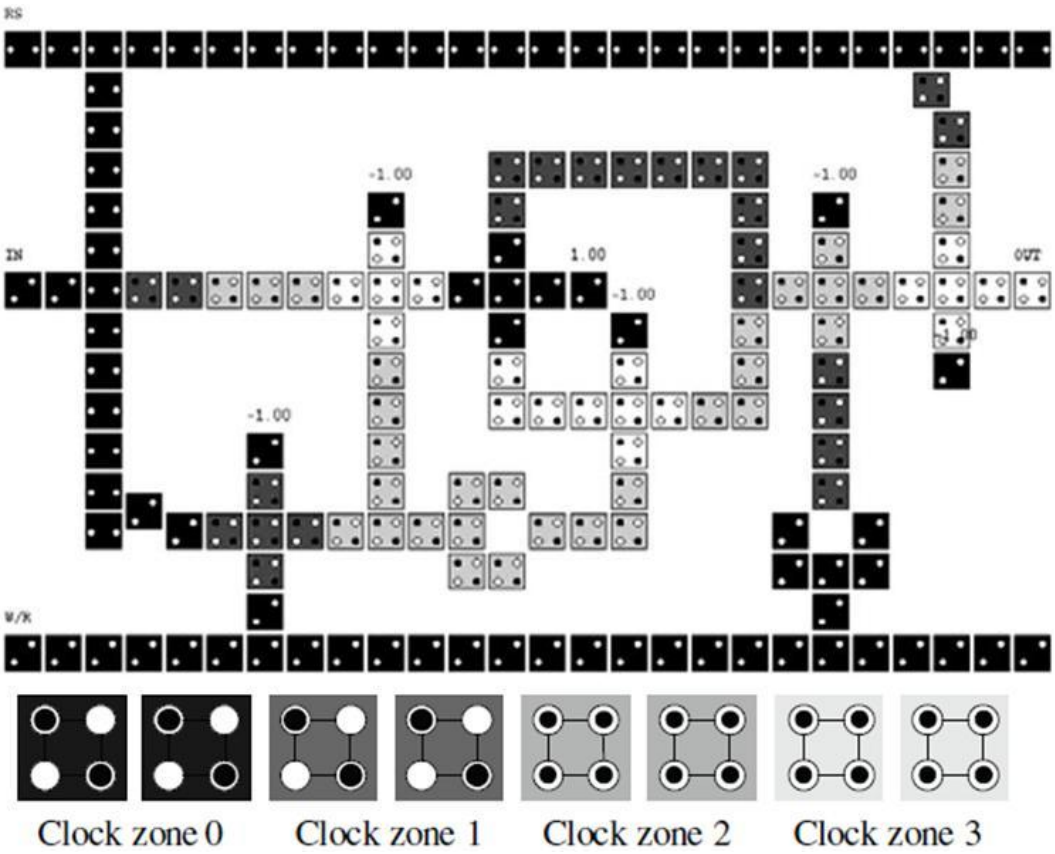


Figure 2-22. QCA memory cell. The cells are colored with different shades of grey corresponding to the usage of one of the four clock zones. Taken from [79]

2.5.3 Implementation of QCA Clocking

In the original experimental realizations of QCA which utilized metal dots, clocking was implemented by the addition of a third “middle dot” to each half of the QCA cell. These middle dots ware then capacitively coupled to a gate electrode [53]. The voltage of the gate electrode was adjusted to provide the waveform shown in Figure 2-20. Using this mechanism to clock QCA allowed for an effective barrier to be raised between outer, logically interacting, dots. Additionally, since only the potential of the middle dot was raised, and that dot was equally spaced between outer dots, the effect of the induced electrical field

did not disturb the degeneracy of the logical states. However, it is clear that this direct method of clocking would not scale well to the single nanometer QCA cell size of a reasonable nanoelectronics proposal, as the wiring for the clocks would dictate the minimum feature size and therefore not provide a large improvement over current technologies.

For these reasons a new method of implementing the clocking mechanisms for molecular scale QCA was proposed in [62]. In this proposal, traditional molecular QCA cells were constructed using two V-shaped molecules such as shown in Figure 2-23. The proposal depends on these molecules being attached to the surface with the middle dot down. A wire embedded in the surface material then induces a perpendicular electrical field in the plane with the molecule and has the effect of either pushing the free electron into one of the arms of the V-molecule or pulling the electron into the middle clocking dot. When the electrons are pushed into the arms, they are able to induce an effect on the polarization of neighboring cells and therefore this state is, the afore mentioned, “hold” clock phase. When the free electrons are pulled into the middle clocking dot, there is no net effect to the polarization of surrounding QCA cells and therefore this becomes the “null” clock phase. Also, by using the electric field of the embedded clocking wire, there no longer has to be direct connection with each QCA. Therefore, a large area of QCA can be clocked with the same wire, naturally allowing for the clock zone approach.

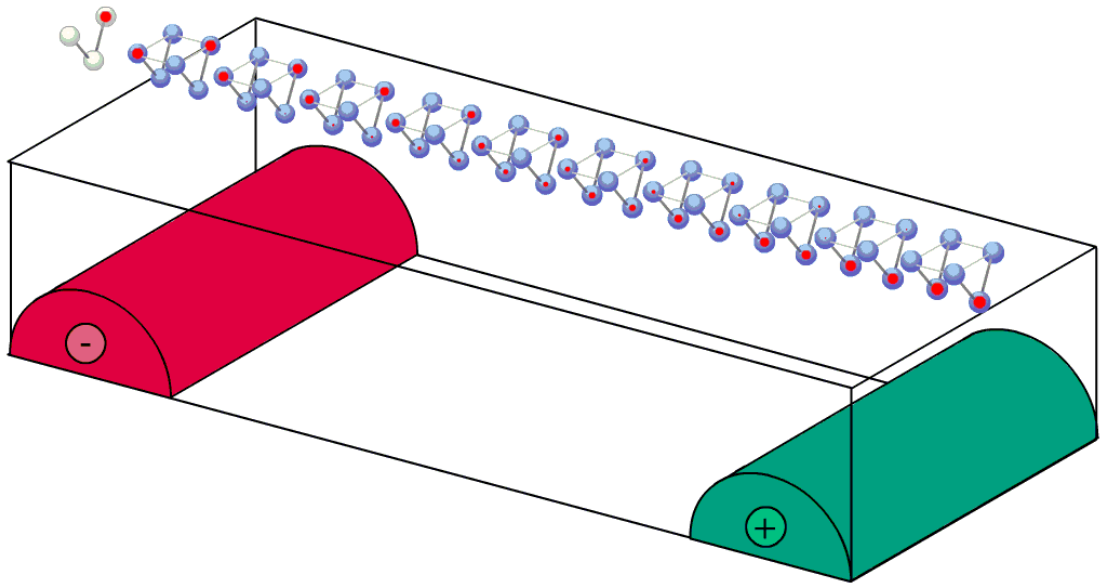


Figure 2-23. Candidate QCA molecules when clocked – Buried clocking wires induce a perpendicular electric field into the QCA molecular cells – red dot shows free electron in each of the two molecule parts – from [80]

2.6 QCA Logic Advances

With the addition of the clocking scheme, QCA circuits can be built which are logically equivalent to standard CMOS based circuits. However, as with the change to any new paradigm, challenges which are specific to the new paradigm must be addressed. For many nanoelectronics proposals, including QCA, fault tolerance will play a major role in the correct operation of any circuit. This is due to many factors, such as the probabilistic nature of circuit assembly at this level and the low relative magnitude of the state energies compared to environmental, thermal, and stray energy sources. Therefore, fault tolerance must be addressed at both the physical level of device implementation and the logical design level.

In addition to the attention that must be given to the challenges which are specific to the QCA paradigm, attention must also be given to opportunities to advance the state of logic design and computing by utilizing the inherently useful properties of QCA. In particular, two interesting opportunities such as these exist for QCA. The first utilizes the inherent parallel nature of QCA, along with the possibility for coplanar wire crossing and subsequent simpler circuit layout and design, to provide advanced resources in the design of systolic and parallel architectures [81, 82]. The other opportunity involves the implementation of reversible circuitry by utilizing the charge state based logic of QCA and some unique clocking proposals which are possible through the paradigm. The proceeding sections discus fault tolerance techniques for QCA as well as reversible computing concepts of QCA.

2.6.1 QCA Fault Tolerance

Logic level fault tolerance designs are common in nearly all nanoelectronics proposals. This is generally due to the lower power and probabilistic processes involved when using devices at the ultra-small size scales. Common logical techniques to accomplish this often fall into the categories of re-configurability [83, 84, 85] or redundancy [86, 87, 88]. While the need for logic level fault tolerance is common to nanoelectronics paradigms, the choice of methods for designs should be specific to the underlying implementation technology and analyzed based on the tenants and physics of the paradigm.

With this in mind, Finjay and Toomeran [89] proposed block gates and thick wires shown in Figure 2-24 to provide increased robustness in the presence of

QCA specific fault mechanisms. However, the design stopped short of providing details to important circuit design specifics such as how to route or connect gates and wires. However, this work did provide an important first step in understanding how QCA specific fault tolerance would work. Additional QCA-specific fault tolerance works also focused on this sort of hardware redundancy by adding additional width to wires or creating block gates to account for cell misalignment, addition, or deletion affects [90, 91, 92]. Additionally, other works on N-modular redundant QCA designs have shown limited overall benefits due to the extra complexity involved with their addition [93].

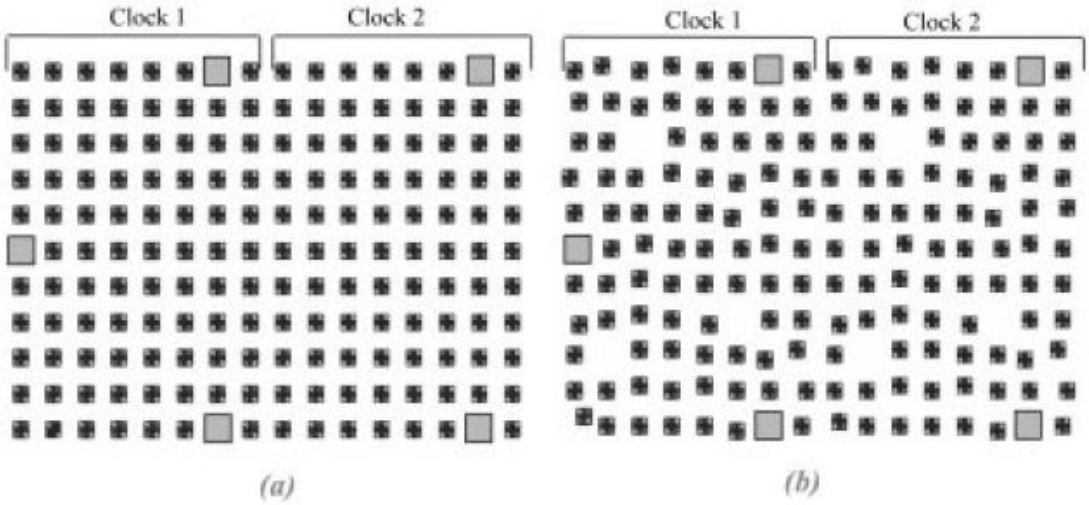


Figure 2-24. Block of QCA composing two cascading majority gates a) regular arrays b) irregular defective arrays. From [89]

2.6.2 Reversible Logic Designs and Bennett Clocking

Power dissipation is ever increasing in importance as feature sizes decrease and clock speeds increase. This is especially true of the QCA paradigm as cell size of 1nm and clock speeds of 1 THz have been predicted. In order to achieve these results power dissipation must be limited. Fortunately, the QCA

paradigm is particularly well suited to implement reversible computing; which enables computing without destroying information and thus invoking the fundamental $k_B T$ limit of power dissipation according to Landauer's Principle [94].

In QCA, there are two different methods to reversible computing. The first method involves implementing reversible gates in QCA and clocking the circuitry with the Landauer method which was previously discussed in the last section. The other method to reversible computing does not require specialized reversible gates. Instead the clocking mechanisms themselves save all of the information in the system and keep it from being erased. The clocking style used in the second method is named after Bennett who extended Landauer's principle by suggesting that reversible computing could be achieved if copies of the inputs were echoed to the outputs [95].

An example of the information flow for Bennett and Landauer clocking methods can be seen in Figure 2-25. These methods have been shown to be highly effective for reducing power dissipation requirements in QCA circuitry [78]. Additionally, reversible gate designs have been shown in [29, 96, 97] to aid in testing and fault detection.

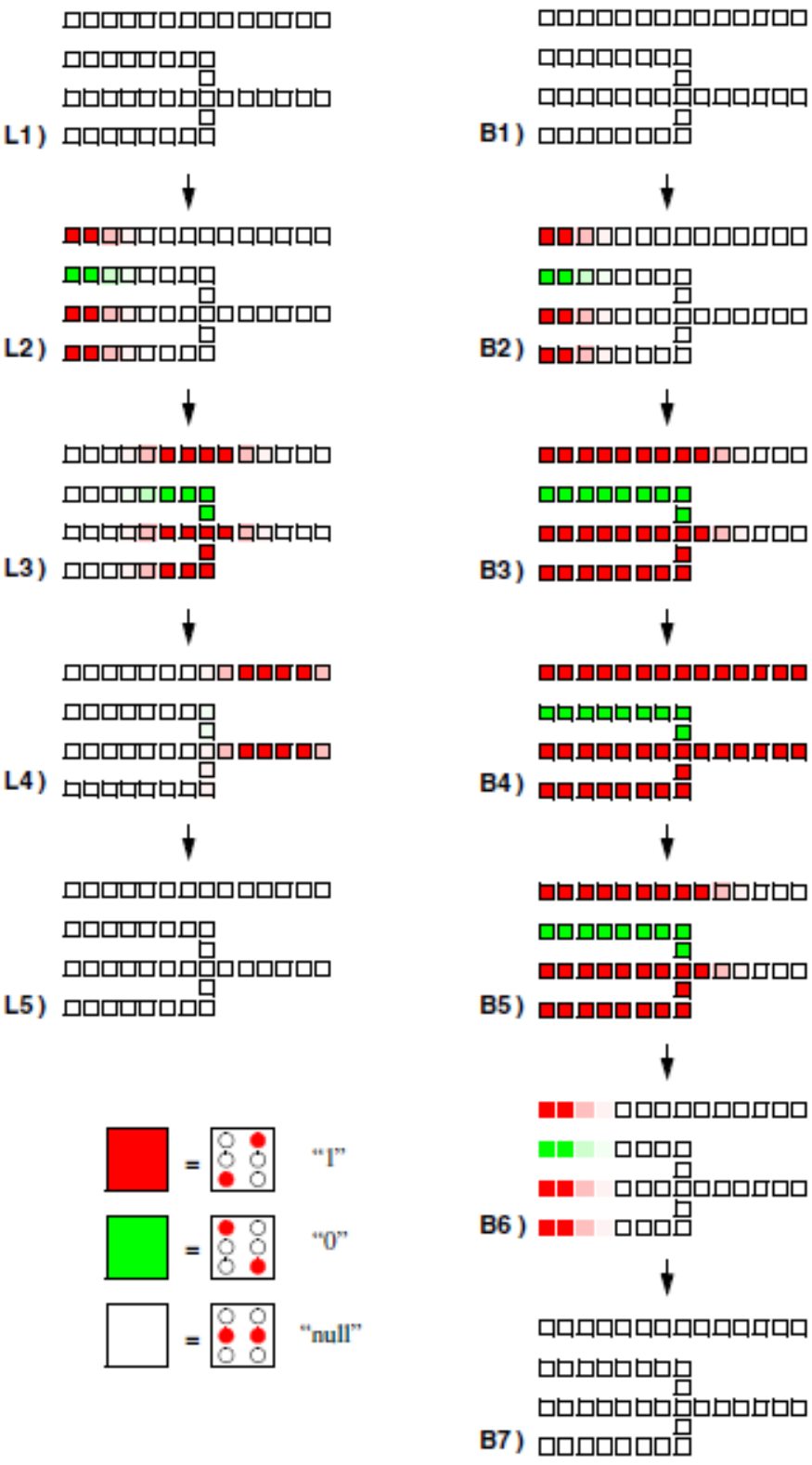


Figure 2-25. Example of the information propagation for Landauer clocking (right) and Bennett Clocking (left). From [78]

2.7 Power, Speed, and Reliability in QCA

It has already been shown that QCA is one of the most well developed and promising nanoelectronics paradigms as evidenced with the advanced logical constructs of fault tolerance and reversibility discussed in the previous section. However, even more important to the future of the QCA paradigm are the fundamental properties of power, speed, and reliability (particularly at room-temperature). These factors drive design decisions and system performance for currently available electronics systems and for QCA, or any other nanoelectronics candidate, they will be even more crucial. Due to this observation, research has been ongoing to attempt to understand and optimize these properties and develop solutions to the most pressing challenges associated with them. This goal extends to this research presented in this dissertation and thus a background in the evaluation of current QCA designs is warranted.

For QCA, the properties of circuit speed, power dissipation requirements, and reliability in a thermal environment are highly interrelated. This creates problems with investigating the system performance of any of these characteristics individually. This is further complicated as other properties such as cell size and circuit layout, which are not fixed, due to a lack of specific implementation material, have additional significant impact. To simplify the process, early non-clocked QCA are used which yield information concerning individual cell dynamics and environmental coupling. This information can then be used as clocked QCA cells are studied to provide quantitative results on

potential circuit speeds, power, and reliabilities. (These attributes are highly favorable to QCA, compared to projections for other technologies, if a suitable implementation material can be fabricated.)

2.7.1 Non-clocked QCA evaluation

Switching in QCA without an applied external clocking mechanism takes place as the influence of neighboring cells provides energy through Coulombic interaction to shift the cellular state to a higher energy level. During this process, other states are also shifted energetically leading to a different ground state for the cell and the system. As the cell dissipates energy through a coupling to the environment, the cell ideally “falls” into the new ground state. This process often may lead to the cell falling into a state with a low local energy and thus becoming trapped in a meta-stable state. In order to “find” the correct ground state the cell must then be given suitable energy to overcome the metastable state and hopefully move to the more energetically favorable ground state. So, two factors are present here which affect the speed at which the correct switching of un-clocked QCA cells occur. The first is the speed at which the cell may dissipate energy to the environment and relax into a lower energy state. The second is the amount of thermal energy which can be gained from the environment to overcome metastable states. Furthermore, the actual ground state barriers, which are directly related to tunneling energies and cellular and circuit geometries, may also be overcome and state errors may occur if thermal energy exceeds other limits. Therefore, a balancing exists between the high temperature and cellular geometrical and electrical properties.

Generally, un-clocked cellular switching is a statistical process in QCA, which has a direct effect on the reliability of circuits and the speed at which they can be switched. In [98], this switching is measured as relaxation time $< t_{rel} >$, or the time it takes the circuit to relax to the correct output state. As can be seen in Figure 2-26, average and worst case relaxation times are a function of temperature to a certain point but then, as high temperatures are reached, the cells cease to relax at all to the ground state and the function breaks down. The cells analyzed here operate in the energy regimes of the original metal-dot implementations, meaning that very low temperature operation is required (seen clearly in the figure.) However again, as cell dimensions decrease, the temperature dependence becomes more favorable to a room-temperature operation.

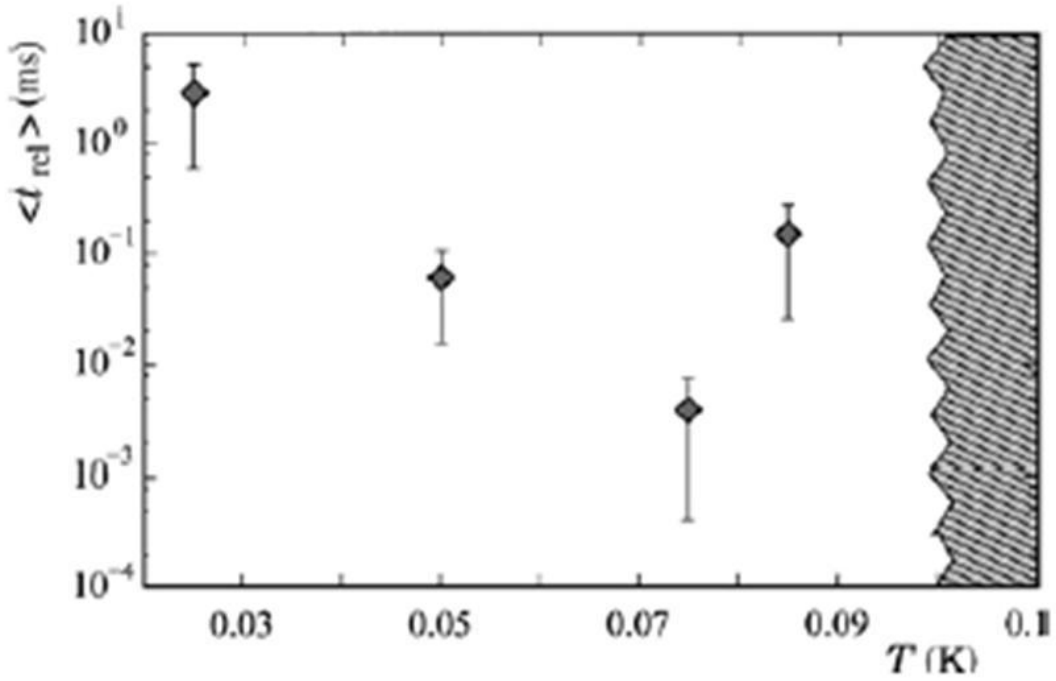


Figure 2-26. Average and range of relaxation times $< t_{rel} >$ for metal dot implementations as a function of temperature. From [98]

In [61], alternate cellular geometries were tested to determine statistical probabilities of correct output. These results are shown in Figure 2-27, and point to a dependence of the probability of correct output on cellular geometry, temperature, and number of cells in a wire. Circuit complexity is also given as a factor affecting these probabilities.

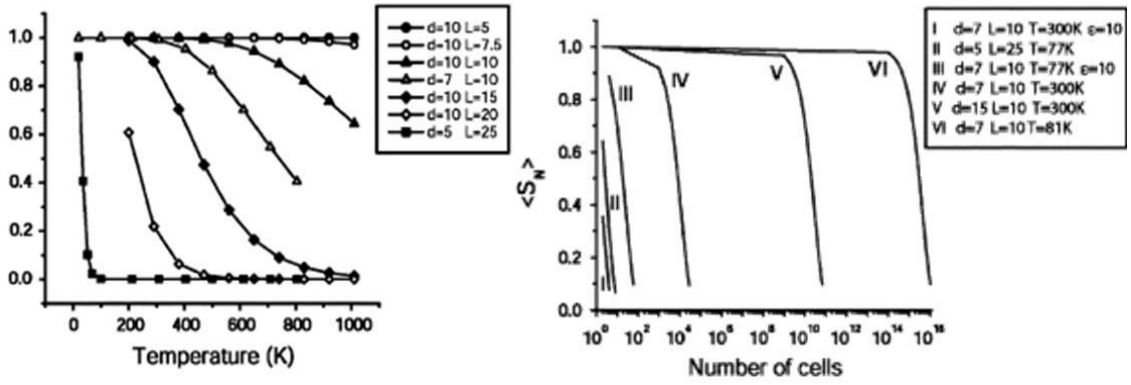


Figure 2-27. Reliability dependence of non-clocked QCA wires on cellular geometry, temperature, and number of cells. From [61]

2.7.2 Clocked QCA circuits

Results from analysis of non-clocked QCA cells and circuits show reliability dependence on temperature and energy. Also shown, are a dependence on relaxation times, which is directly correlated to switching speed. In clocked QCA circuits these dependences are even stronger, as problems with metastable states are removed and clock speeds are able to increase by many times. Clocking also limits the complexity of circuit constructs as cells in different clocking zones switch at different times and do not affect each other from a statistical prospective. However, this has an effect on overall circuit timing and reliability. In [99], it was found that as wire length increases there is a linear decrease in reliability, thus making short wires and a large number of clocking zones advantageous. However, as the number of clocking zones increased there was an exponential decrease in reliability. Therefore, there is a balance that must be found between clock zone size and circuit complexity. This

relationship can be seen in Figure 2-28. where reliabilities for two different wire lengths are shown.

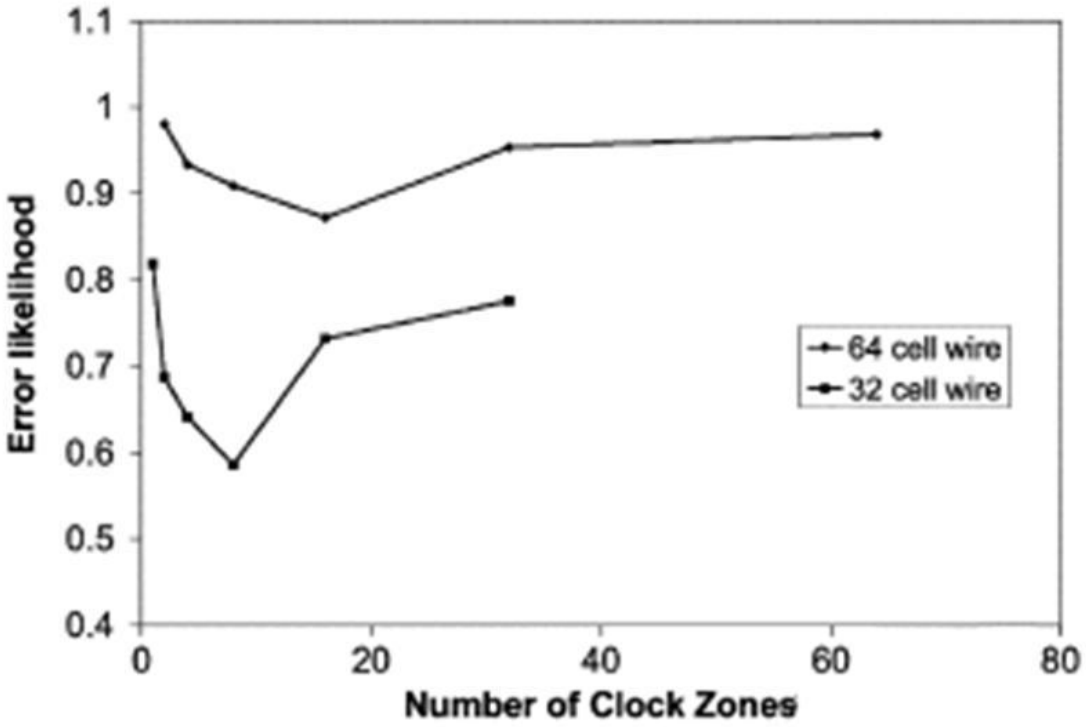


Figure 2-28. Relationship between reliability and clocking zone size in wire of different sizes. From [99]

The power that must be dissipated from clocked versions of QCA come from two different sources. The first is the clocking itself and has been described as a process analogous to leakage current in CMOS electronics. The leakage current does not depend on cell switching, but instead depends on the clock rate and its deviation from the adiabatic ideal, which is directly influenced through circuit energies (and thus cellular geometries) and coupling to the environment. The other power mechanism in QCA comes from the unavoidable cost of irreversible switching of cells and the subsequent information that must be dissipated to the environment.

As the clock speeds increase, power dissipation requirements for each of these mechanisms increase. This is due to the extra switching events which could occur at each clock cycle, but also the quicker switching and therefore greater deviation from the adiabatic ideal.

Therefore, clock speeds, cellular geometries, and coupling to the environment have direct effects on the power which must be dissipated by a single QCA cell. However, cellular geometries also affect circuit density and therefore the power density required of each QCA circuit. For example, results in [60], show that if a maximum power of $100W*cm^{-2}$ were allowed, a maximum worst case clock rate for specific circuit geometries could be calculated. The results of this can be seen in Figure 2-29 as an operational range of QCA circuits. The range is bounded on the top by the $100W*cm^{-2}$ limit and non-adiabatic continuously irreversible switching, and on the bottom by quasi-adiabatic reversible switching. These results also show that greater than THz clock speeds are possible for molecular size scale devices with these reasonable power limits. These results are also collaborated in [98, 100].

The effects of the interplay of power, clock speed, and reliability in QCA will be crucial to the development of paradigm in the coming years. The research that is presented in this dissertation has recognized this fact and has been improved immensely due to it.

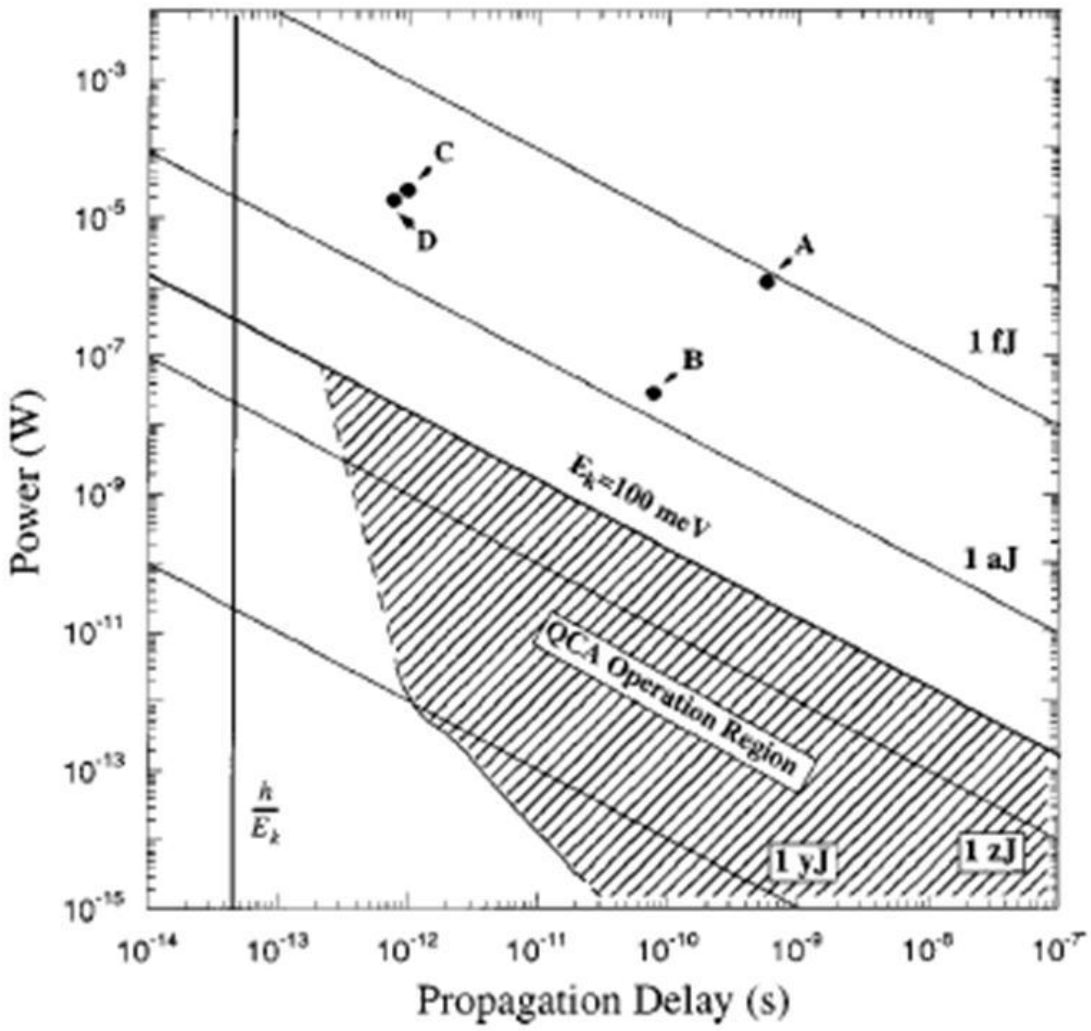


Figure 2-29. Projected circuit speeds and power dissipation for QCA circuits as well as previous CMOS technology (A-D). (30nm and 20nm gate length CMOS circuits are shown as C and D, A and B are somewhat older CMOS versions). From [60]

2.8 Chapter Summary

With many possible implementation technologies, the potential for THz switching, and advanced logic constructs, QCA seem to be well positioned to fulfill the role as a nanoelectronics replacement to CMOS ICs in the coming decades. This chapter has highlighted these important attributes and discussed

others as well which are critical to the understanding of QCA devices going further. However, the chapter has not provided a path to solving the two most important unsolved challenges facing QCA, these being reliable room-temperature operation and an architecture that provides the path to VLSI integration. For these challenges, new research will be presented in the next chapters that will be built on the strong base of theoretical and experimental QCA research to provide potential solutions and enable a path to nanoelectronics realization.

Chapter 3

Design of 2D 2-Dot Quantum Dot Cellular Automata

The path to LINA begins with the development of new QCA cell and circuit designs which mimic the 2 dimensional lattice structures of many common self-assembled materials. This is important due to the wide range of new technologies that these new designs allow for construction of circuits and the precise relative cellular placement that is required. In this way, the first of the two critical design challenges, discussed in Chapter 1, is addressed. However, in order to be preferred to traditional QCA for these reasons, these designs must also be logically equivalent to traditional QCA and scalable to the molecular level. To accomplish these goals, a cell with 2 logically interacting quantum-dots (which is based on the half-cell proposed for many molecular implementations) was found to be the most suitable choice. This cell allows a directional component to the layout which provides minimization of complexity compared to traditional QCA designs along with applicability for many other dipolar molecules or macromolecules. This chapter introduces the first step to LINA in these designs which are called “2-D 2-dot QCA” and addresses the underlying architecture and the logical constructs which make it functionally equivalent to traditional QCA and explores other benefits as well.

The organization of this chapter is as follows. Section 3.1 provides a further introduction to the new 2-dot QCA design. Section 3.2 discusses advantages of the 2-dot designs and establishes the 2-D 2-dot QCA “map,” which offers the possibility of easier implementation by using a more regular structure than seen

in other designs. Section 3.3 introduces logic constructs developed by using the 2-dot QCA cell and Section 3.4 summarizes the chapter.

3.1 Introduction

As the evolution of QCA research has progressed to include other cell configurations and implementation technologies which were discussed in the previous chapter, the 4-logically-interacting quantum dot cell configuration proposed in the original QCA papers remains to be the most widely used and studied design. This design has been shown to provide better bistability when compared with other configurations, which is especially important when considering devices with the relatively large dimensions of the original metal-dot or semiconductor experimental implementations. However, QCA cells consisting of only two logically interacting quantum dots have also been explored in literature as possible candidates for QCA cell designs or ways to simplify QCA calculations [61, 62, 28]. Interestingly, these 2-dot QCA may offer many advantages over the traditional QCA designs because of their relative simplistic operation, natural fit to many advanced QCA implementations, and ability to produce logic functions while being arranged in highly regular patterns. Even with these advantages, limited work has been accomplished using 2-dot QCA because an architecture which is able to utilize the unique properties of a 2-dot QCA has not previously been produced. Furthermore, design and simulation tools have not included 2-dot QCA to allow design and verification of

2-dot QCA logic elements. Therefore, a new architecture is proposed in this chapter which is based on the use of 2-dot QCA cells [101].

3.2 2-D 2-Dot QCA Architecture

The 2-dot QCA consists of a quantum dot and electron configuration similar to the half-cell parts used in clocked conventional QCA cells of the six dot variety. Hence, the cell is comprised of three total quantum dots which are oriented in the way shown in Figure 3-1 with the central dot being used only for clocking purposes. The quantum dots are connected to each other via tunnel junctions, which allow movement of a single free electron in each cell. Logic values “1” and “0” are then assigned according to a pre-determined convention based on electron localization and position on the outer quantum dots. Additionally, the 2-dot QCA cell relies on a four phase clock in the same way other clocked QCA designs do.

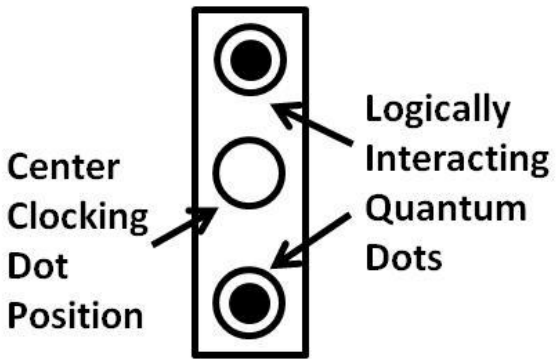


Figure 3-1. Electrostatic 2-dot QCA cell consisting of 2 logically interacting quantum dots (quantum dot) and a single quantum dot used for clocking.

3.2.1 Advantages of a 2-dot QCA architecture

With a 2-dot QCA cell, the two possible electron positions at the QD locations each correspond to either a logical 1 or 0. This is different from the case of a 4-dot QCA cell which may have as many as six different possible configurations of localized electrons. This is due to the two electrons and four possible QD positions in each cell and does not include the highly unlikely possibility of two electrons sharing the same QD. Among the six possible electron configurations, Figure 3-2 shows two nominal unambiguous configurations, and the remaining four possible ambiguous configurations. It is also seen that even in 4-dot QCA cells consisting of two half-QCA parts there are still four possible electron configurations. This increases the chances for a logic error impacting the QCA device reliability. Additionally, it increases the chance of error in simulation programs which often dismiss the unassigned electron configurations to allow for simpler calculations. In a 2-dot QCA, however, there are no ambiguous electron configurations.

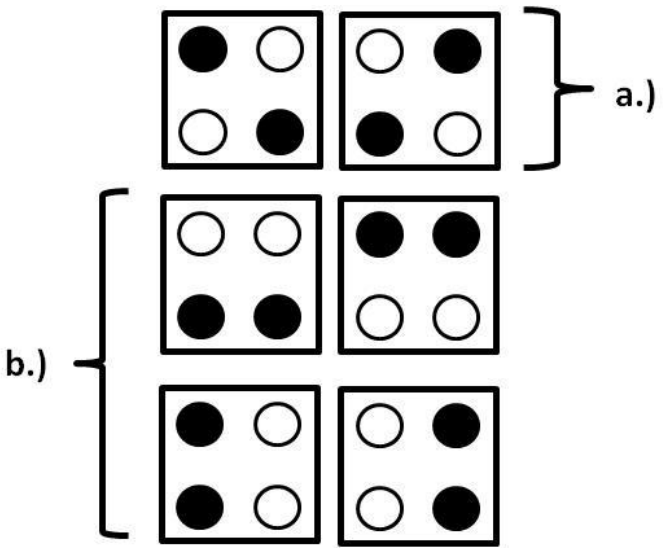


Figure 3-2. Six possible configurations of 4-dot QCA cells a) Nominal unambiguous configurations b) Possible additional ambiguous configurations

Another added benefit of the 2-dot QCA design is simply that the number of electrons and dots needed to implement logic circuitry is reduced (which will be shown in the next section). This is important due to the statistical nature of errors when these devices are operated at non-absolute zero temperatures.

3.2.2 2-D lattice structure of the 2-dot QCA

Individual placement of QCA cells may be difficult or impossible and may pose a serious roadblock to QCA fabrication especially at the size scales required to make it a viable alternative to CMOS. For this reason, utilizing a crystal lattice structure for QCA design may be helpful for fabricating QCA circuitry. This is due not only to the lattice structure of many well-known molecules and compounds, but also artificial self-assembled structures [102, 103, 104] (see

Figure 3-3), which both may be explored for the realization of periodically positioned QCA on this scale.

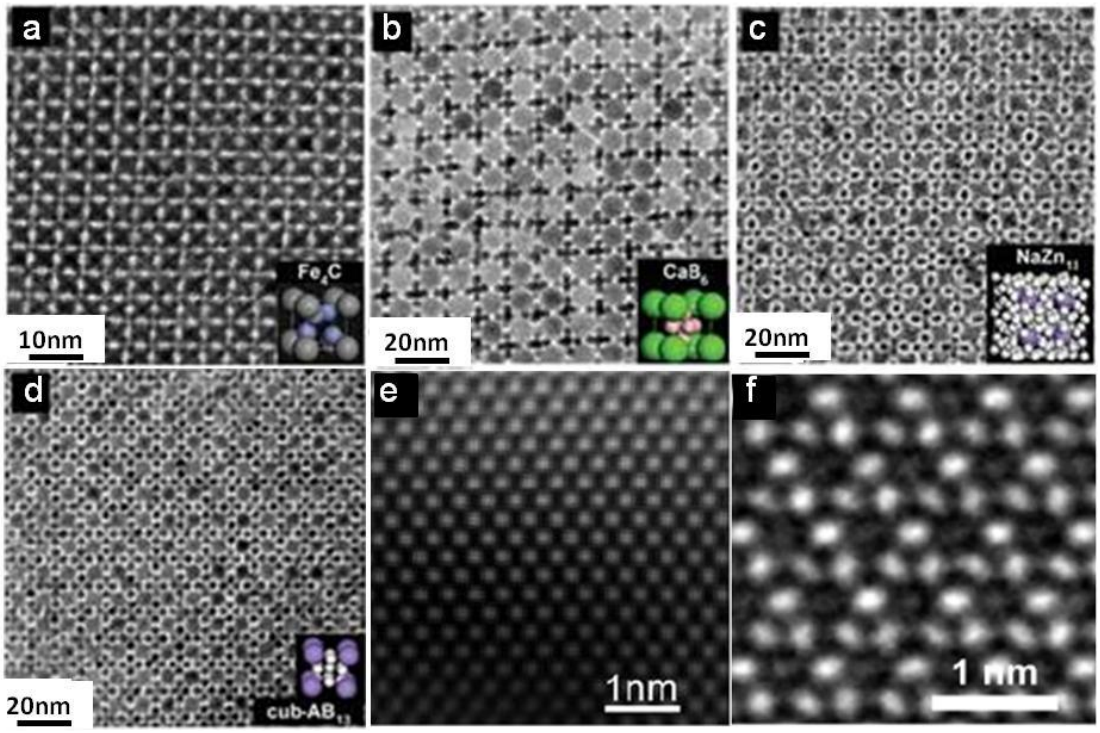


Figure 3-3. a-d) TEM images of self-assembled binary superlattices from [102] e) HRTEM image of centered rectangular 2-D molecular lattice of cross section of MnGe [103] f) HRTEM image from molecular β-Si_3N_4 lattice [104]

However, because of the layout of the 4-dot QCA cell, it is difficult to utilize a regular structure to perform many essential operations. Inversion, for example, relies on a 4-dot QCA cell which is offset by at least half a cell from the input or which is rotated by 45 degrees with respect to other cells. Planer wire crossings also rely on these 45 degree rotations. Moreover, most current QCA circuit layout designs tend to take on a similar structure to CMOS, and thus, may require lithographic techniques (to be used for both patterning and cellular layout) that are predicted to not be available at the scales required of traditional

QCA technologies. Therefore, creating a QCA architecture which could benefit from these periodic structures may, on its own, provide a breakthrough to realizable nano-scale QCA.

With these factors in mind, a “centered rectangular” 2-D periodic lattice (similar to those found in Figure 3-3) was chosen to provide the structure for possible 2-dot cell positions. It will be shown, that by residing only in the positions specified by this 2-D 2-dot QCA “map,” the 2-dot QCA cells provide a design architecture which is better than functionally equivalent to modern CMOS. Additionally, the map provides circuit designers opportunities to take advantage of the inherently parallel and reversible properties of cellular automata.

The 2-dot QCA map contains locations for 2-dot QCA cells which are orientated either horizontally or vertically (thus the 2-D name) in the manner shown in Figure 3-4b. In the vertical orientation, the cell is given the logic “1” state when the upper QD is occupied by the free electron and the “0” state when the lower QD is occupied by the free electron. For the horizontal orientation, the logic “1” state occurs when the electron is found in the right position and logic “0” when it is found in the left position. This convention is shown in Figure 3-4a.

Many logic constructs which utilize the 2-D 2-dot QCA map, such as those which will be presented in following sections, require that some map locations do not contain logically interacting cells. These locations may be left empty or otherwise nullified through means such as providing a continuously null phase clocking mechanism for these particular cells.

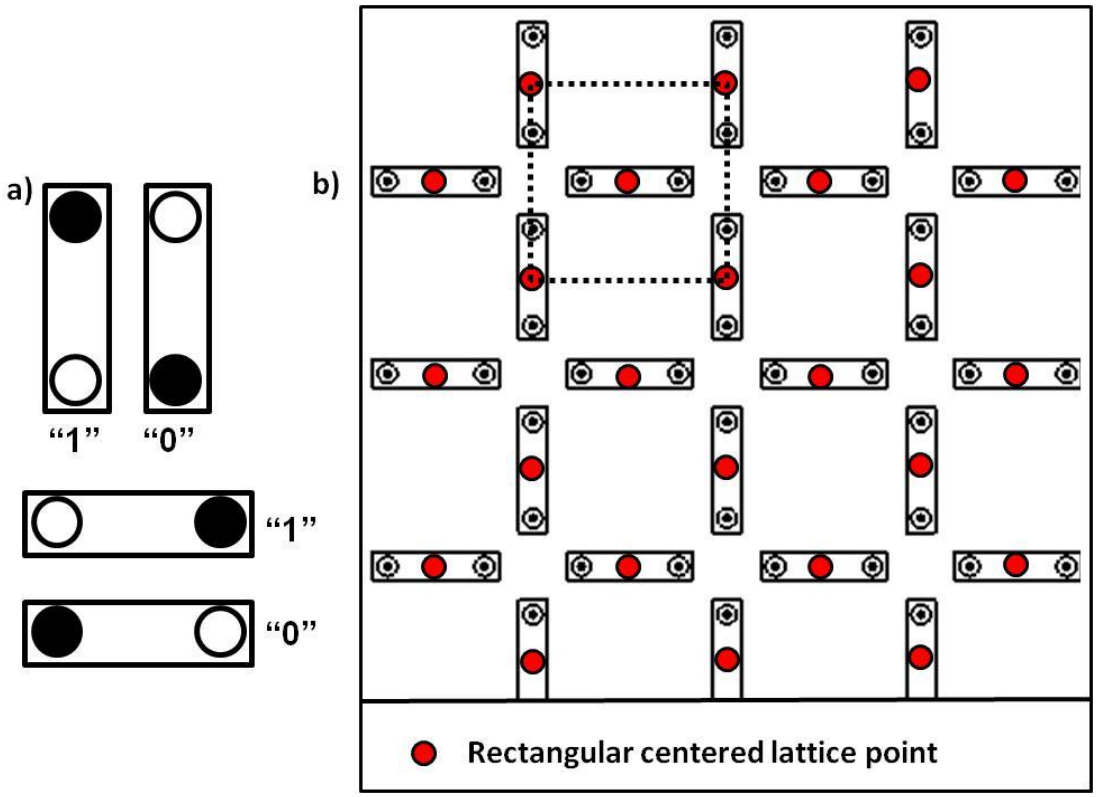


Figure 3-4. a) 2-D 2-dot QCA logic convention b) Completely populated 2-dot QCA "map" with lattice points placed on the cells for illustration purposes only

3.3 Logic design using 2-D 2-Dot QCA

The traditional QCA architecture utilizes the majority gate, which, along with an inverter, provides logically complete computation along with allowing for several interesting logic constructs to be designed [29, 42, 105, 106, 107]. The following section will recreate the complete logic of the traditional designs by introducing five new constructs to the 2-dot QCA architecture. These constructs are: the binary wire, the fan-out gate, the inverter, the planer wire crossing, and the majority gate. Together with the delay flip-flop, they will bring the 2-dot QCA architecture logically on par with the traditional architecture. However, it should

be pointed out that the 2-dot QCA constructs will require less dots and electrons for the implementation of the same logic function and will reside in the rectangular centered 2-D QCA map.

3.3.1 The binary wire

The first of a group of fundamental logic constructs is the binary wire. The wire consists of a string of like-oriented 2-dot QCA with the adjacent opposite oriented sites uninhabited by QCAs. During switching, each QCA passes the information to its adjacent QCA cell, starting at the input QCA and continuing throughout the wire.

3.3.2 Inverter

The next fundamental logic construct to be introduced is the inverter. There are at least two ways to invert a signal in the 2-dot QCA architecture. For the first way, one oppositely oriented QCA is placed in a position next to the binary wire between two like oriented QCAs. This QCA, in turn, passes the information on to the next QCA except now the binary information is inverted. This inverter can be seen in Figure 3-6b. The second way to invert a bit in the 2-dot QCA architecture is by “turning a corner” in the correct direction. Of the four possible ways to turn a corner, two produce inverted signals, and two produce original signals. An example of this can be seen in Figure 3-5.

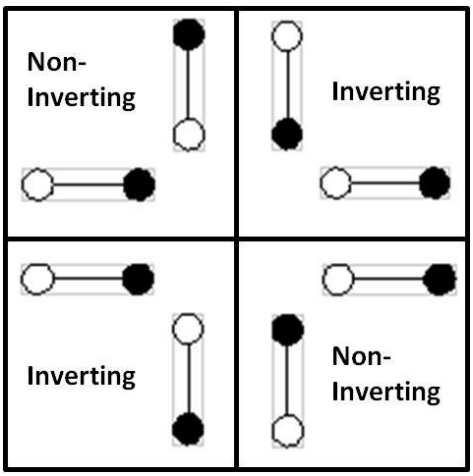


Figure 3-5. Direction of inverting corners

3.3.3 The fan out gate

Fan-out is important in computing systems as a means of using the same bits of information to drive more than one logic operation. For the 2-dot QCA architecture, fan-out gates consist of two branches coming perpendicular off of a central input driver. Then, another perpendicular branch sends the information in the original direction. The second perpendicular branch is important due to the fact that one side of the fan-out gate will be inverted after the first branch. Of course, inverters can be used to transform the bit back to its original state if the direction used in the second branch is undesired. An example fan-out gate is shown in Figure 3-6c.

3.3.4 The 2-D 2-dot planer wire crossing

Because of the unique structure of the 2-dot QCA architecture shown, it is possible to cross wires without adding another level or dimension to the structure. This is accomplished by using QCA wires which are using different

clocks. For example, two QCA wires which cross at a point (shown in Figure 3-6d) do not affect each other unless they are using the same clock. This allows the clock 1 wire to pass unaffected by the clock 3 wire. In general, this effect holds true for any clocking scheme for a wire crossing, as long as the wires are not using the same clock. The ability to clock individual QCA or groups of QCA independent of other, possibly adjacent, QCA is assumed for this planer wire crossing scheme. Clocking with this precision may prove to be a challenge, especially for molecular scale implementations; however, the architecture is flexible enough to allow for other constructs based on other wire crossing schemes, such as multilayer crossing, if it becomes necessary.

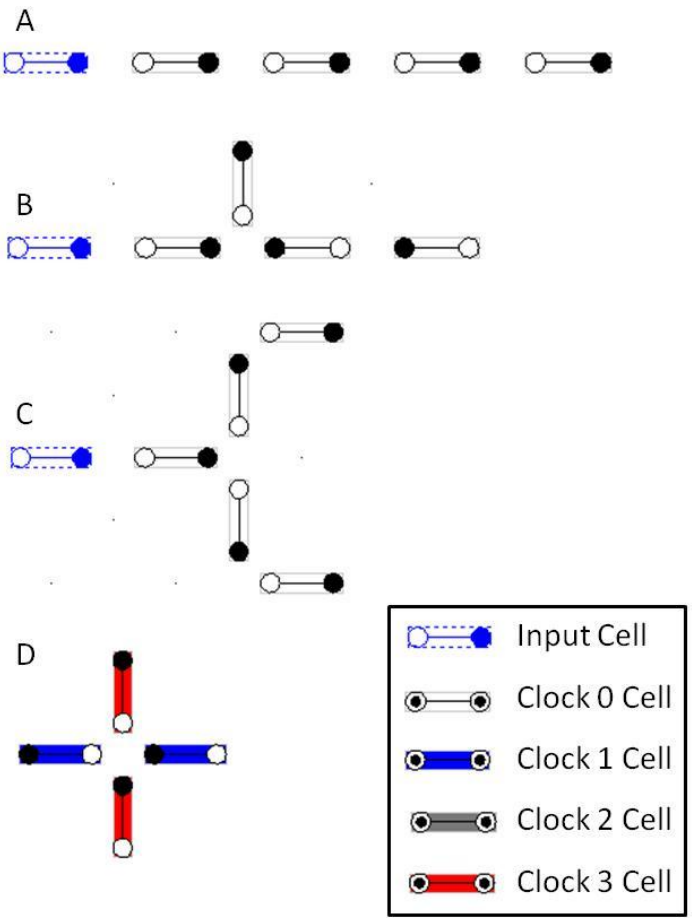


Figure 3-6. Fundamental logic constructs: a) Binary wire b) Inverter c) Fan-out gate d) Planer wire crossing.

3.3.5 The majority gate

The addition of a majority gate into the fundamental logical constructs already presented for the 2-dot QCA architecture creates a logically complete set of primitives. Before the majority gate is presented however, it is required that sufficient explanation of the terms used to describe the majority gate must be given. First, “global inputs” are individual QCAs which are locked into their respective logic configurations. This type of QCA is common to all QCA architectures and could be implemented either by an external user input or a

specifically created cell which is inherently fixed in regards to its electron configuration. “Local inputs” are cells which serve as inputs to a specific logic construct but are not external circuit inputs and are not fixed. Thus, these cells have variable electron configurations which add to the total energy evolution of the system. “Outputs” must always have variable electron configurations and must also be assumed to dynamically contribute to total system configurations.

Like the 2-dot QCA architecture in general, the 2-dot QCA majority gate allows for greater control over its operation than the traditional QCA majority gate. This is accomplished by the use of clocking, orientation, and global and local inputs. The simplest 2-dot QCA majority gate can be created with only 4 2-dot QCA cells. Shown in Figure 3-7b, three of these QCA are held as global inputs (denoted by the blue dashed outline). The single output QCA must be either clocked where it is driven by the inputs or, since the global inputs do not change, they may also be clocked using the same clock signal. The first clue that the 2-dot QCA variety of the majority gate will be different than the traditional QCA variety is that the top input to the majority gate is naturally inverted in its addition to the majority logic. This is due to properties which invert signals as they turn corners in a specific direction (which is also used in the inverter of Figure 3-6b). This simple majority gate can be used to create two-input AND and OR gates by using the top input to “program” which gate is needed. For example, if a static logic 1 is applied to the top input and variable inputs “A” and “B” are applied to the bottom and left inputs, the operation of the gate is an AND(A,B) gate. If the same orientation has instead a logic 0 applied

to the bottom input the operation of the gate is an OR(A,B) gate. (Note that because the top input is inverted, the typical majority gate logic of adding a static “1” to one input to produce an OR gate and adding a static “0” to one input to produce an AND gate is itself inverted.) The simple 2-dot QCA majority gate can also be used to create gates which perform the AND(A’,B) and OR(A’,B) operations by adding the static input to the bottom or left inputs instead of the bottom input. Additionally, this majority gate can also be used as an inverter if opposite static inputs are applied to the bottom and left inputs and the bottom input is reserved for a variable input. The fact that this majority gate can be both an AND gate, an OR gate, or an inverter allows the 2-dot QCA majority gate to be in itself a logically complete gate.

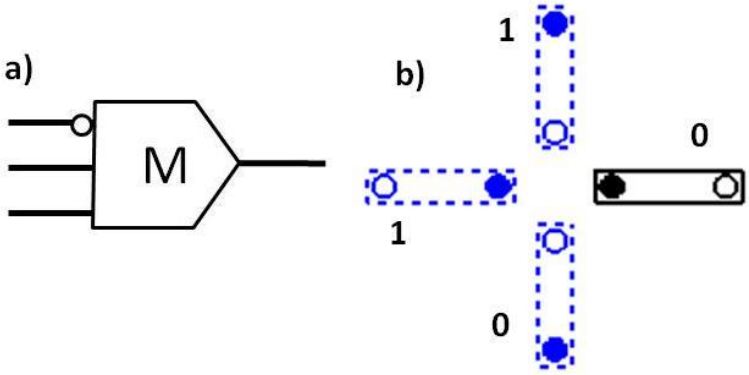


Figure 3-7. a) Schematic for the simplest of 2-dot QCA majority gates b) implementation of this majority gate

The vast majority of complex circuitry will require that global inputs are not applied directly to individual majority gates. However, converting global inputs to local inputs can modify the logical function produced. This is due to the configuration of the 2-dot QCA map which places diagonally neighboring cells closer in spacing (thus giving them greater influence) compared to collinear or

parallel neighbor cells. An example of this can be found in the following majority gate configuration, in which, the local input sites are driven by collinear global inputs (simulating short collinear wires). The operation of this majority gate, shown in Figure 3-8, does something interesting. It changes its function from the gate of Figure 3-7 to a majority gate with the top - and also left - inputs inverted. This interesting feature is due to the majority gate “rejecting” local inputs of the gate. For this layout, the four local cells making up the majority gate (3 local inputs and 1 local output) prefer only two different configurations. Because of the strength of the interaction of the local cells and relative weakness of the collinear wires driving them, they reject single inputs. (This is shown in Figure 3-8b where the left input is rejected by the majority gate.) This is the property that produces the modified majority gate function, which can be used to create a NAND gate, a NOR gate, an AND(A’,B) gate, an OR(A, B’)gate or an inverter and is thus, in itself, a universal logic gate as well.

Clocking can also be used to change the action of the majority gate. Using the same QCA orientation found in Figure 3-8 we can recover the operation of the majority gate in Figure 3-7. We do this by clocking the cells so that the inputs drive the output. Other clocking and orientation schemes produce similar logic gate operations to the gates shown in Figure 3-7 and Figure 3-8. These different schemes for producing different types of majority gates begin to show and unlock the complexity of the 2-dot QCA architecture. This complexity and richness will be used as the more complex constructs are formed.

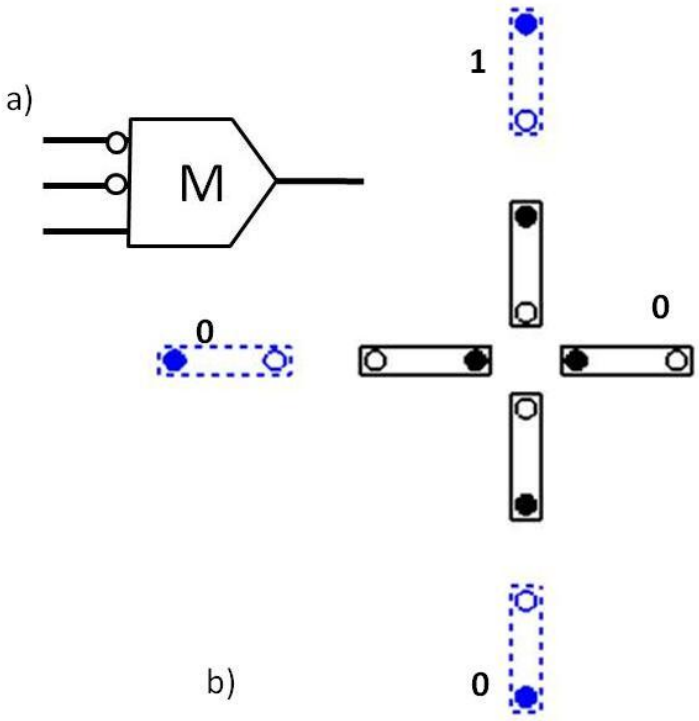


Figure 3-8. Majority gate with global inputs which are removed from the local input sites a) Schematic b) 2-dot QCA implementation

3.3.6 The delay flip flop (D-FF)

The previous five logic constructs can form any desired combinational logic element. However, for sequential logic another construct is needed. The simplest sequential element is the delay flip-flop, or D-FF. The D-FF simply passes, as an output, the bit state of the input after one complete clock cycle. The D-FF implementation in the 2-dot QCA logic looks very much like a binary wire, except that its 2-dot QCA cells are each found to be using different clocks. An example of a D-FF can be found in Figure 3-9. This is the first construct which uses all of the possible QCA clocks and has at least one element found in each. Other more complex constructs will have this same property but might

not be intended to be sequential constructs. This interesting aspect is shared by all QCA architectures which is different from modern IC design, in that every QCA is clocked, even those used in combinational type circuitry like majority gates. This property will allow the architecture to provide both the combinational and sequential circuitry using the same integrated QCA and will be demonstrated in the following two sections.

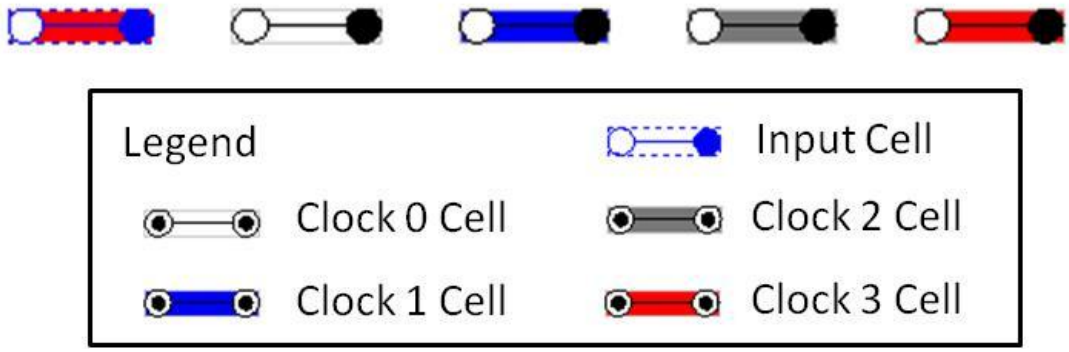


Figure 3-9. Delay flip-flop implementation in the 2-dot QCA

3.3.7 The XOR gate

The XOR gate is a standard two-input gate which produces a logic “1” output when its two inputs are different and a logic “0” output when its two inputs are the same. Owing to the inherent properties of QCA, a simple QCA logic construct has not been found to produce the XOR gate. Therefore, a design based on majority gates has been developed in part to demonstrate the use of majority gate based logic. The functional design of the XOR gate is shown in Figure 3-10 along with its implementation in the 2-dot QCA, and logical trace of its functionality.

This gate also serves to show some important aspects of the 2-dot QCA design; including how corner inversion is handled and also how information is propagated using the four clocks. In the first and second “stages” of the XOR gate, the two signals, “A” and “B”, are passed to majority gates in their original and inverted form, with one input being inverted for each gate. In the third and fourth stages, the output of this first group of majority gates is used to drive the local inputs of the last majority gate. (Note the wire crossing of input “B” which requires the output of the top majority gate to have a different clock than this input.) The fifth stage produces the output of the last majority gate and provides the XOR output as well. In this circuit, the configuration of each of the majority gates produces the same logic function with an inverted top input and non-inverted left and top inputs (the same operation that can be found in Figure 3-7). If other circuits were connected to this XOR gate and the programming inputs to the majority gates were not global inputs, the operation (and thus required layout of the QCA) might be slightly altered. In general, it is important to note that while the operation of all logic operations can be easily generated without global inputs, it might not correspond to the exact circuitry which is developed when using global inputs (as has been discussed).

It is also interesting to note that the circuit here may be “reprogrammed” to provide different operations. For instance, the XNOR operation can be generated by inverting all of the programming inputs to the majority gates, or the circuit can produce a constant “1” or “0” output, also with a change to the

programming inputs. This reconfigurability is easily verifiable with some simple logic calculations by using the schematic in Figure 3-10.

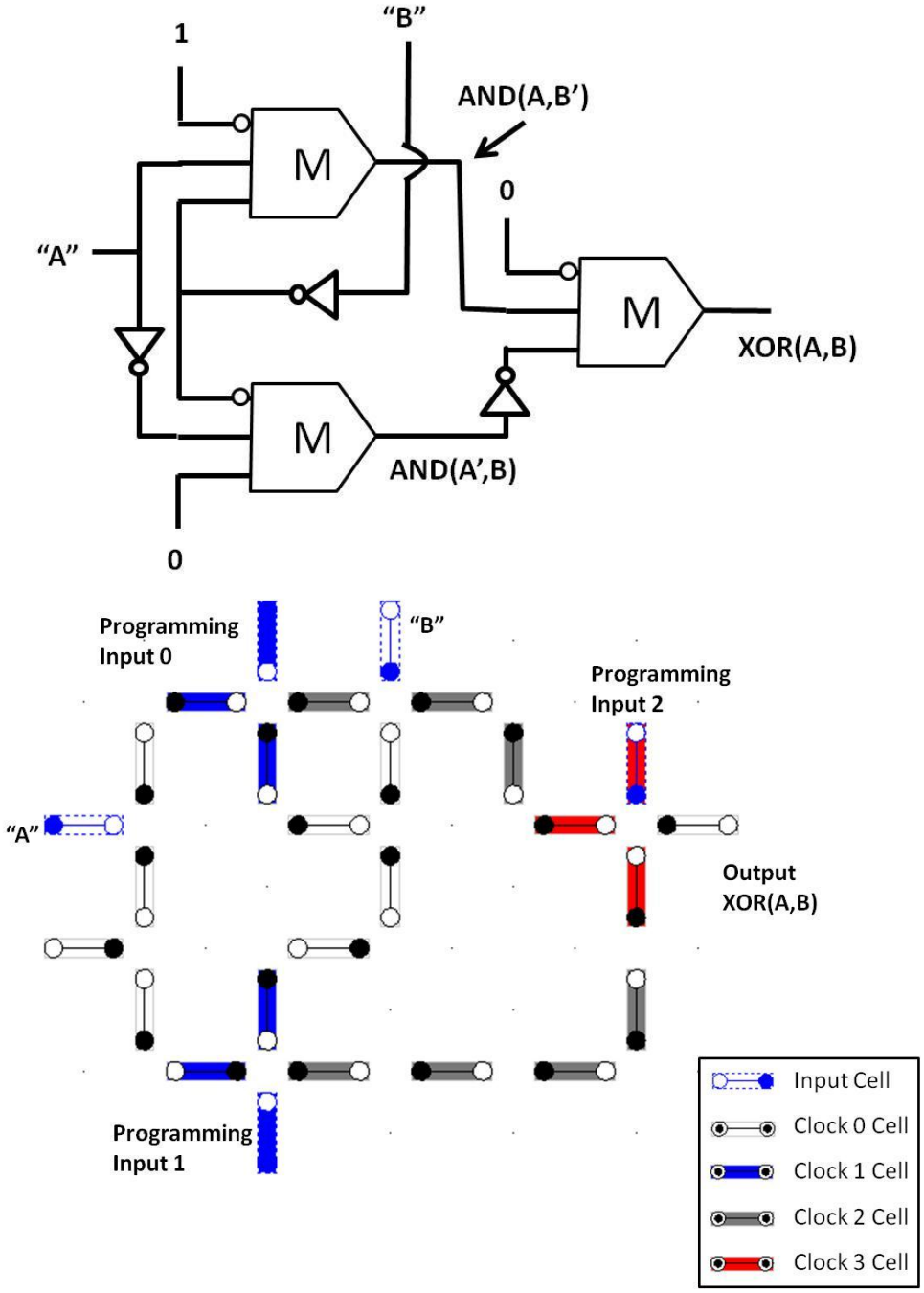


Figure 3-10. Majority gate based XOR gate using 2-dot QCA cells along with its schematic

3.3.8 The Toggle Flip-Flop

The toggle flip-flop or T-FF is a sequential circuit in which the output is toggled when its only input is set to a one, or the output remains constant as long as the input is a logic “0”. This circuit can be created by connecting the XOR output to the “B” input of the circuit in Figure 3-10. Its implementation is shown in Figure 3-11 and provides an example of many important characteristics of a sequential circuit using the proposed 2-dot QCA architecture.

This circuit also provides an interesting example of a QCA specific sequential design method in which a combinational circuit can become a sequential circuit by simply feeding back the output into an input. This is, of course, only possible when the QCA clock for the output is the same as the input QCA or drives the input QCA.

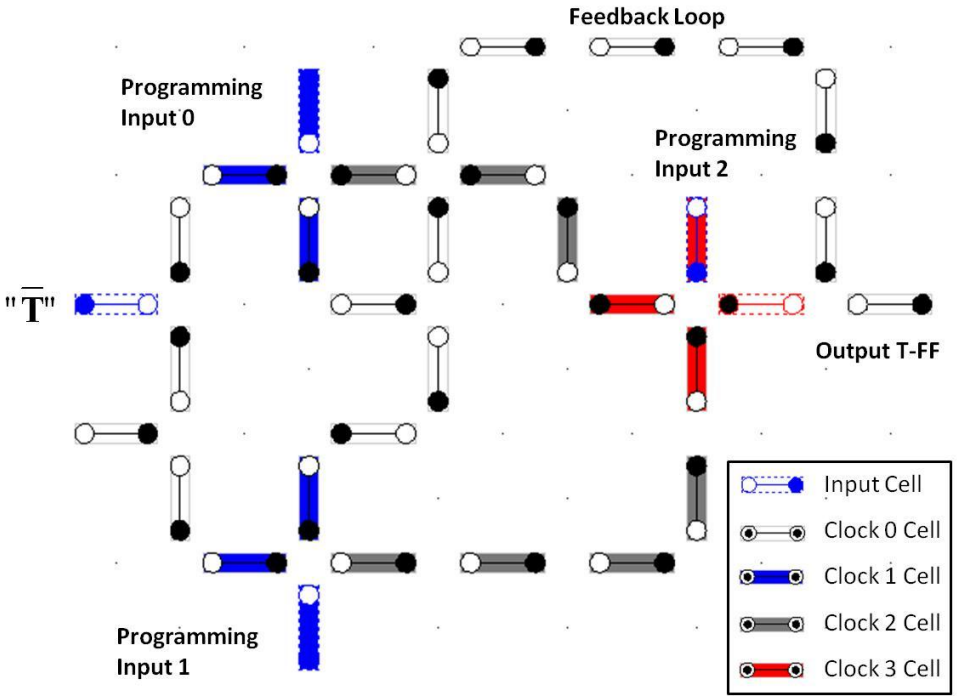


Figure 3-11. 2-dot QCA implementation of Toggle Flip-Flop

3.4 Chapter Summary

This chapter has presented a new architecture, based on the lattice structure of naturally occurring and artificial self-assembled materials and 2-dot QCA cells. When compared to the traditional QCA cell designs, 2-dot cells offer advantages at size scales required to make them a viable replacement to CMOS. Functionally complete sets of logic constructs which can implement any combinational and sequential logic were developed. These new QCA constructs demonstrate a rich and flexible nature of the 2-D 2-dot QCA architecture.

Chapter 4

Simulation Methods and 2D 2-Dot QCA Results

4.1 Chapter Introduction

When designing logic constructs for the 2-D 2-dot QCA and resultant LINA architectures it was necessary to use simulation software to verify and aid in their design. Because most, if not all, publically available QCA simulations are set up for the traditional QCA case, new software had to be created to make this possible. However, this new software depends heavily on simulation techniques developed for the traditional QCA architecture and modified to be used with the 2-dot QCA case. This chapter presents the new and modified simulation engines in Sections 4.2- 4.4 and results of these simulations for the 2-D 2-dot case in Section 4.5.

4.2 Simulation Engines

“Ab-Initio” simulations of QCA cells provide very accurate results for at most about two interacting QCA cells. Because of the computational complexity involved, more cells cannot be added to the simulation without increasing the required simulation time beyond practical limits. For this reason, when simulating a larger number of cells, other methods which employ approximations must be used to simplify the calculations. There are many different models which can be generally counted on to give reasonably accurate results for specific aspects of QCA operation. For instance, Coherence vector,

and bistable simulation methods are utilized in software including QCA designer [79, 108], which is a tool used to simulate traditional clocked QCAs. Each of these methods has its own pros and cons but both models provide reasonably accurate logic simulations. Coherence vector simulations are generally accepted as the most accurate simulation engine for clocked QCA due to the quantum mechanical properties which are integrated in the simulations. They also provide information on power, speed, and reliability and include temperature and other electrical properties. For these reasons, coherence vector simulations were chosen to do complex analysis on larger clocked QCA circuits especially LINA. For simpler circuits or circuit elements, traditional statistical mechanical analysis techniques were used to generate Boltzmann distributions to predict correct logical output and temperature dependant reliability. When possible, an exhaustive analysis of all possible circuit states were examined, however, this limits circuit sizes to around 16 cells due to the exponential increase in computing time required for each additional cell added. For slightly larger circuits, Monte Carlo techniques were used to approximate distributions without the exponential increase. These techniques are presented here and results for the statistical mechanical simulation for the 2-D 2-dot architecture.

4.3 Statistical mechanical simulation

The technique to find the statistical mechanical Boltzmann distribution, and therefore provide information on the temperature reliability of QCA circuits, assumes that the QCA clocking mechanism is perfect; thereby, providing

perfectly localized electron wave functions with instantaneous electron transitions. This assumption is thought of as a semi-classical approximation and allows for certain properties of the system to be studied independently and in more detail. The simulation operates by performing the following calculations. In a circuit with N cells, there are 2^N possible circuit states which correspond to all the two-state combination of cells. Each of these possible states has an energy which is calculated as a summation of all of the point charges of the circuit according to (4.1).

$$E_{state} = \sum_{i}^{N-1} \sum_{j>i}^{N} \left(\frac{q_{i1} * q_{j1}}{4\epsilon_0 \epsilon_r r_{i1j1}} + \frac{q_{i1} * q_{j2}}{4\epsilon_0 \epsilon_r r_{i1j2}} + \frac{q_{i2} * q_{j1}}{4\epsilon_0 \epsilon_r r_{i2j1}} + \frac{q_{i2} * q_{j2}}{4\epsilon_0 \epsilon_r r_{i2j2}}\right) \quad \textbf{(4.1)}$$

where, q_{xy} is the amount of charge in cell x at dot location y, r_{iyjz} is the distance between cell i dot location x and cell j dot location y, and $\epsilon_o \epsilon_r$ is the electric permittivity of the material. The configuration with the lowest total energy produced the ground state of the system and resultant correct logic output of the circuit. When degenerate ground state configurations were identified, they were examined to determine if different logical outputs were produced by the degenerate states. If the outputs were the same in each of the degenerate states, the circuit was maintained as an acceptable circuit; if not, then the circuit output was deemed to be random, from a logical sense, and thus unacceptable.

At non-zero temperatures and finite energies, the circuit may deviate from the ground state due to thermally induced state transitions. This effect is probabilistic in nature and dependent on the temperature, or amount of thermal

energy present, and the energy separation between circuit states. It is always found that the most likely single state for a circuit to be in at any given time corresponds to the state with the minimum system energy, or the ground state. For states with higher system energy, or excited states, the ratio of the probability of the circuit being in this state compared to the circuit being in its ground state is calculated with the usual Boltzmann distribution law which states:

$$\frac{P_{excited}}{P_{ground}} = e^{-\frac{(E_{excited} - E_{ground})}{kT}} \quad \textbf{(4.2)}$$

where P_i is the relative probability of the circuit being in the state i, E_i being the energy of state i, k being the Boltzmann constant, and T being the absolute temperature. Since the sum of all of the probabilities must be 1, this equation can be modified to directly calculate the probability of any circuit state as in (4.3).

$$P_i = \frac{e^{-\frac{(E_i - E_{ground})}{kT}}}{\sum_i^{(2^N)} (e^{-\frac{(E_i - E_{ground})}{kT}})} \quad \textbf{(4.3)}$$

This equation does not give the probability of correct logical output directly, however. To know that quantity the logic value of the output cell of each circuit state must be known Furthermore, this value may be correct even for excited circuit states. An example of this is seen in Figure 4-1 where 4 different circuit states consisting of all of the possible configurations of a binary wire is shown. In this figure, the input cell is held constant, (denoted by the blue outline) and the output is taken at the right most 2-dot cell. For this wire, the S_0 configuration

produces the ground state of the system and thus the correct logical output is a logical “1”. The first excited states (S_1 and S_3) produce equal energies configurations which are greater than the ground state by the energy difference between a correctly aligned neighbor and incorrectly aligned neighbor. This difference is known as the “kink” energy (E_{kink}) and is an important parameter when studying different QCA configurations as all energy levels will be an integer multiple of the kink energy above the ground state. The logic level of first excited states is opposite to the correct logical output and thus degraded the probability of correct logical output (PCLO). The highest energy of all of the states occurs for at $2 * E_{kink}$ above the ground state at S_2. Because of its relatively high energy, this state has the least probability of occurring in the example system. However, S_2 also produces a correct logical value at the output and therefore adds to the PCLO for the circuit and thus adds to the circuits overall reliability.

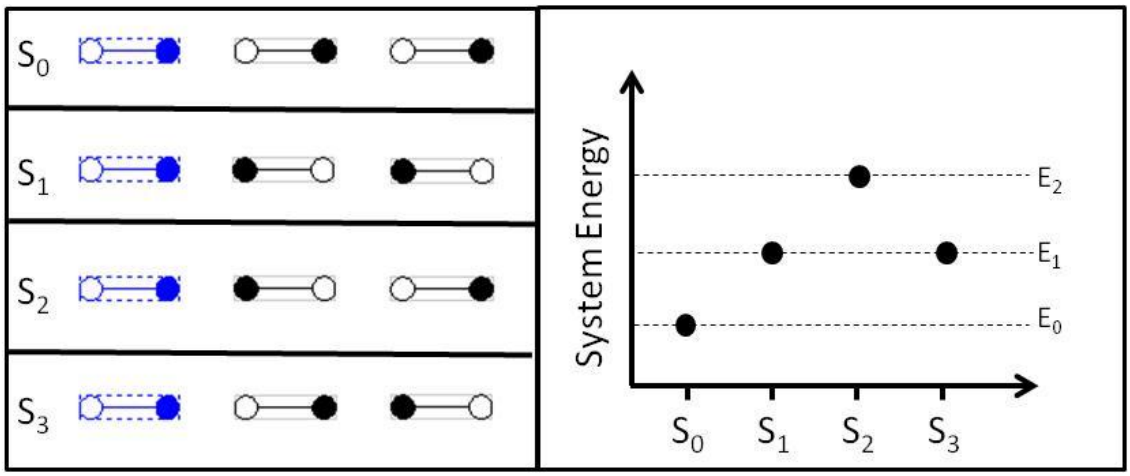


Figure 4-1. Possible circuit states of small binary wire example

In order to factor in the excited states into the PCLO, statistical mechanical equations based on a system in thermodynamic equilibrium is used. The equation, shown in (4.4), produces an expectation value of the output cell which can then be used to calculate the PLCO value.

$$\langle O \rangle = \frac{1}{F} \sum_{i,S_N=-1,1}^{2^{N-1}} S_N e^{\frac{E(i)_{S_N}}{kT}} \quad \textbf{(4.4)}$$

In this equation, F is the partition function for the system, $E(i)_{S_N}$ is the energy of the i^{th} circuit state when the output cell has polarization equal to S_N, and $\langle O \rangle$ is the expectation value of the polarization of the output cell. The canonical partition function for the system is:

$$F = \sum_{i}^{2^{N-1}} e^{\frac{-E(i)}{kT}} \quad \textbf{(4.5)}$$

These equations allow for the probability of correct logical output (PCLO) to be determined which can be used as an effective reliability metric when analyzing alternate circuit geometries, like our 2-D 2-dot layouts, different circuit designs and temperature reliabilities. However, for a more detailed analysis of QCA properties of speed, reliability, power, and logic operation in the presence of a reasonable clocking mechanism a more extensive quantum mechanical simulation is required. The following section presents the “coherence vector” simulation engine that was adapted to be used with the 2-D 2-dot QCA designs.

4.4 Coherence vector simulation

The coherence vector simulation engine is based on a density matrix approach to describe the statistical state of the QCA system. It has the features of being able to model dissipative processes as well as the dynamics of cell switching. For the traditional QCA designs coherence vector simulations assumed that each cell was two state, which is not entirely correct. For the 2-dot designs this assumption is correct and thus provides a more accurate simulation model. Therefore, the two-state Hamiltonian in (4.6) can be constructed for the 2-dot system.

$$H_i = \sum_j \begin{bmatrix} -\frac{1}{2} P_j E_{i,j}^{kink} & -\gamma_i \\ -\gamma_i & \frac{1}{2} P_j E_{i,j}^{kink} \end{bmatrix} \quad \textbf{(4.6)}$$

where $E_{i,j}^{kink}$is the kink energy between cells i and j, P_i is the polarization of cell i, and $\gamma_i$is the tunneling energy of the electrons in cell i. The tunneling energy term, γ_i, is where the clock comes into the Hamiltonian and thus this term varies with clocking zones. As has been discussed with the Boltzmann distribution engine, the kink energy is the difference between the favorable and unfavorable Coulomb interaction in two cell possible cell states. The summation j is over all cells besides i, but can be limited to the cells in a small radius for complex calculations because the dipole-dipole interaction of the cells decays inversely as a power of five of the distance between cells. This allows cell-to-cell interaction which is outside a small neighborhood to be ignored.

The coherence vector, λ, is a vector representation of the density matrix, ρ, of a cell, projected onto the basis spanned by the identity matrix and Pauli spin matrices σ_x, σ_y and σ_z. The components of λ are found by taking the trace of the density matrix multiplied by each of the Pauli matrices such as in (4.7).

$$\lambda_i = Tr\{\hat{\rho}\hat{\sigma}_i\} \qquad i = \{x, y, z\} \tag{4.7}$$

The polarization of cell i, P_i, is then the z component of the coherence vector as in (4.8).

$$P_i = \lambda_{z,i} \tag{4.8}$$

The Hamiltonian must also be projected onto the spin matrices as in (4.9).

$$\Gamma_i = \frac{Tr\{\hat{H}\hat{\sigma}_i\}}{\hbar} \qquad i = \{x, y, z\} \tag{4.9}$$

The Γ vector represents the energy environment of the cell and includes the effects of the neighboring cells. Γ can also be evaluated explicitly as in (4.10).

$$\vec{\Gamma} = \frac{1}{\hbar}\left[-2\gamma, 0, \sum_j E_{i,j}^{kink} P_j\right] \tag{4.10}$$

The equation of motion for the coherence vector including the dissipative effects is:

$$\frac{\partial}{\partial t}\vec{\lambda} = \vec{\Gamma} \times \vec{\lambda} - \frac{1}{\tau}(\vec{\lambda} - \vec{\lambda}_{ss}) \tag{4.11}$$

Here τ is the relaxation time representing the dissipation to the environment. λ_{ss} is the steady state coherence vector defined as:

$$\vec{\lambda}_{ss} = -\frac{\vec{\Gamma}}{|\vec{\Gamma}|}\tanh(\Delta) \tag{4.12}$$

where Δ is the where the temperature comes in and is defined as the temperature ratio. It is equal to:

$$\Delta = \frac{\hbar\left|\vec{\Gamma}\right|}{2k_B T} \quad \textbf{(4.13)}$$

The simulation evaluates the equation of motion using an explicit time marching algorithm where Γ and λ_{ss} are evaluated at each time step and the coherence vector then stepped forward in time. Further information on the coherence vector simulation and the time marching algorithm can be found in [109].

Additionally, the results of this simulation method are supplemented with calculations originally performed in [60, 100]. These new calculations separate power elements analogous to "leakage" and "switching" power in CMOS, which is important to the range of power values which may be required during worst case events.

The coherence vector calculations provide a more complete view of complex QCA circuits which allows the analysis found in following chapters on LINA (including the power/speed/reliability tradeoffs to be achieved). The next section take a step back however, and discuss results obtained for simple 2-D 2-dot circuits running Boltzmann distributions.

4.5 Comparison of 2-dot and traditional QCA wire

Analysis of different variants of the QCA binary wire begins with an assumption of parameters which define the geometry of the given cells. For instance, given the QCA cell-to-cell distance (L) (which is the minimum distance between dots of different cells), and intracellular dot spacing (D) (the minimum distance

between dots of the same cell), a particular QCA binary wire requires a certain number, N, of cells to communicate information down a fixed length. This number N is also dependant on the type of layout geometry which spans the distance. For example, 2-dot QCA cells which are laid out perpendicular to the direction of information propagation (shown in Figure 4-2a) will require more cells than 2-dot cells which are laid out parallel to the direction of information propagation (shown in Figure 4-2b). This factor becomes important when analyzing traditional and 2-D 2-dot QCA types because traditional QCA utilize the perpendicular approach (with two "half cells" making up the full cell also shown in Figure 2-6d) and 2-D QCA utilize the parallel approach. However, in order to compare these two approaches without bias the same cellular structure is used and thus the half cell parts are treated as 2-dot full cells such as has been proposed in this dissertation.

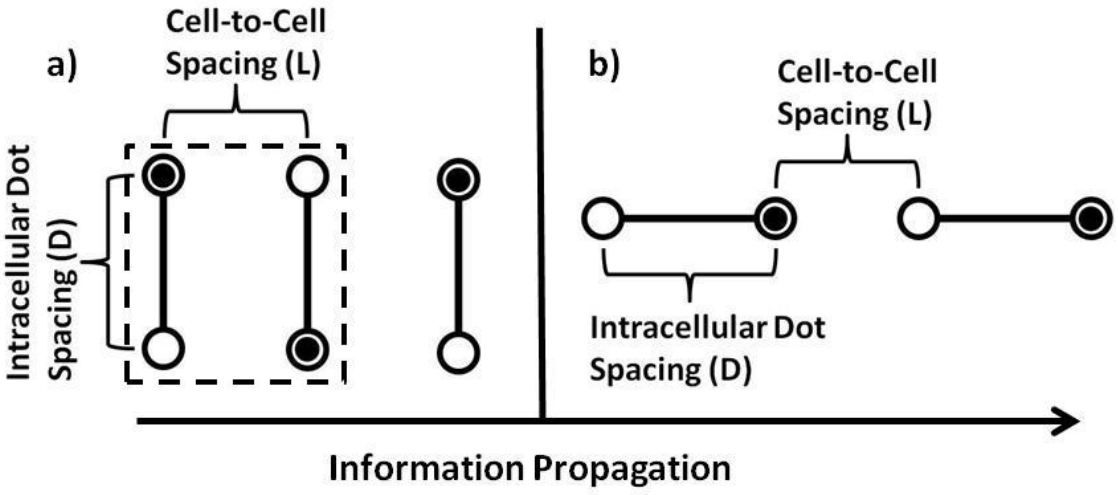


Figure 4-2. a) Traditional QCA layout used by four dot designs b) Parallel 2-D 2-dot QCA wire design

So, if the cells of the wire are arranged from 1 to N, (and 1 to M for the traditional cell layouts) increasing in number sequentially, and cell 1 is held constant to provide the driving input of the circuit, then the wire output is taken from cell N (or M). For the traditional QCA layout, the correct operation of each successive QCA half-cell is to invert the signal of the previous cell as the signal is carried down the line. So, if M is an even number the correct output of the wire would be an inversion of the input state and thus the probability of the inverted input would be analyzed as the PCLO. However, if M is an odd number the correct output of the wire would be the same as the input state. For the case of the 2-D 2-dot QCA layout the output is always the same state as the input cell regardless of wire length as long as the wire's cells are collinear.

4.5.1 Wire comparison simulation results

Three different analyses were done with cells of different dimensions, which were chosen to be consistent with literature for current and proposed semiconductor and molecular fabrications. In each of the sets of data the parallel or "collinear" wires were found to be more robust than traditional four-dot designs for equal wire length as has been previously mentioned. This result allows either the device to perform more reliably at higher temperatures or wire lengths to be longer for a given temperature for the collinear case.

The first cell design is based on proposed molecular QCA dimensions, found in [61], of D=L=1nm with an $\epsilon_r = 1$ (results shown in Figure 4-3). This data shows that the output expectation values for the collinear wires are closer to the ideal of -1 at all temperatures and thus more robust than traditional four-dot wires of

equal length. The data also shows that as the temperature increases the deviation from the traditional and 2-D designs gets larger. This indicates that the 2-D designs are also more resistant to changes in temperature. It must also be noted that reliable room temperature operation for each of these design types, at these L and D scales, is predicted to be possible by analyzing the data and the breakdown temperatures for each is likely well above any possible operational temperature. However, the additional advantages of the 2-D layout must also be factored in for a complete comparison of these two designs.

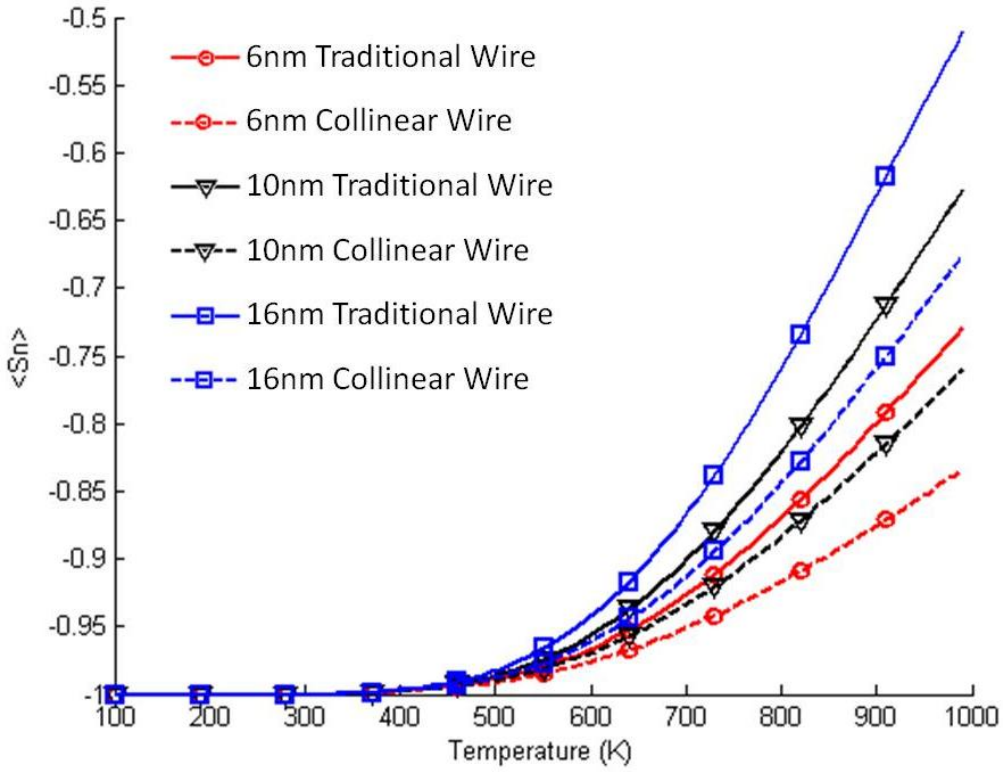


Figure 4-3. D=L=1nm QCA cell wire expectation vs. temperature

The next analysis set is based on proposed dimensions for GaAs/AlGaAs semiconductor quantum dot structures of D=L=40nm with $\epsilon_r = 12.9$ [110].

These QCA cell dimensions show very high susceptibility to thermal effects and degradation of reliability of all the wire lengths tested above 1K. The collinear wires do again show improved results over the traditional designs in Figure 4-4. One interesting result is that the data for the 400nm collinear wire is nearly overlaid with that for the 240nm traditional wire demonstrating increased maximum wire length for any required fidelity.

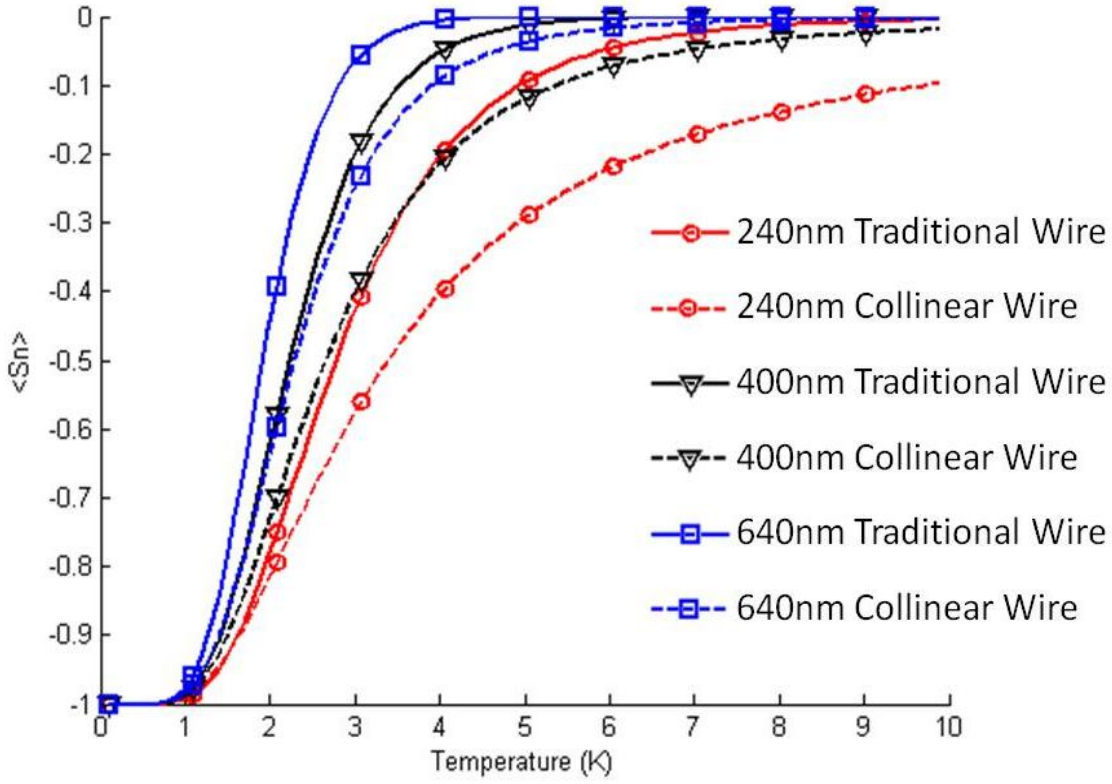


Figure 4-4. D=L=40nm QCA cell wire expectation vs. temperature

Finally, a compromise dimension of L=D=5nm denoting another possible future QCA realization is shown. Even at these relatively small scales, the length of wires is limited at room temperature by thermal effects (as shown in Figure 4-5). However, it has been proposed that devices cooled to liquid nitrogen

temperatures (~77K) may become a viable alternative until molecular operation is possible. The further results using these size scales show similar patterns to the other wire dimensions tested with improved reliability for the collinear wire designs.

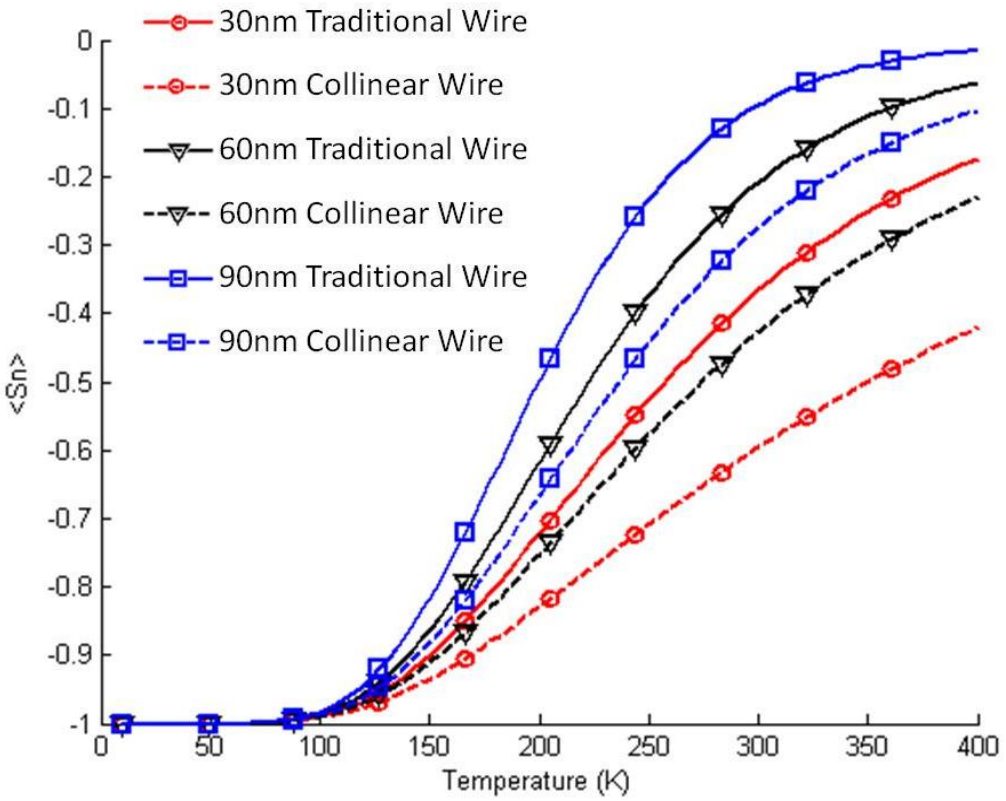


Figure 4-5. D=L=5nm QCA cell wire expectation vs. temperature

4.5.2 Thermodynamic analysis of 2-D 2-dot majority gates

It is clear by reviewing the data of the previous section that 2-D binary wire layouts provide benefits in robustness in the presence of thermal noise and consequently more reliable operation at finite temperatures when compared to traditional designs. It is also important to analyze the 2-D 2-dot majority gate with this method as well in order to complete the investigation. Therefore, the

majority gate design of Figure 3-8 was utilized. The results are shown in Figure 4-6 for two different sets of spacings corresponding to the molecular 1nm spacing and the compromise 5nm spacing. The results continue to show the thermal robustness of the 1nm cells and possibility of room temperature operation at these scales and the liquid nitrogen operation temperature of the 5nm cells. This confirms what has been seen with the binary wire and allows for the extension of these results to complete 2-D circuitry.

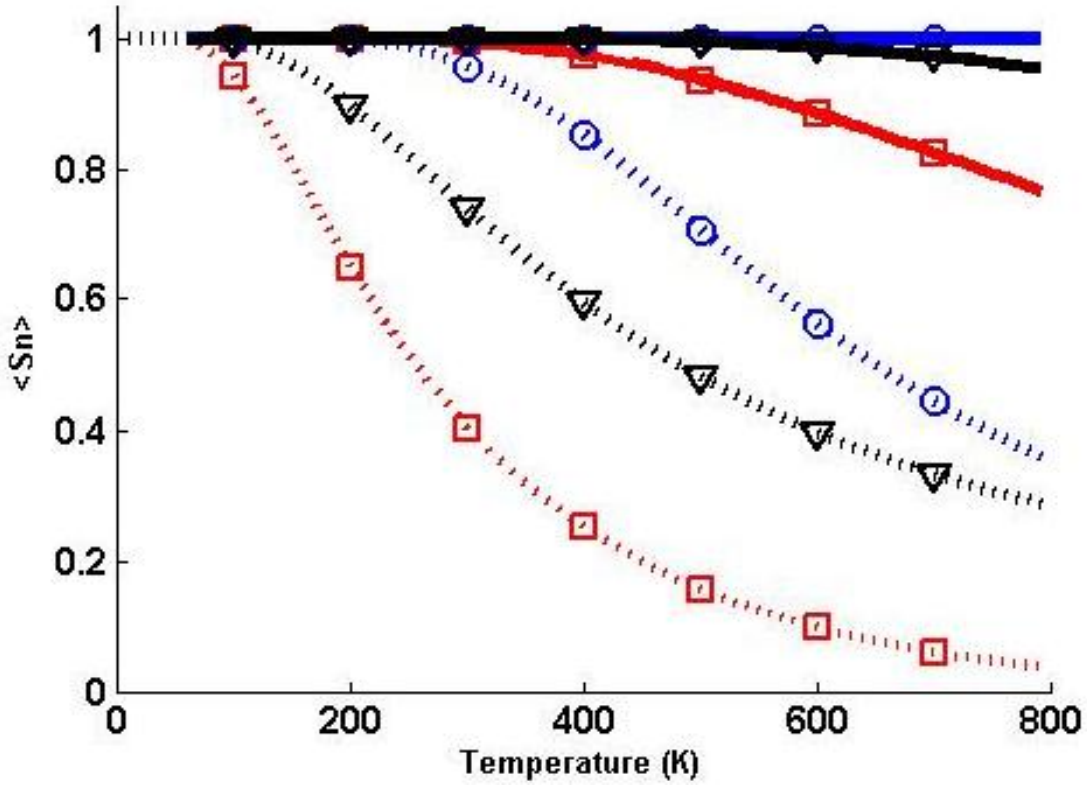


Figure 4-6. Thermodynamic analysis of universal logic gate of Figure 3-8 for devices with D=L=1nm (solid lines) and D=L=5nm (dotted lines) with different inputs given to the gate (circles indicate all inputs favorable to the output, triangles indicate perpendicular (to output QCA) input rejection and squares indicate collinear (to output) input rejection

4.6 Chapter Summary

In this chapter calculations based on statistical Boltzmann distributions were developed for 2-D 2-dot cells. Additionally, coherence vector calculations were presented which give more in-depth results and also show power and speed potential of 2-dot QCA circuitry. The results of these calculations provided insight into how the reliability of 2-D 2-dot binary wires as well as majority gates are affected by temperature and cellular and circuit geometries. These results also showed reliability advantages over traditional QCA designs with similar cell and dot spacings.

Chapter 5

Lattice-based Integrated-Signal Nanocellular Automata (LINA)

The 2-D 2-dot QCA architecture has been shown to provide advantages in terms of reliability of components and the hope for viable implementation strategies. Furthermore, this new architecture has been shown to be functionally equivalent to traditional QCA designs. However, challenges remain to the realization of large-scale room-temperature QCA, including 2-D 2-dot QCA designs, for experimentation in the near future and commercialization beyond that. For this reason, research was conducted into techniques to improve the reliability of 2-D 2-dot QCA to the point where cells constructed using nanoparticles, of the size scale currently available, may be used for fabrication. The result of this research is realized in the Lattice-based Integrated-signal Nanocellular Automata (LINA) design variant. LINA uses integrated signals to boost reliabilities even more than could be achieved with traditional redundant designs, while also allowing for flexibility of design which may allow for currently available large scale patterning technologies. LINA theory and new logical constructs designed for LINA will be introduced in this chapter along with simulation results of the improvements LINA provides. This chapter proceeds as follows: Section 5.1 will discuss the theory and advantages of LINA, Section 5.2 will discuss the basic logic and communication structures of which the paradigm is built.

5.1 Theory and Advantages of LINA

One of the most pressing challenges facing the implementation of room temperature electric QCA into large reliable circuits is the precise deposition and patterning of single nanometer sized molecules into structures which perform useful communication and logic. Single nanometer sized molecules are required to increase energy separation between ground and excited cell states above error producing thermal noise for all previously proposed QCA designs. Research using a mixture of self-assembly and patterning on DNA tiles is promising, but currently has issues at the required size scales and integration levels [63]. Specifically, the electron beam lithography (EBL) used does not scale well to mass production techniques for VLSI circuitry, and the resultant DNA tile cells were on the order of 10nm which is still too large to enable room-temperature operation of previous QCA designs. In general, techniques to deposit and pattern molecules on the required size scale and with the precise placement of traditional QCA designs remain very difficult if not impossible in the near term.

One reason for this difficulty lies in traditional QCA cellular designs, and the resultant circuit layouts, which utilize some circuit design methods developed for other technologies. 2-D 2-dot cells with lattice positioning found in Figure 3-3 have been presented in Chapter 3, thereby producing a method in which the relative cellular layout can be achieved. However, the ability to pattern large scale complex circuit layouts on this small cellular size scale is not available for most large scale lithography techniques. Additionally, the 2-D 2-dot QCA

designs do not account for common fabrication defects such as cell deletion, misalignment, or other fault mechanisms, commonly found with any self-assembly process. LINA attempts to advance the transition to lattice based QCA designs by adding “width” to the communication and logic structures and “integrated signals” to communication and logic structures. The increased width allows for robustness in the presence of the self-assembly circuit layout errors and flexibility to adjust structure widths based on large scale patterning technologies. The additional integrated signals have the effect of increasing reliability by taking advantage of the inherent majority property of QCA to self-correct logical errors due to thermal noise, stray charge, fabrication defect, or other probabilistic error process. The increased reliability also allows for larger cell sizes and cell spacings (possibly greater than 20nm), to be utilized for reliable room-temperature operation, which may allow for other larger nanoparticles, to be utilized in the role of a LINA QCA cell. This last attribute of LINA would greatly increase the likelihood of full scale QCA nanoelectronics by opening up fabrication to a much larger group of well understood and currently available materials.

Redundant QCA designs have been previously proposed which advocate for the use of triple modular redundancy or *n*-modular redundancy in some cases [93]. The integrated signals of the LINA designs communicate extra information, much like redundant designs would, but advance the concept by restoring and repairing signals continually and allowing for multiple paths for each individual signal. Additionally, due to the unique geometries of these

integrated signal designs, they do not require condensing the multiple signals into a single wire or cell for input to logic. This is possible because LINA gates are able to accept each of the full integrated-signal wires as separate inputs. This allows for robust communication and logic structures and removes weak points which are susceptible to logical faults. Additionally, the structure of the integrated signal wires and gates does not require complicated layouts with additional wire crossings, which is a major drawback to traditional redundant designs.

The structure of the integrated signal wires can be seen in Figure 5-1, where three different possible wire widths are shown. The term “wire width” or “n-wide” is in reference to the number of integrated signals which are contained in the wire and not to its geometrical width. For example, the wire of Figure 5-1B has a width of 3 (making it a “3-wide” wire) even though the geometrical width is 7 times the lattice spacing. In general LINA wires can be made any odd integer number width providing design flexibility for increased reliability or to fit with clocking or patterning technologies.

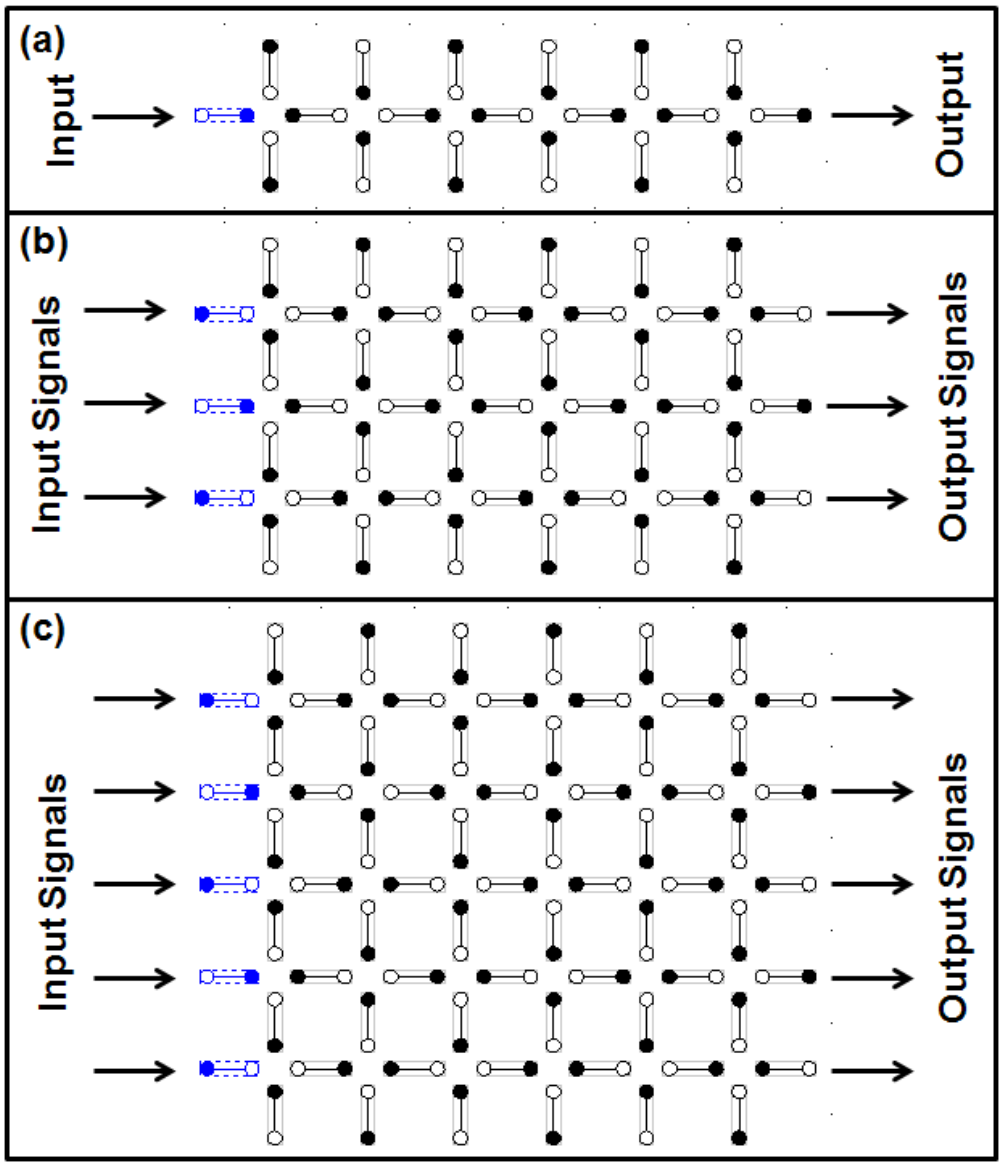


Figure 5-1. (a) 1-wide LINA wire (b) 3-wide LINA wire (c) 5-wide LINA wire

5.1.1 LINA design convention

The addition of integrated signals to the design adds complexity due to the fact that the information carried by LINA wires must be understood based not only on cell state, but also geometric position. Another added complexity arises in the fact that LINA utilize two cellular orientations in the lattice arrangement,

such as was also seen in the 2-D 2-dot designs of Chapter 3. Therefore, in order to be able to quantify and study the operation of LINA wires and gates, a convention will be developed based on the geometrical layout shown in Figure 5-2. In this convention, the binary state of the cell is determined by the position of the free electron as developed for 2-D 2-dot QCA and shown in Figure 3-4. When the electron is in the positive location, according to the axis parallel to the cell's orientation, the cell is given the binary value of 1 and polarization of +1. When the electron is in the negative direction, the cell is given the binary "0" value and polarization of -1.

The convention also dictates that the origin of the coordinate plane (0,0) is taken as the center cell of the input plane of a wire or gate, regardless of width. From there, the axes must be positioned along the directions of the two cellular orientations. This convention allows for the wire shown in Figure 5-2 to be given the binary value of 1, due to the value of the cell at the coordinate origin. The scale of the axes is based on a common cellular lattice spacing (L) which directly corresponds to the eventual intercellular spacing and along with the intracellular-dot spacing (D) provides the position of the cells' component parts.

With this convention in hand, the expected binary value of the remaining cells of the wire can be found with (5.1) where $V_{x,y}$ is the binary value of the cell at position (x,y). For example, in the figure, the cell at position (0,0) has a binary value of 1 (so $V_{0,0} = 1$). Therefore, using (5.1) we can surmise the expected binary value of the cell at (2,-2) to be ($V_{2,-2} = V_{0,0} = 1$) because ($-2 - 2 =$

-4) & ($-4\ mod 4 = 0$). Likewise, for the cell at (3,5), the expected binary value ($V_{3,1} = \bar{V}_{0,0} = 1$) because ($1 - 3 = -2$) & ($-2\ mod 4 = 2$).

$$V_{x,y} = \begin{cases} V_{0,0}, & (y-x) mod\ 4 == 0 \\ \overline{V_{0,0}}, & (y-x) mod\ 4 == 2 \end{cases} \quad \textbf{(5.1)}$$

In addition, the correct binary value of any true output plane of a LINA circuit will be the expected value of the center cell on the output plane. Furthermore, the total probability of correct logical output (PCLO) of this output can be obtained with knowledge of the individual probability of all the cells of having their respective expected logical values. The individual probabilities are combined through the use of the probabilistic ensemble majority voting methods, such as shown for an 3-wide wire in (5.2) where P_i is the probability for $Cell_i$ (here $Cell_1$, $Cell_2$, and $Cell_3$ are the output cells) and P_{Total} is the total output PCLO. For example, if the individual expected logic value probabilities of the three output signals in the wire in Figure 5-1B are .95, .97, and .95, then P_{Total} would be equal to .99465 according to (5.2).

$$P_{Total} = \sum_{i=1,(j\neq k\neq i)}^{3} ((1 - P_i)\, P_j P_k) + P_1 P_2 P_3 \quad \textbf{(5.2)}$$

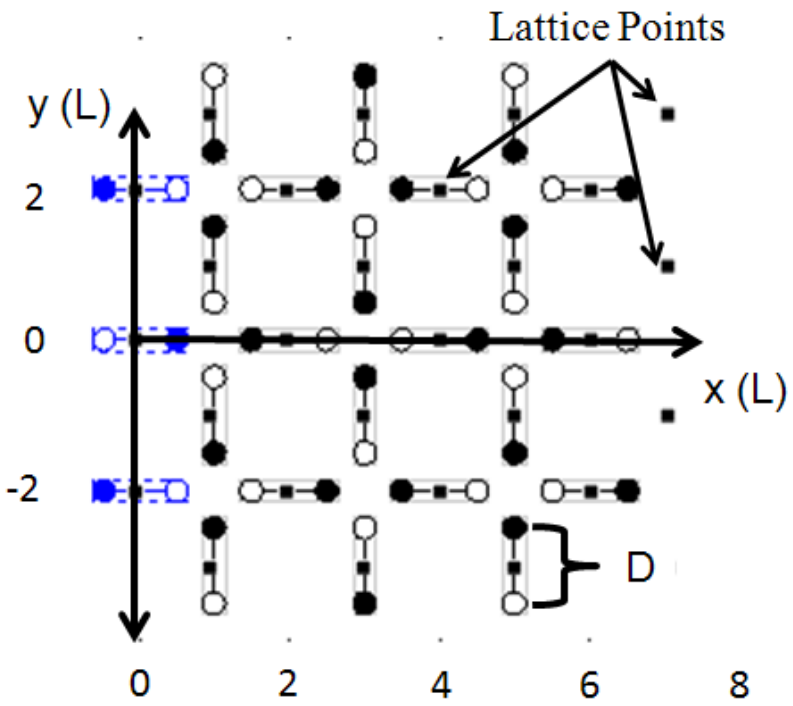


Figure 5-2. Geometrical layout convention used for LINA designs

5.1.2 LINA Thermal reliability improvements

Although there is an increase in LINA design and/or layout complexity as opposed to traditional QCA, this is offset by the significant increase in reliabilities of LINA. An example of this reliability increase can be seen in the coherence vector reliability results for two wires shown in Figure 5-3. As can be seen from the figure, a 300nm wire created from cells with an inter-dot distance (D) equal to 10nm and an intercellular lattice space (L) distance also equal to 10nm was simulated. 10nm was chosen due to the fact that many nanoparticles arrays which are currently able to be fabricated have lattice spacings and cell sizes that are equal to or greater than 10nm. The simulations of these wires were ran assuming a relative permittivity equal to 1, and

tunneling energies, which are driven by the QCA clock, oscillating between 9.8e-20 J and 3.8e-23J (which are typical QCA simulation values). The results show a PCLO of .86 for the wire of the traditional QCA design at the room temperature of 300K. PCLO for the LINA designs are much improved at this temperature with 1-wide LINA PCLO of .97, 3-wide PCLO of four 9's (.9999), and 5-wide PCLO of six 9's. The PCLO value is the expected reliability rate of the component being tested. In this case, a six 9's reliability would mean that with a clock rate of 1 GHz, the expected error rate would be 1000 errors per second down this length of wire, well exceeding error rates for current technologies but also a dramatic improvement over traditional QCA designs. Additional methods of fault tolerance, such as in-time redundancy or error correction methods, would have to be used in this case, but it opens the possibility of room-temperature QCA circuitry at this previously unavailable size scale.

The predicted increase in room-temperature reliability is consistent for different L and D values (as well as for other simulation methods such as those which use Boltzmann distributions). PCLO for room temperature operation of the L=D=20nm 200nm long wire demonstrates this fact. Traditional QCA designs are nearly completely random (PCLO ~.5) at this temperature. The 1-wide LINA PCLO is also nearly random here; however, 3-wide LINA PCLO is .96 and 5-wide PCLO is .98. The dramatic improvement in thermal reliability for such a large scale QCA cell opens up the possibility to even semiconductor

realizations, although the other fault tolerant methods would certainly be required here also.

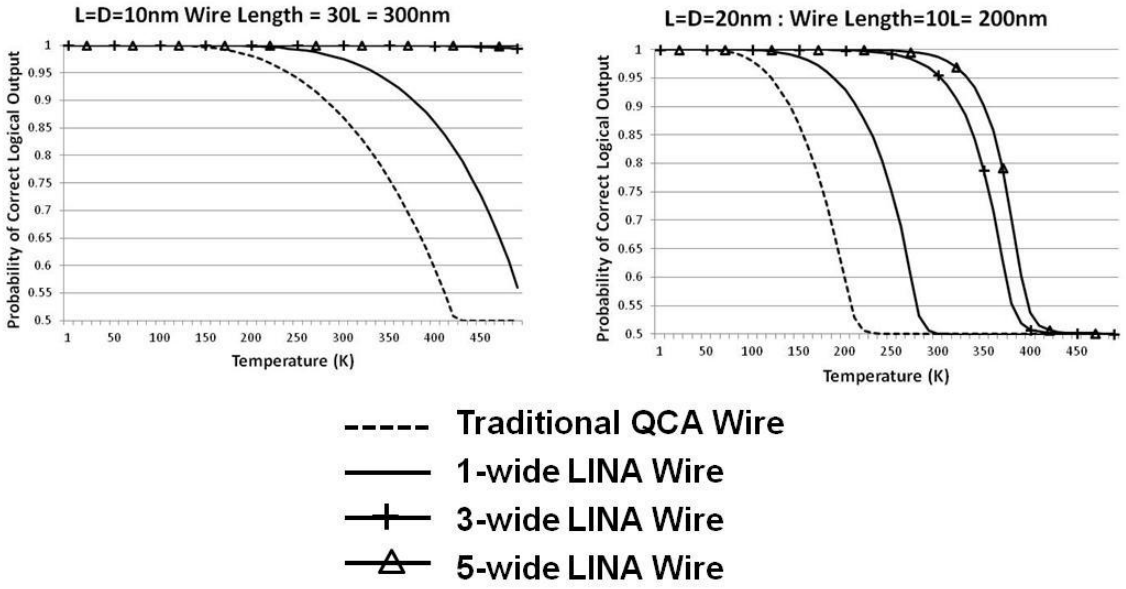


Figure 5-3. Probability of Correct Logical Output (PCLO) for traditional and LINA wires utilizing different cell sizes and spacings (The simulations were performed with relative permittivity of 1, high clock level of 9.8e-20 J, and low clock level of 3.8e-23J.)

5.1.3 LINA robustness to fabrication defect

In addition to improving reliability in the presence of logical errors caused by thermal noise, LINA is also well suited to provide robust operation in the presence of fabrication defect such as cell addition, deletion, and/or trapped stray charge. This is critical due to the probabilistic processes which usually govern any self-assembly process and the small scales in which the circuits would be patterned. Figure 5-4 shows an example of this type of tolerance. Part C in the figure shows a fully functional section of 3-wide LINA wire complete with many randomly placed cell additions and deletions. The results shown here are common to the LINA paradigm and indicate that errors that

would cause permanent faults in other QCA circuitry are able to be tolerated for LINA. This effect is increased further as the width of the wires is made larger. Therefore, wire width could be adjusted in the design phase to account for the amount of expected layout errors.

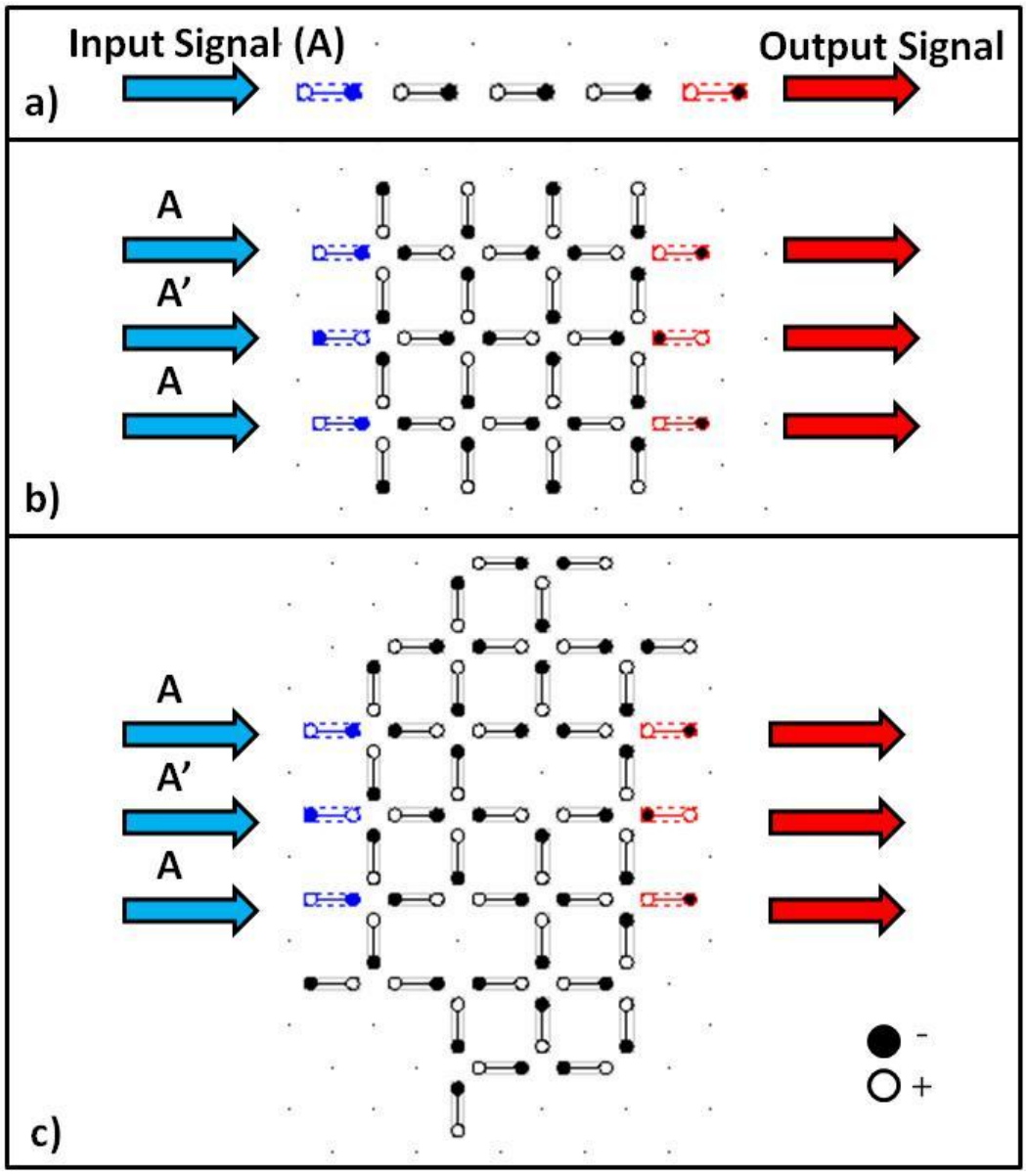


Figure 5-4. Figure 1a) 2-D 2-dot QCA wire which, like traditional QCA, are not robust in the presence of fabrication errors b) ideal 3-signal LINA wire c) Fully functional LINA wire with random cell additions and deletions

5.2 LINA Logic Structures and Circuitry

5.2.1 LINA majority gates and blocks

Traditional QCA logic design is centered on the three input majority voter gate which is typically made up of a single QCA cell. This gate along with the ability to invert a signal gives the traditional QCA design logical completeness. The LINA designs are also based on the three input majority gate; however, the implementation of this logic gate requires a fully populated n x n area of the lattice map to perform computations (where the input and output wires are n-wide). The LINA majority gate performs the majority function in a way similar to the majority gates developed for the 2-D 2-dot QCA except that the input which comes into the gate 90 degrees clockwise from the output is always inverted. This is shown in Figure 5-5, where the bottom “C” input is being inverted in the majority gate. In the figure the cells which are circled in red correspond to the values of the inputs and outputs of the gate. In general, the closest cell in the center of the LINA wire to the majority gate for each wire is chosen, and the output is taken from the center cell of the wire one block spacing from the gate on the output wire.

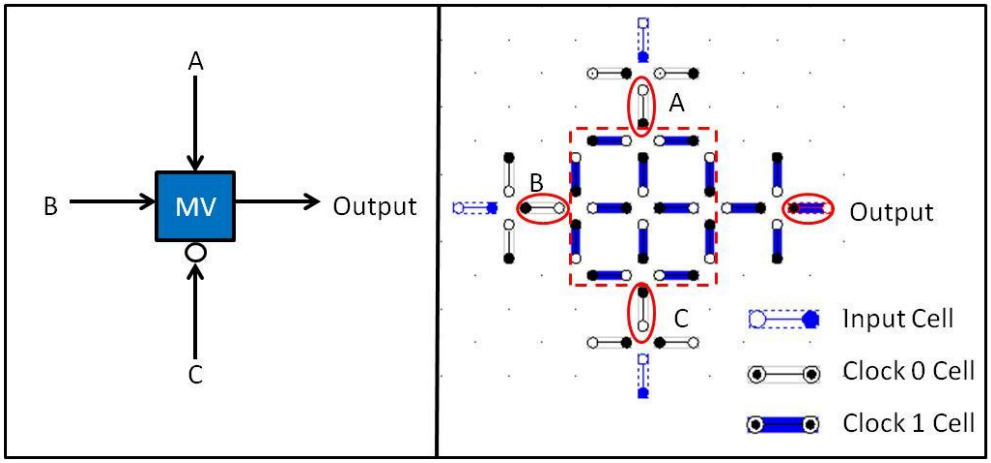


Figure 5-5. Majority Voter gate in 1-wide LINA

Due to the regular structure of the LINA lattice map and other clocking considerations, it is convenient and in many ways necessary to group LINA cells together when laying out circuitry. The proposed 1-wide LINA majority gate is an example of this with the gate defined as a square block; however, the wires should also be grouped this way. This provides the advantage of allowing a simplified layout and design process as groups, or blocks, of cells are used. Blocks are defined as squares of cells that have a length equal to the LINA design width. It should be pointed out that the width of the blocks and therefore the LINA design should be directly related to the layout technologies for the clocking structures as well as the cells themselves; therefore, intra-block cells should utilize the same clock phase. It also should be noticed that the same block layout can be used for circuitry regardless of wire width. Figure 5-6 and Figure 5-7 show examples of 3-wide and 5-wide LINA majority gates where this can be seen.

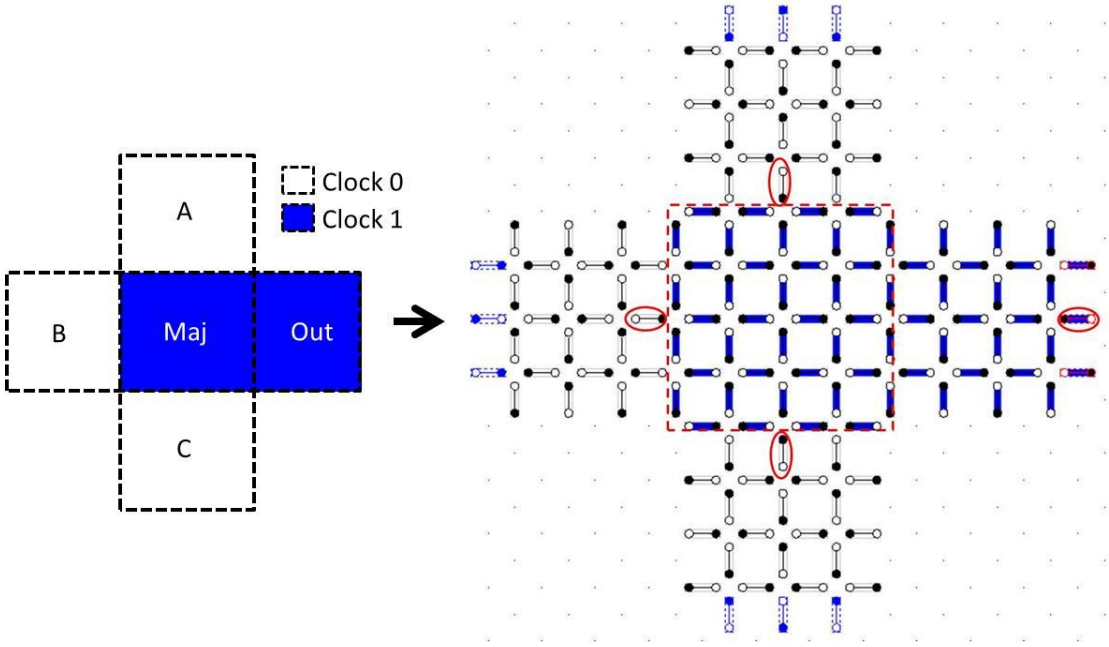


Figure 5-6. 3-wide LINA majority gate with associated LINA block representation

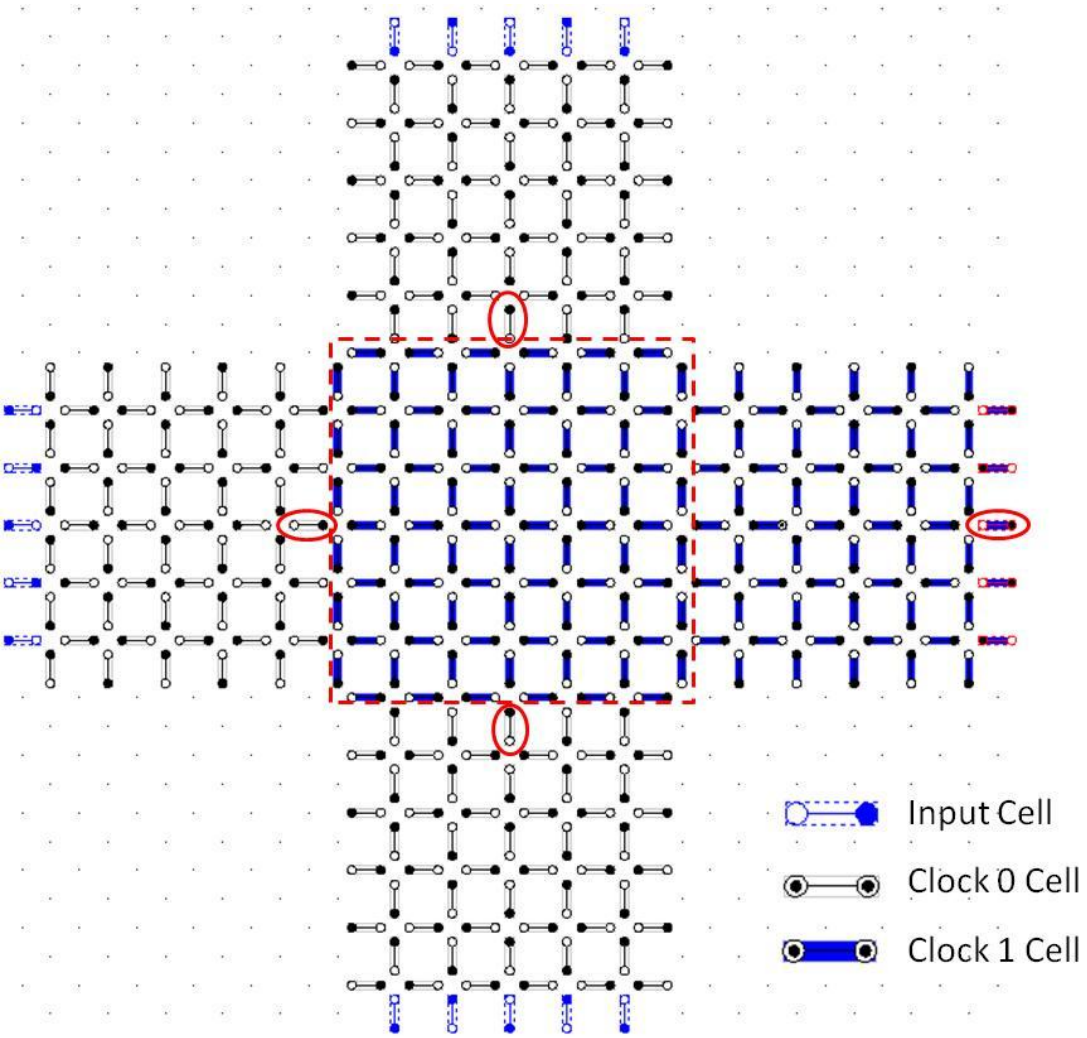


Figure 5-7. 5-wide LINA majority gate

The same majority gate/block structure shown can also be used for different functionality depending on how the circuit is laid out and/or how the clocking signals are distributed. For instance, a single input wire can be fanned out using this structure or be used to turn a corner, if the other wires are down the signal path from the input. The following section shows yet another use of the structure for a planer wire crossing.

5.2.2 LINA planer wire crossing

In LINA, a planer wire crossing can be made by using the same block structure as the majority gate. However, due to the structure of LINA, it will not be available without a modification to the traditional QCA clocking scheme. The required clock signal which will drive the crossing block does not have hold or null phases. Instead it has two switch and relax phases per normal clock period. This allows a signal to pass across the block in each switching phase. However, only one wire should be allowed to affect the block during each switching phase, so the two wires which cross at the block should be ½ a clock period out of phase with each other for the block to function properly. This will assure that only one signal crosses the block at any given time. Simulations verify correct functioning of this wire crossing block which is shown in Figure 5-8. Additionally shown in Figure 5-8 is the triangle waveform of the clocking signal used by the crossing block (as opposed to the clipped sinusoid for the other clock signals) to give it two switch/relax phases per normal clock period.

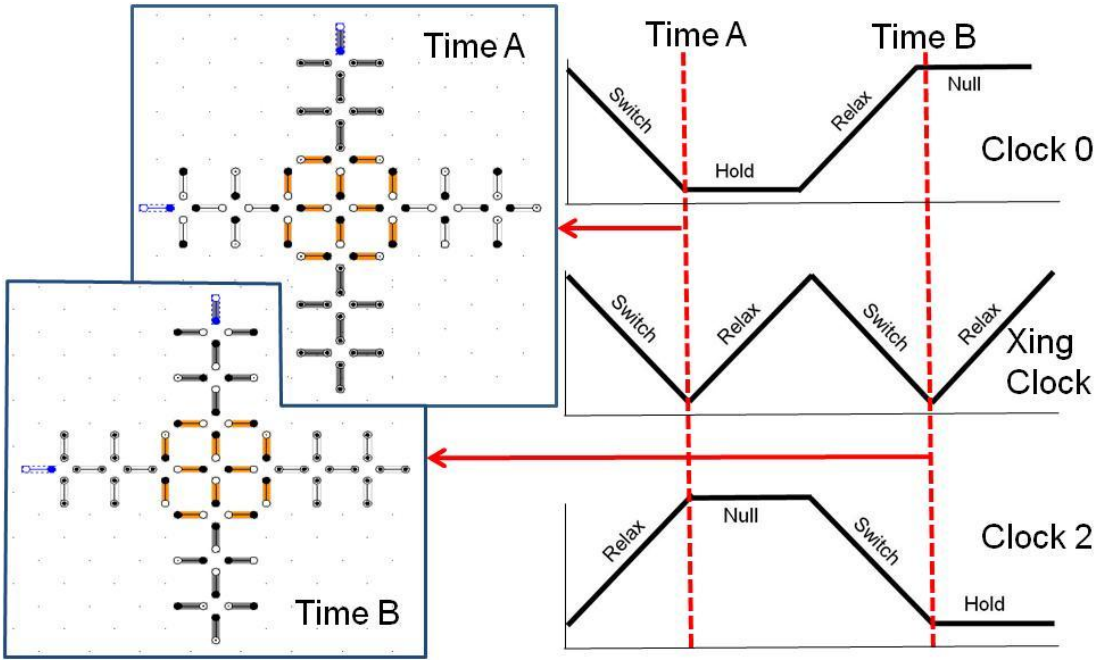


Figure 5-8. Planer wire crossing using a 1-wide LINA crossing block. Other width of LINA crossing will use the same block scheme. At time A, the first signal passes through the block from left to right. At time B, the second signal passes through the block from top to bottom. QCA circuit shows actual simulation results.

5.2.3 LINA Inverter

The last logic block that is required for logic completeness for the LINA paradigm is an inverter, which in LINA can come in many forms. Due to the inherent inverter chain nature of the LINA design, the simplest inverter can be achieved by carefully choosing the correct length of wire. However, this method of inverting a signal will be intolerant to even the slightest patterning errors and thus may not be the optimal choice for this function. Also, the method of controlling the length of the wire does not scale well to large circuitry where wires must meet at precise locations to perform logic with some of the inputs being inverted and some not. Instead a dedicated LINA logic block to invert

signals is preferred. The inverter block is created by removing a column in an otherwise normal LINA wire. This method is applicable to any width LINA technology and is shown in 1 and 3 - wide implementations in Figure 5-9.

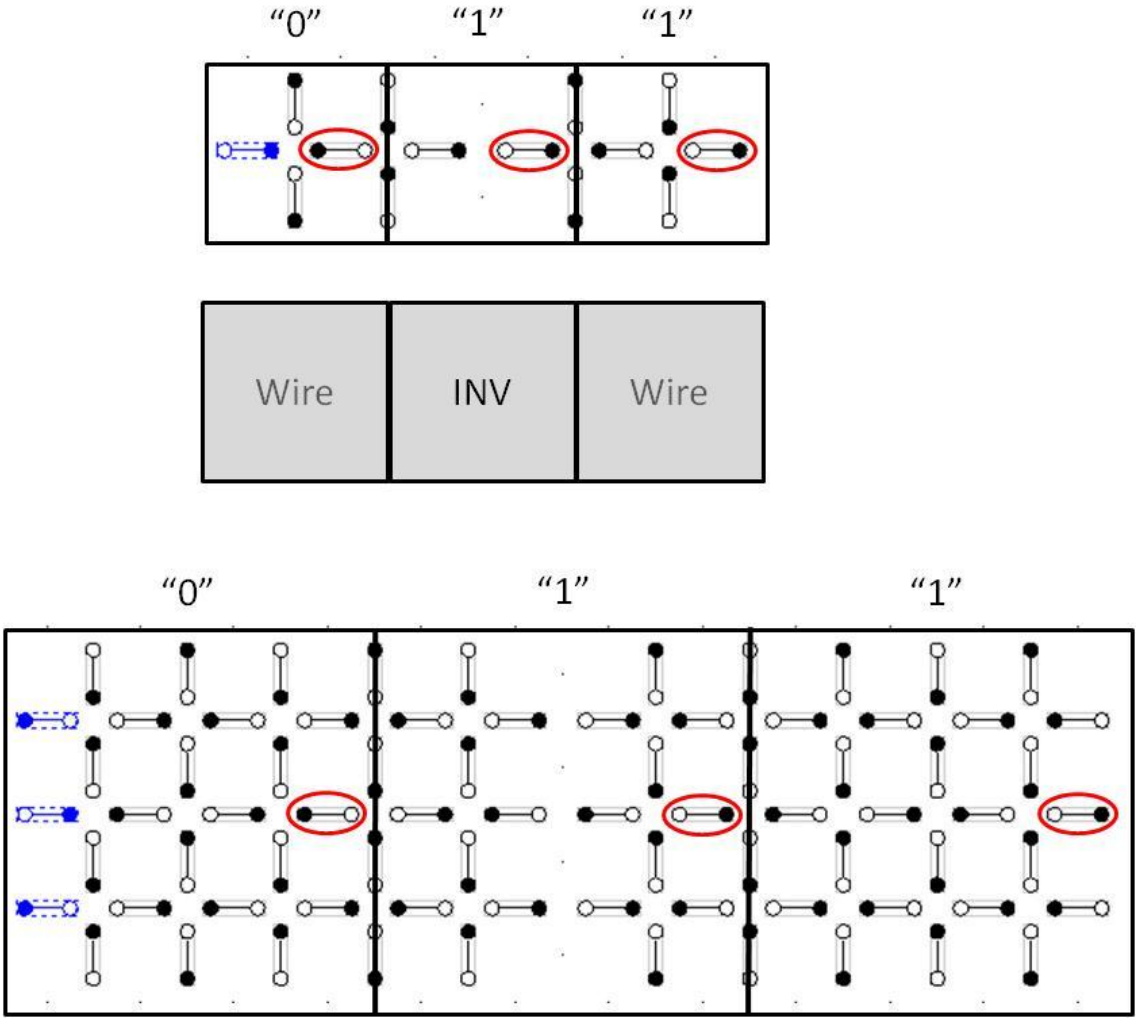


Figure 5-9. LINA inverter implemented with 1-wide LINA, block representation, and 3-wide LINA. Note output reference cell circled in red.

5.3 Chapter Summary

This chapter presents the logically complete functionality of LINA and the potential advantages that it provides in reliability and fabrication practicality going forward. However, power and speed considerations for these devices

must present an improvement over end of the line CMOS to justify the significant investment required to develop any replacement technology. Therefore, simulations results will be used in the next section to analyze properties of these LINA designs for high temperature reliability, power dissipation densities and switching speeds and compare these to end of the line CMOS.

Chapter 6

LINA Analysis and Design Study

It has already been shown, in the previous chapter, how LINA designs can improve reliability by adding width to gates and wires. However, it is common to nanoelectronics proposals (and QCA specifically) that an increase in reliability is usually accompanied by an increase in power requirements. Certainly, adding additional QCA to circuitry, in the form of LINA wires and gates will create additional power which must be dissipated to the environment. However, LINA designs actually generate less heat for fixed reliabilities as opposed to reducing cell dimensions and spacing for certain conditions. To prove this statement, formulas derived in [60] (and presented in Section 4.4) for power dissipation are utilized along with coherence vector simulation methods.

6.1 LINA design trade space: power, speed, geometry, and reliability

Concurrent evaluation of power, speed, and reliability is complicated by their interrelated nature and the fact that QCA cells both process and communicate information. This provides a rather difficult task in developing suitable metrics for quantifying the results of this evaluation. However, by borrowing concepts used to categorize CMOS technology levels, a reasonable metric called the "effective QCA pitch" was formulated. This value is based on the distance between basic QCA and LINA blocks (whether they be used for majority gates, fan-out, or planer crossing), as shown in Figure 6-1, and provides a measure of

the circuit density available for particular power, speed, and reliability constraints.

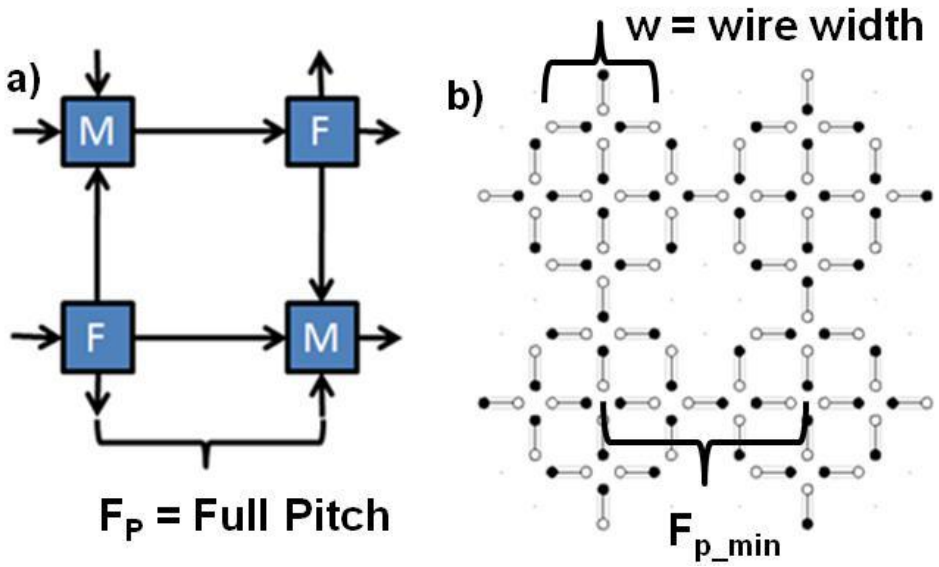


Figure 6-1. a) Small array of blocks (in this case Majority (M) and Fan-out (F) gates) with associated full pitch (F_p) b) Example of smallest possible 1-wide LINA full pitch

The process to calculate the half-pitch value begins by assuming a reasonable upper limit of power dissipation of 100W/cm^2, and that the average per cell power dissipation is evenly distributed throughout the cell. This allows for calculations of the maximum density of cells based on the average power per cell that must be dissipated at a given clock frequency. The constants in the calculation are: the density of cells for a particular LINA width wires and gates and the minimum distance which two blocks can be placed together. For examples, Figure 6-2a shows a minimum pitch of 10 times the distance L for 3-wide LINA. In general, the minimum “full” pitch can be found with (6.1).

$$F_{p_{min}} = (2 * n + 4)L \qquad for\ LINA$$
$$F_{p_{min}} = 4L \qquad for\ Traditional\ QCA \tag{6.1}$$

where n is the width of the LINA wire and L is the cell to cell spacing as defined in Section 4.5.

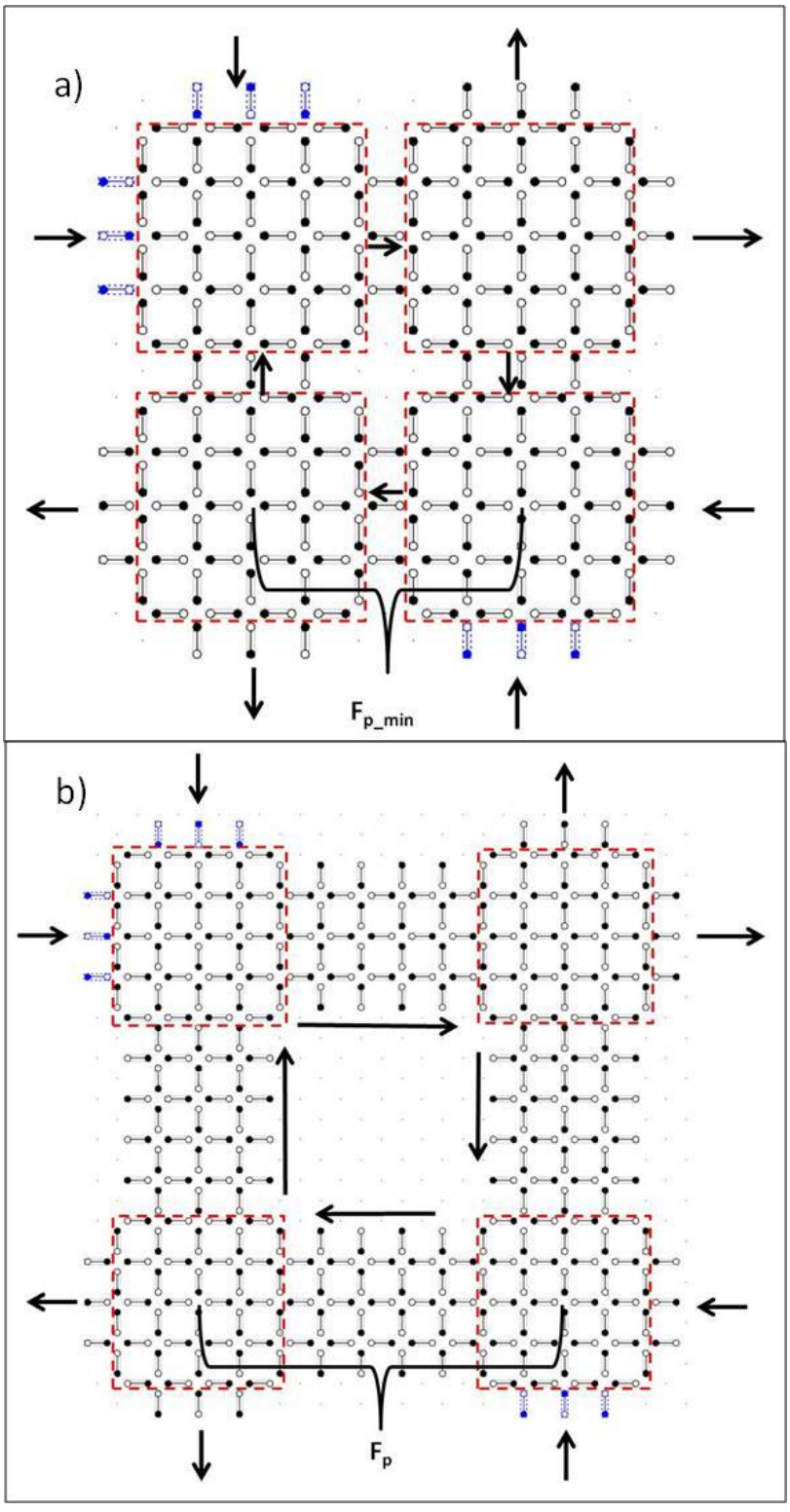


Figure 6-2. Basic array circuit for calculation of pitch a) minimum pitch for a 3-wide LINA b) larger pitch allowing for less circuit density

The minimum pitch occurs with a single row or column of QCA cells separating the block gates. In general, these wire lengths are an integer value of cells because of the cellular nature of the QCA paradigm. The value of the full pitch is therefore generalized to (6.2).

$$F_p = (2 * n + 2 * s + 2)L \tag{6.2}$$

where s is the integer value cells in the length of each wire (with s equal to 1 for the minimum case. Therefore, the full pitch becomes an integer value of the cell to cell lattice spacing. Also, the length and the size of the block gates allows for calculation of number of cells within a square area of the array with sides equal to the length of the full pitch. This number of cells is also dependant on the width LINA used, due to the fact that the cells of each wire must stay together and is equal to (6.3).

$$N_c = \frac{\#_{cells}}{Area_{pitch}} = 2n^2 + 4n + 2 + s(4n + 2) \qquad for\ LINA$$

$$N_c = \frac{\#_{cells}}{Area_{pitch}} = 2 + 4s \qquad for\ Tradtional\ QCA \tag{6.3}$$

It is clear from these equations that the number of cells required, N_p, by traditional QCA can be significantly less than that required by LINA for a fixed pitch value, F_p. This is offset by the need to utilize smaller cells, and therefore larger power dissipation per cell, P_c, to obtain the reliabilities that the LINA arrangements provide. Therefore, for a constant reliability, the LINA designs dissipate a smaller amount of P_c and require larger N_c when compared with traditional QCA. Whether the P_c element of this trade or the N_c element is the largest contributor to overall circuit size is determined by the geometrical QCA

properties (D = intracellular dot spacing and L = cell-to-cell spacing) as well as the frequency of the clock compared to the relaxation time for cell switching (therefore the deviation from the adiabatic ideal).

Therefore the minimum F_p based on per cell power dissipation requirements and number of cells is determined by (6.4) with the predefined 100W/cm^2 maximum.

$$N_c * P_c/{F_p}^2 = 100\ W/cm^2 \quad \textbf{(6.4)}$$

Results of these calculations can be seen in Figure 6-3 for various L and D values and various QCA types. In part a) of the figure, the PCLO was calculated for a length of wire of $Length = (20 * L)$ for traditional, 1-wide LINA, 3-wide LINA, and 5-wide LINA designs for various cell geometries. As is expected, the LINA wires increase PCLO as the wire width increases. In part b) of the figure, the minimum $F_p$value was calculated based on these room-temperature calculations, a 1THz clock frequency, and a required PCLO reliability of .9999. The results show that while the traditional QCA requires smaller cell geometries and requires fewer cells per length of wire, LINA designs actually have a smaller effective pitch based on power requirements. Furthermore, the LINA designs are able to provide these attributes at larger cell geometries which increases the opportunity for fabrication, as has been discussed.

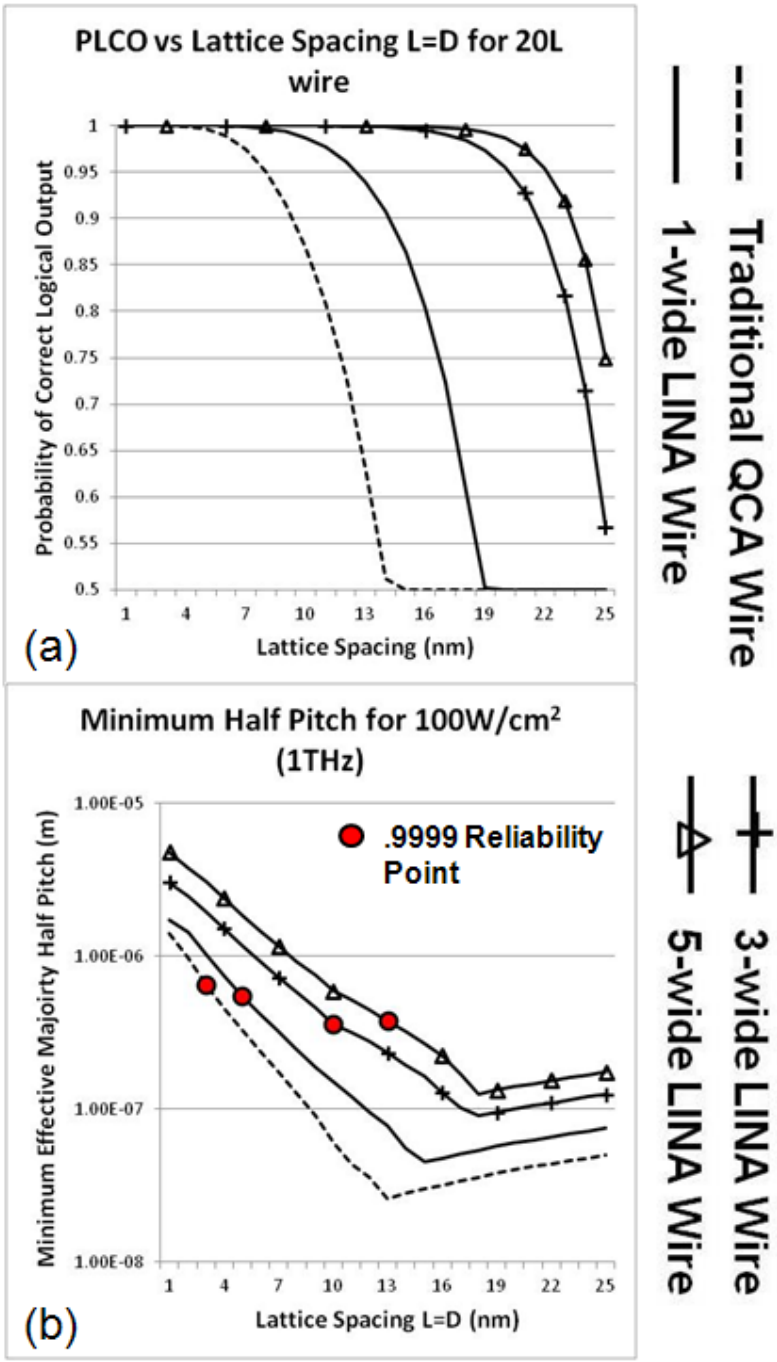


Figure 6-3. (a) Probability of correct logical output (PCLO) for room temperature operation with increasing lattice spacing from 1nm to 25nm for traditional and 1,3,5-wide LINA wire designs. Wire length is 20L. (b) Minimum "effective majority" half pitch for 4 traditional and LINA wire circuit design along with the 4 9's reliability point at 1THz. Note the minimum half pitch is seen with the 3-wide LINA design at this reliability. The simulations feeding this data was ran with relative permittivity of 1, high clock level of 9.8e-20 J, and low clock level of 3.8e-23J.

Table 1 shows calculated values for full pitch for various reliabilities based on this process. The table shows clear advantages for the LINA designs at high frequencies and with high reliability requirements. The data also shows that the traditional QCA designs are advantageous in circuits where the desired frequency or reliabilities are low. (Further data reiterating these claims can be found in [111, 112])

It is interesting to see in Table 1, that the 1nm cell spacing does not provide a minimum pitch for any of the entries. This is due in part to the number of cells and thus switching events that must be accounted for using such relatively small cells and the large power per cell values which scales inversely with cell spacing due to higher kink energies. It is also interesting to note that simulations involving QCA designs do not yield a particular small circuit area if 1 THz switching with high reliabilities is desired; instead a tradeoff between circuit area, clock frequency, and reliability will have to be made. These types of trades are common for IC designers even today and as technologies improve these trades are sure to grow more favorable.

Table 1 - Minimum full pitch and wire design parameters for various clock speeds, and reliabilities

Clock Speed	Reliability > 6 9's	Reliability > 5 9's	Reliability > 4 9's
1THz	F_p = 1180nm L = 12nm 5-wide LINA	F_p = 1034nm L=13nm 5-wide LINA	F_p = 720nm L=10nm 3-wide LINA
500GHz	F_p = 360nm L = 10nm 5-wide LINA	F_p = 308nm L = 11nm 5-wide LINA	F_p = 182nm L=13nm 5-wide LINA
100 GHz	F_p = 30nm L = 3nm 1-wide LINA	F_p = 24nm L = 4nm 1-wide LINA	F_p = 18nm L=3nm Traditional QCA

6.2 LINA design examples (full adder circuit)

As an example of LINA designs and how the results found in the previous sections may be used, the full adder circuit, based on the simplified sum and carry outputs found in [45] and shown in Figure 6-4, will be constructed. The design of this example will require greater than 5 9's reliability at the circuit outputs, a 100GHz clock speed, and one full clock cycle for operation. Additionally, the circuit uses a simple design rule which dictates a single block spacing between adjacent wires. An initial design presupposing the most efficient implementation technology is available will be presented. Then another design with many practical limitations will be given.

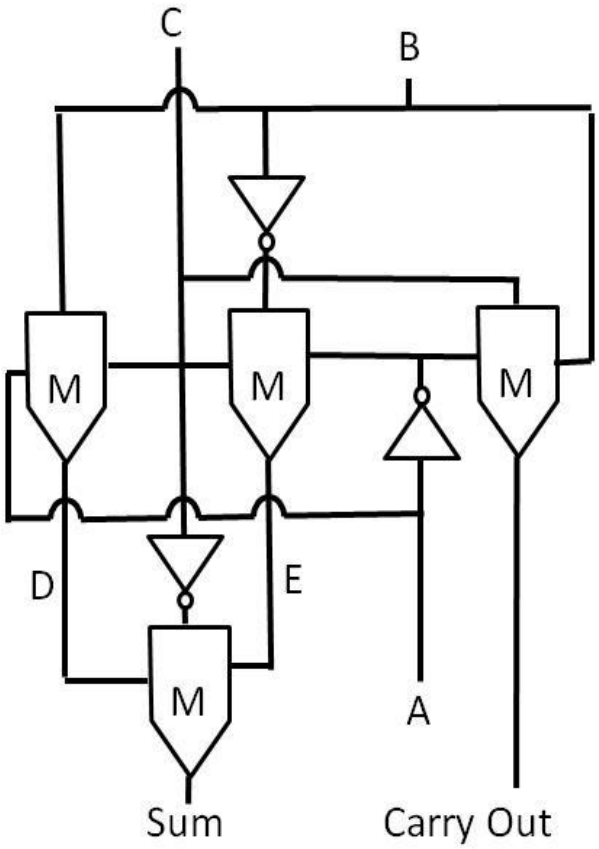


Figure 6-4. Logical Schematic of the full adder used in the design examples of Section 6.2

6.2.1 Greatest space/power efficiency approach

Table 1 shows that, for the required speed and reliability, 1-wide LINA provides the greatest space/power efficiency using a 4nm spaced LINA circuit. So, it would be ideal to use these circuit geometries if the implementation technologies required are available. These technologies include:

- A 4nm bipolar molecule which self assembles at the 4nm lattice spacing as is seen for the lattice map

- Patterning technologies which is able to pattern both the LINA circuit and the underlying clocking circuitry at a resolution equal to half a single block width (which in this case of a 1-wide LINA design with L=4nm and D=4nm, is 16nm).
- Input/Output mechanisms which are able to individually force and read QCA states at the 4nm range.

Assuming, for the time being, that these technologies are all available the first design of the full adder will use the 4nm 1-wide geometry.

As has been briefly discussed, for complex circuitry, such as seen for this circuit, it is important to utilize a blocks design methodology. The first step in constructing the blocks representation of the adder will be to determine the number of blocks which will be required between each logical element. The circuit design rule which dictates that at least one block be present between each wire is the first consideration which must be used. Additionally, Table 1 gives a minimum full pitch of 24nm to remain under the allotted power requirements. For this design we are required to use the maximum of these two requirements to be certain that both are full filled. In the 1-wide LINA design the width of a block is equal to the width of two full cells, therefore, the full pitch for a single block spacing according to (6.2), is 8L. So for this case, 8L is equal to 32nm, which is less than the 24nm power dissipation requirement and thus the design rule will set the minimum block spacing. With the minimum block spacing set, the blocks design for the adder now turns attention to the full clock cycle requirement. This requirement dictates that, the inputs and outputs

of the adder be tied to the same clock. Furthermore, all wire crossings must occur ½ a clock cycle out of phase (or two clock zones out of phase). And lastly, it is beneficial to the design to have the inputs to all majority gates be on the previous clock from the gate itself. This allows for more robust operation due to rejection of the inputs as previously discussed. These considerations produce the blocks design seen in Figure 6-5. In the figure, the blocks are labeled with either the input (A, B, or C) or the block function (M for majority, X for crossing, or I for inversion). This design has dimension of 12 blocks x 16 blocks or for this technology 192nm x 256nm (due to 4*L per block for 1-wide LINA and L = 4nm for this design).

A couple of observations which must be pointed out with this design, first in order to reduce the total number of wire crossing blocks, input A comes in from the bottom of the circuit while inputs B and C come in from the top. It is interesting to note the directional dependence of LINA blocks here, which, because of the logic convention used, creates an inversion of input A when fed into each of the majority gates. Although, the inverted state of input A is required for the leftmost majority gate, the others require a non-inverted input A. Therefore, an inverter is placed in line upstream from these gate inputs. In general terms, the direction from which a signal enters the circuit is important as is the direction from which an output leaves the circuit, although, in a global sense, the natural inversion as wire corners are turned in a specific direction cancels out all of the inversions internal to the circuitry (even for the inversion seen on the input of the majority gate!) This discovery greatly simplifies circuit

construction and LINA blocks design by allowing the design to progress more intuitively.

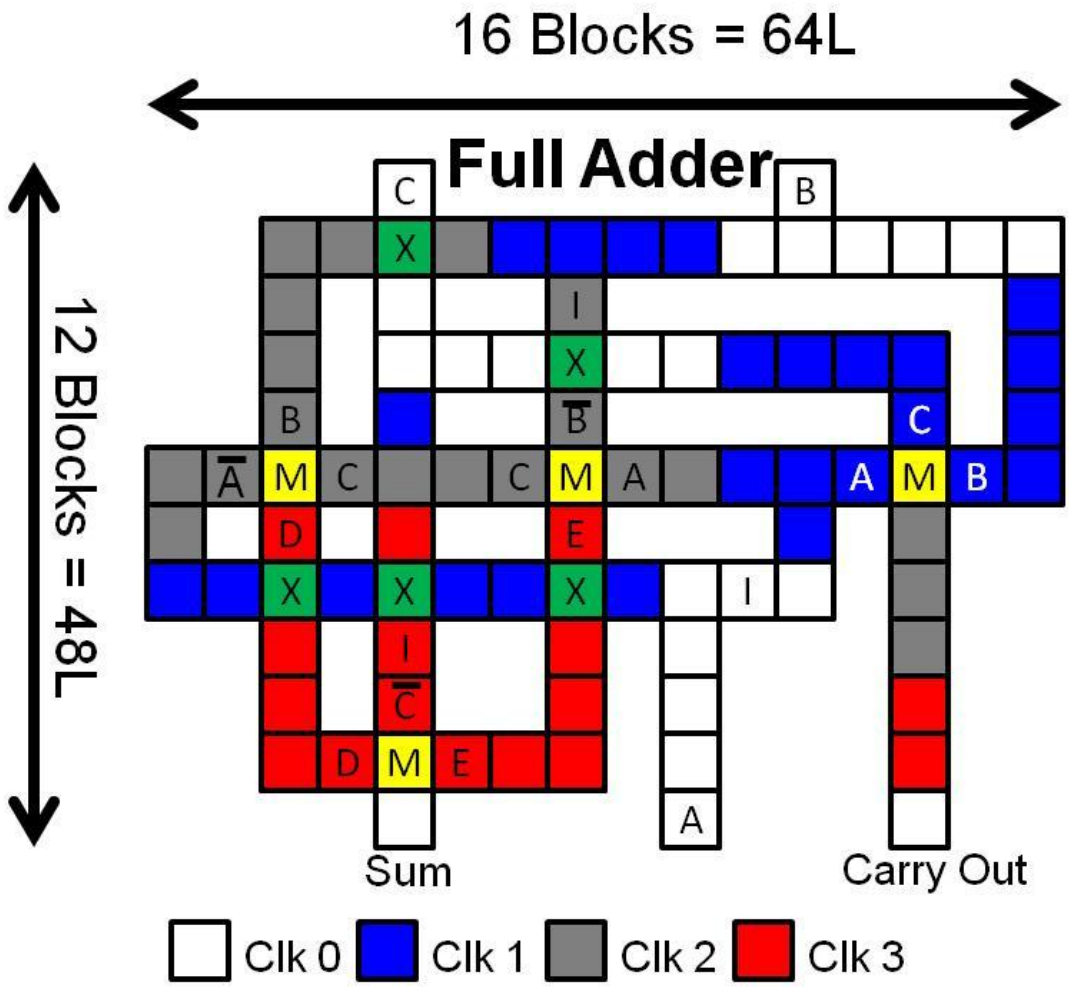


Figure 6-5. Blocks design for the first LINA full adder example (1-wide 4nm)

Once the blocks design has been completed, the implementation of the LINA cells and clocking circuitry can proceed naturally.

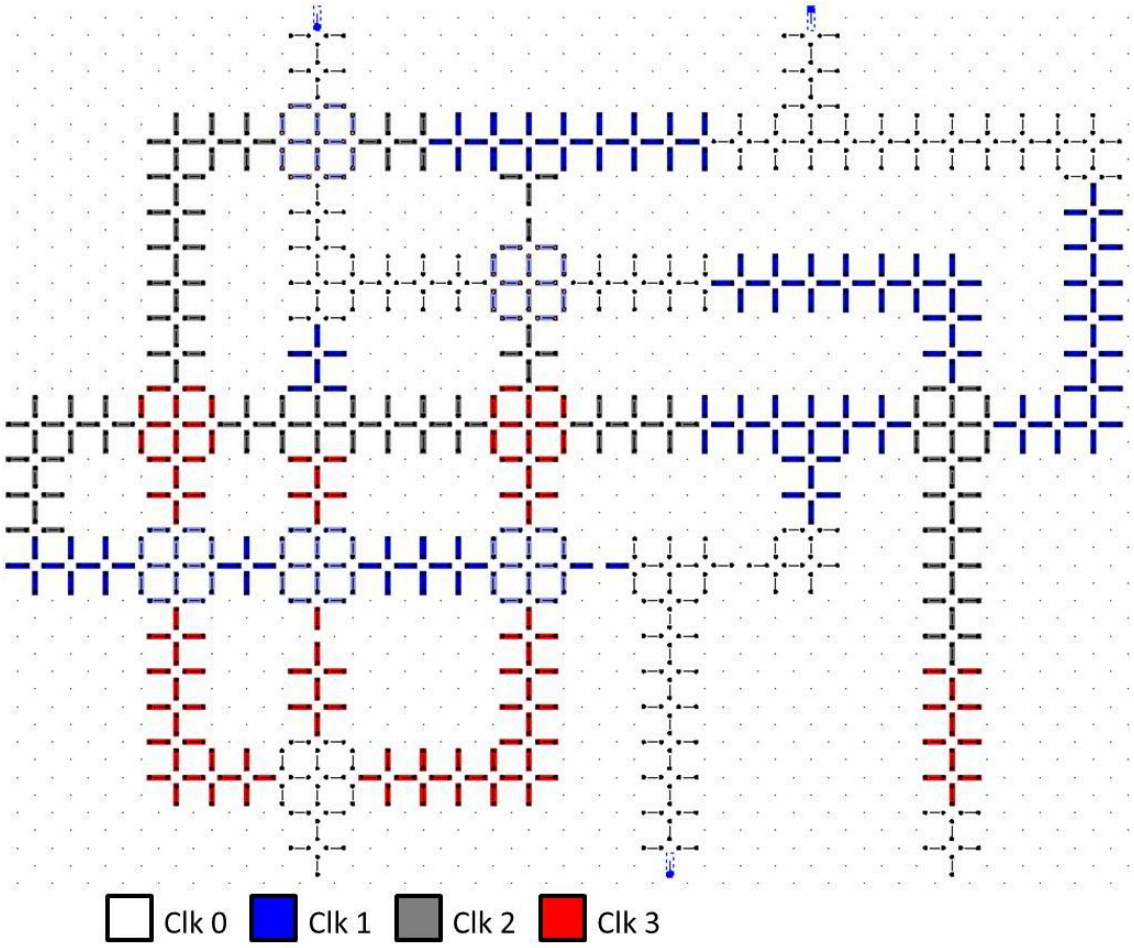


Figure 6-6. 1-wide LINA layout of full adder circuit

Figure 6-6 shows the 1-wide 4nm LINA layout for the circuitry corresponding to the blocks design. As seen in the LINA layout and blocks design, sum and carry-out outputs are taken from the bottom of the circuit and, as can be seen by the simulation results of Figure 6-7a, are valid one complete clock cycle after the corresponding inputs are latched in. Another important feature that should be discussed further is the use of five LINA coplanar wire crossing blocks and both LINA wire crossing clock patterns. As has been discussed, the coplanar crossings are able to pass signals which are half a clock out of phase with each

other (Clocks 0 and 2 or clocks 1 and 3). The clock signals which allow this are shown along with the traces for all of the other clock signals in Figure 6-7b.

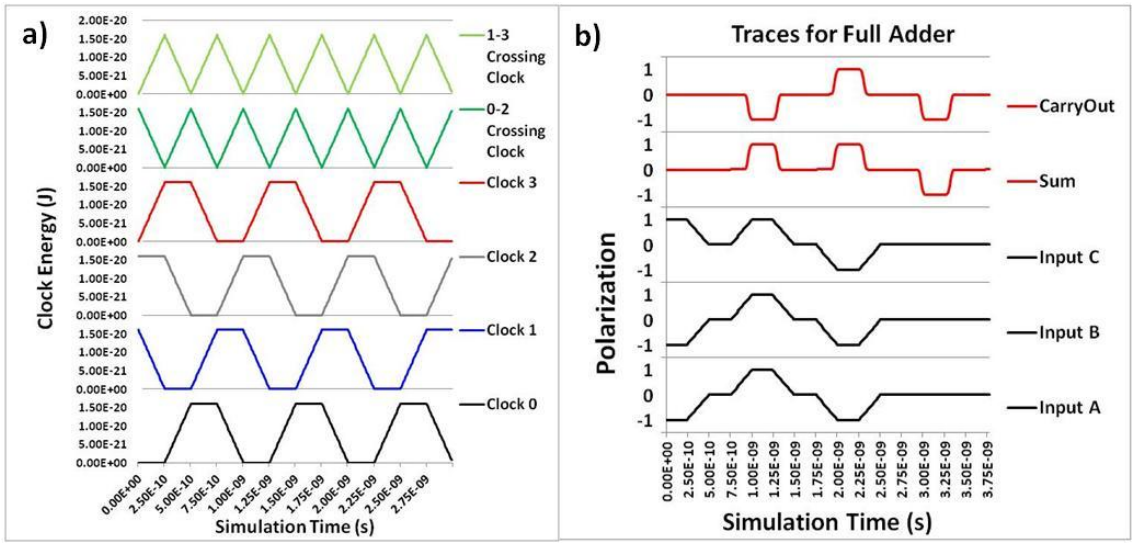


Figure 6-7. a) Clock traces used for the full adder b)Traces for the inputs and outputs of full adder circuit

As has been mentioned, the blocks design for this full-adder can be implemented with any width LINA wire. However, this blocks design will not be allowed if other factors such as power requirements create block wire spacings which are not supported by this design. In general, other practical issues must also be accounted for in the design of LINA circuitry. These issues along with the layout and simulation of a circuit which is based on them is seen in the next section.

6.2.2 Full adder design using practical implementation issues

In the previous section, implementation technologies were assumed to be ideal. This allowed the full adder design to be solely influenced by the design minimum specifications and efficiencies based on power density and circuit

area. For this design, other limitations will be considered which may arise in the construction of actual LINA circuitry.

Firstly, it will be assumed that three different materials have been found which fit the LINA requirements of bipolar interaction, and the self-assembly pattern of the lattice map. These materials can produce LINA cells with the following spacings:

- Material 1 - L_1 = 10nm D_1 = 10nm
- Material 2 - L_2 = 13nm D_2 = 8nm
- Material 3 - L_3 = 8nm L_3 = 8nm

Additionally, high density large scale lithographical techniques are assumed to allow for patterning of clock and LINA circuitry with a resolution which is no less than 35nm. (Certainly smaller resolutions should be possible but just for this example the large resolution is chosen.)

With the larger cells and cell spacings, a larger width LINA wire will be required to provide the 5 9's reliability requirement for the circuitry. Simulation results show that 3-wide LINA wire would provide this reliability for material 1, greater than 7-wide LINA would be required for Material 2, and a 3-wide LINA would be required for material 3. All other things being equal, choosing the smallest width LINA wire with the smallest spacings possible for the required reliability seems ideal. However, it has already been shown how power dissipation requirements have an effect on this choice. Additionally, the resolution with which the circuit can be patterned affects this choice. For instance, the minimum resolution of the patterning technologies is 35nm and the minimum width of LINA block must

be greater than or equal to 2 times this width. For material 3, the width of a 3-wide LINA block is 8 * L = 64nm. Since this number is less than two times the minimum patterning resolution, the block width (and thus the LINA width) must be expanded. Also since the width of LINA must be an odd integer number the LINA design for material 3 must be a 5-wide design. This 5-wide design then creates blocks with a width equal to 12 * L = 96nm. In contrast, a 3-wide LINA block for material 1 would be 8 * L = 80nm in width and also contains less cells than a 5-wide LINA design using material 3. In this case, it is better to use the slightly larger cell and lattice spacing material, because of limitations in the patterning technologies.

Since these materials provide blocks which are much larger than the minimum blocks and full pitch based on power dissipation limitations, the design rule of one block per spacing will be the dominant property setting the wire and gate spacings. Since this is the same case as was shown in the previous section, the same blocks design shown in Figure 6-5 can be used. This demonstrates how LINA designs can scale with different technologies. The layout for the circuit is shown in Figure 6-8. Although, due to the relative size of the cells the clocks are difficult to see they are the same as in the blocks diagram.

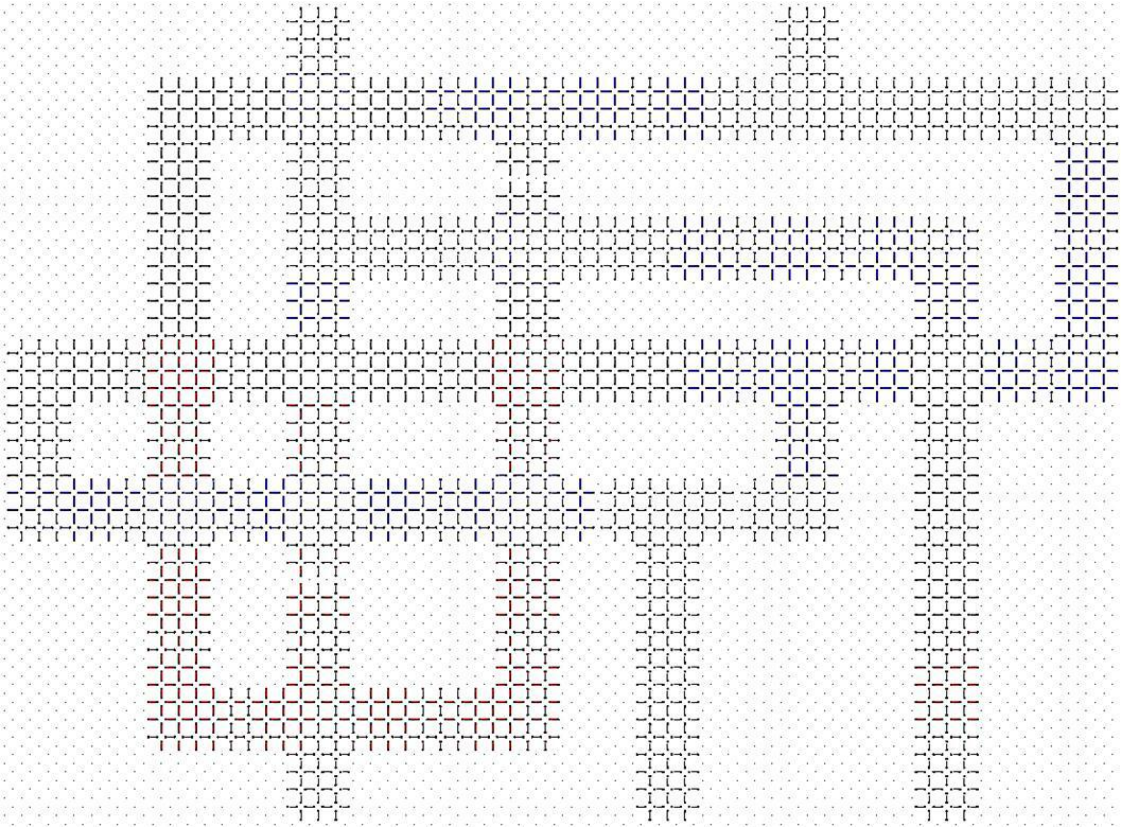


Figure 6-8. 3-wide LINA layout for Section 6.2.2

The apparent complexity of the clocking circuitry may be an issue when developing circuitry. At this time, only primitive clocking mechanisms consisting of buried clocking wires have been proposed [62]. Therefore, the design of the underlying clocking structure must also be of utmost importance to any LINA design. However, in order to de-mystify the process, a clocking layout consisting of 6 layers (one for each clocking zone, including the crossing clocks) has been developed for this circuit. The layout conforms to the minimum patterning resolution of 35nm set as a design limitation at the beginning of this section. The layout of the clocking layers is shown in Figure 6-9. In the figure, vias carry the clocking signal from layer to layer in much the

same way they would in modern electronics. In fact, the technology to produce the clocking circuitry for this full adder currently exists.

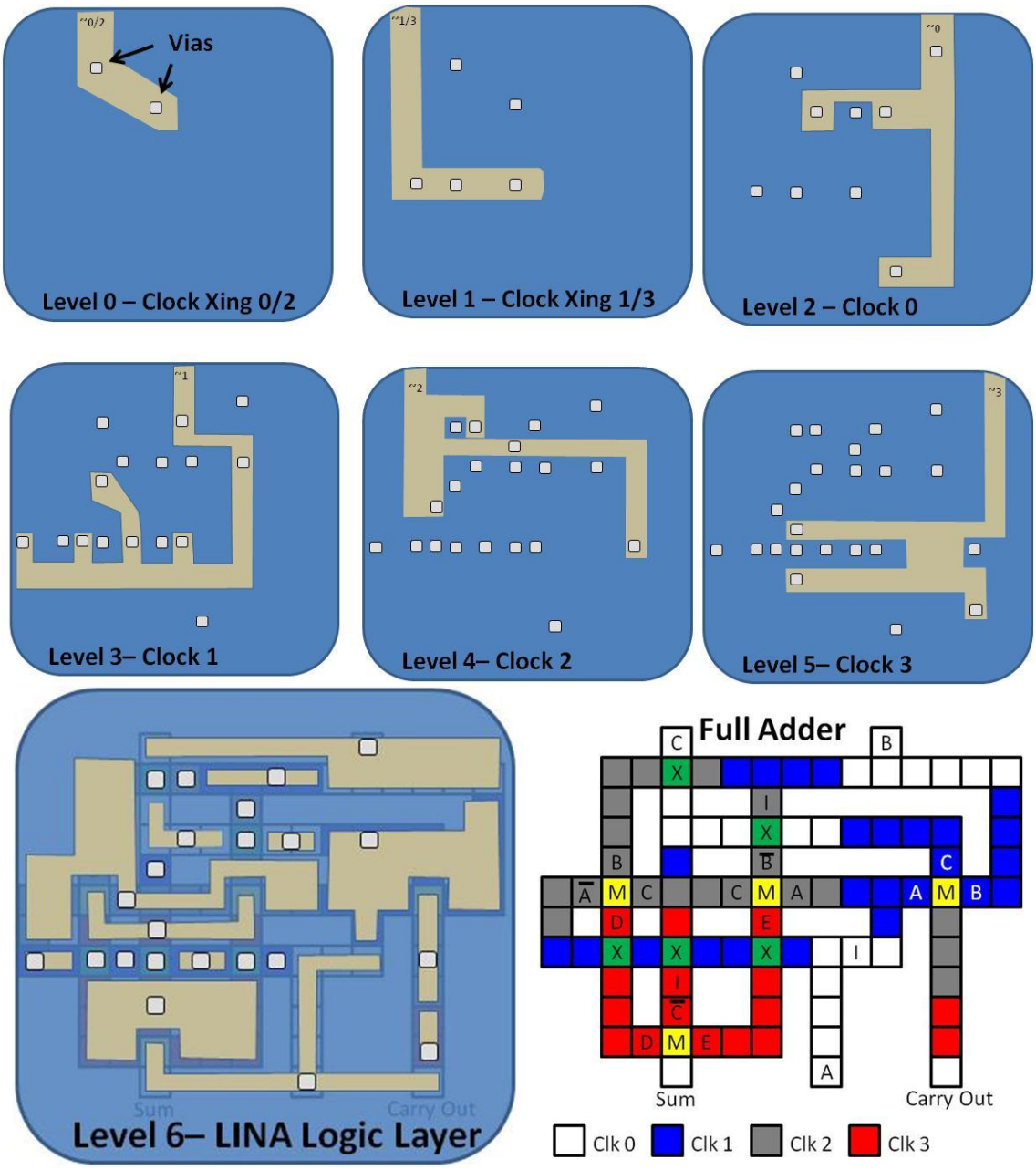


Figure 6-9. Proposal layout of clocking wires for full adder implementation

6.3 Chapter Summary

In this chapter a more thorough understanding of the tradeoffs between power, reliability, geometry, and speed was presented. This study culminated in the QCA full pitch metric that can be used to drive design decisions. Additionally, it was shown that LINA designs provide smaller circuitry for fixed speeds and reliability requirements as opposed to traditional QCA designs. These design metrics were then used to develop a LINA full adder. The full adder had requirements which dictated not only the design that was used, but also the material implementation used. In all, two implementations were presented, a 1-wide 4nm LINA implementation and a 3-wide 10nm LINA implementation. Clocking layers were also proposed for this structure based on the rule that the resolution of patterning technologies was ½ the size of the standard LINA block.

Chapter 7

Summary and Future Directions

This dissertation has provided designs and simulation results for a new nanoelectronics computing architecture based on the quantum-dot cellular automata (QCA) paradigm. The design, which is called the lattice-based integrated-signal nanocellular automata (LINA), retain the great potential of QCA in terms of size, speed, power dissipation, and logic; but also enable the potential for room-temperature operation and a viable path to VLSI scale circuit construction.

7.1 Dissertation Summary

The development of these new designs began with an introduction to the past, present, and future state of digital integrated circuit technologies. This introduction included the prospects for many nanoelectronics paradigms and highlighted the potential advances which could be garnered in size, power, and circuit speed if the major drawbacks of nanoelectronics circuits based on quantum-dot cellular automata (QCA) could be overcome. These drawbacks include the lack of viable path to implementation of QCA for precise placement and/or patterning of cells at the size scale required for reliable room-temperature operation. Major components in the challenges relating to these drawbacks are the lack of architecture which is amenable to self-assembled materials and the size of cells required to increase energy separations between ground and excited energy states in the traditional QCA designs. Therefore, the

need for a new design was exposed and the motivation for research that culminated in LINA was shown.

LINA is largely based on QCA principles and a thorough background into QCA was required before detailed discussions on LINA could occur. Therefore, it was shown that QCA is a theoretically well-developed nanoelectronics paradigm loosely based on the mathematical constructs of cellular automata. The physics of individual QCA cells and their interaction with each other was presented. Several different experimental QCA implementations were grouped into two categories of magnetic and electrostatic QCA which relate to the physical state variable used for computation. Each of these groups contained the fundamental logical elements of a binary wire, fan-out, inverter, and majority gate, thereby, achieving logical completeness and the ability to produce any desired logical function. Adiabatic switching and clocking of QCA were shown to be crucial to the proper operation of the paradigm and analysis into power, speed, and reliability showed this to be the case.

In order to break from the architecture of traditional QCA and provide a design which was amenable to self-assembled materials implementation, 2-D 2-dot QCA designs were presented. These designs utilize a cell composed of two logically interacting quantum dot locations and a single free electron. Cells in this design are positioned according to a 2-D 2-dot cell “map” consisting of a centered rectangular lattice with a two cell basis. Even with these restrictions on positioning, the fundamental logic components of a binary wire, fan-out gate, inverter, and majority gate were designed and were shown to have advantages

as opposed to traditional QCA designs. In order to demonstrate the design of more complex logic components, examples including an XOR and toggle flip-flop circuit were presented.

Circuits for the 2-D 2-dot QCA and LINA were simulated using modified software originally designed for the traditional QCA. Simulation engines based on thermodynamic Boltzmann distributions provide insight into the ground state and thermodynamic properties of circuit designs. The details of the Boltzmann simulation were given as were details regarding another potentially more powerful coherence vector simulation engine. The coherence vector engine relies on a density matrix approach to describe the dynamical state of a 2-dot QCA circuit and system. It provides information on logical state, temperature dependent reliability, circuit speed, power requirements for the QCA circuit being simulated. Results from both the Boltzmann distribution and the coherence vector simulation are critical in the design of traditional QCA circuits, 2-D 2-dot QCA and LINA.

With these foundations in place, the lattice-based integrated-signal nanocellular automata (LINA) design paradigm was presented. LINA offers an alternate design strategy which is more amenable to currently available or near-term nano-particle implementation technologies by adhering to lattice maps and cell types used in the 2-D 2-dot QCA and allowing for flexible wire widths to adjust to the resolution of large scale patterning technologies. LINA have also been shown to increase reliability in the presence of thermal excitations and assembly or patterning errors, thereby increasing the potential for room-

temperature operation and near term fabrication of cellular automata based computing systems. With these facts in mind, this work has built a foundation upon which LINA logical devices can be designed by developing a logically complete set of primitives including a LINA majority gate, inverter, and a planer wire crossing structure. LINA designs have also been evaluated in terms of the power/speed/reliability/area trades and have been shown to be advantageous compared to traditional QCA designs in this respect. As an example of the LINA design process, two LINA full adders was designed, laid out, and simulated with good results. Additionally, the requisite underlying clocking structure for this full adder was laid out and is shown to be able to be fabricated with even current technologies.

Taken as a whole, this work provides an important foundation to logical design of LINA nanoelectronic circuits and devices. In LINA, a strategy is provided that offers hope for large scale room temperature implementation and continued viability of the QCA paradigm to supplement and/or replace CMOS in the near future. Further, LINA offers the hope to extend the exponential increase in computing technologies into the next decades and overcome fundamental limitations being seen even today.

7.2 Future Directions

There are several areas of future work that should be pursued as a direct result of the foundations provided by this dissertation. One key area which must be pursued is research into material implementations of LINA. Certain materials have been shown to provide the self-assembled lattice structure that is

required, however, materials which provide the correct bipolar interaction and bistable nature in this lattice must be found. Once found, the properties of this material(s) must be extracted and applied to the calculations which were developed here to give a more exact representation of the limitations of the LINA architecture. Once a suitable material has been chosen, experimental implementations should proceed utilizing lithographical techniques for VLSI scale development.

Further development of materials also should lead to detailed reliability and fault tolerance models which take into account experimentally derived probabilities of layout and patterning faults. This will enable a design which is suitable to build full logic library of components necessary to the paradigm.

Simulation techniques provided in this dissertation are limited in the number of cells and devices which can be tested. As a deeper understanding of the attributes of suitable materials comes into view, these simulation engines should be extended to included research into probabilistic Bayesian networks which could be used to develop larger scale circuit design tools. These tools should then be integrated into currently existing design interfaces to bring the electronics community the tools necessary to develop circuits for LINA [113].

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