STUDY OF SOI ANNULAR MOSFET

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STUDY OF SOI ANNULAR

MOSFET

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Glossary

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
Rad-hard	Radiation hardened
RHBD	Radiation hardened By Design
TSMC	Taiwan Semiconductor Manufacturing Company
TID	Total Ionization Doze
SOI	Silicon On Insulator
SOS	Silicon On Sapphire
Vdd	Supply voltage
Gnd	Ground
Cgd	Gate to drain capacitance
W	Transistor Width
L	Transistor length
Weff	Effective width
Leff	Effective Length
Ion	On current
Ioff	Off current
DIBL	Drain Induced Barrier Lowering
SER	Soft Error Rate
ID	Drain current
VD	Drain voltage

VG	Gate voltage
VGS	Gate to Source voltage
VDS	Drain to Source voltage
PD SOI	Partially Depleted SOI
Ro	Output Resistance
V_{TH}	Threshold Voltage
TC	Transconductance

1 INTRODUCTION

1.1 Introduction

The scaling of CMOS technologies has followed the Moore's law with respect to the decrease in the feature size and increase in data throughput per chip. But there hasn't been a corresponding scaling in power supply as a result of the threshold voltage requirement to suppress leakage currents. This results in substantial increase in electric fields between the MOSFET channels and oxides with the scaled CMOS technologies. Increased electric field leads to increased reliability issues [12]. The insertion of lightly doped drains into the MOSFET channel reduces channel electric field and improves reliability to some extent, but it is not very effective for shrinking dimensions. This is a major concern in radiation environments.

In order to build radiation hardened devices enclosed transistors are built. These transistors eliminate the edges which are known to create leakage paths in NMOS transistors. These edgeless, radiation hardened transistors are also called annular transistors. The figure1-1 shows conventional rectilinear transistor and annular edgeless transistor.

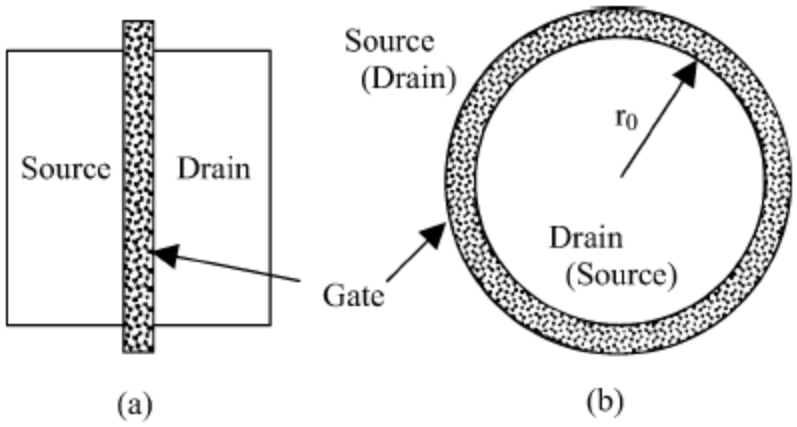


Figure 1-1 MOSFET layout (a) Conventional 2-edged (b) Annular edgeless showing inner radius of curvature [12]

This thesis studies annular transistor and its properties, based on the change of geometry at various temperatures, comparing it with the rectilinear transistor.

1.2 Motivation

The conventional bulk CMOS can operate satisfactorily only at moderate temperatures (typically up to 200°C). At higher temperatures, bulk CMOS circuits fail due to diode junction leakage currents which are proportional to the junction area, width and depth. The excessive leakage current can induce thermal latch up [15]. The leakage current and the latch up effect can be reduced by using SOI annular transistors. Thus the annular geometry transistor is investigated.

This study aims at evaluating the behavior of the annular transistor at room temperature and high temperature. The motivation behind this work is to understand the effects the geometry of the device has on the leakage current and kink effects, related to the NMOS SOS devices at various temperatures.

1.3 Thesis Organization

This thesis consists of 6 chapters. This chapter offers an introduction and the purpose of this study. Chapter 2 reviews the Silicon on Insulator process and makes a comparison to bulk CMOS. Chapter 2 describes the advantages and disadvantages of both processes. This chapter also briefly describes the Silicon on Sapphire process. Chapter 3 describes the annular transistors, their structure, advantages, disadvantages and their applications. The aspect ratio calculation and electric field intensity related to this geometry are discussed. Chapter 4 is a detailed explanation of the hypothesis made before conducting the experiments focusing on the relevance of the "what and why" the measurements were taken. Chapter 5 describes the experimental setup, the extraction procedure and the tests conducted. Additionally Chapter 5 discusses all the results along with the analysis of the experimental data. In this chapter we compare the annular transistors of different lengths and also compare the annular transistor of fixed length to the corresponding rectilinear transistor. Finally, chapter 6 concludes the work and mentions the future work.

2 SILICON ON INSULATOR

2.1 Introduction

Silicon on Insulator (SOI) technology has been researched for decades. SOI is attractive because it offers potential for higher performance and lower power consumption. SOI MOSFET performance depends on the silicon film thickness. SOI devices with a film thickness greater than the depletion region is commonly referred to as partially depleted. A fully depleted SOI device has an active silicon film thinner than depletion region and hence the whole body region is depleted [30]. SOI implementation can be achieved by using various insulators such as, sapphire or SiO_2.

Silicon-on-Sapphire (SOS) is one of several SOI manufacturing technologies. SOS is formed by depositing a thin layer of silicon onto a sapphire wafer at high temperature. SOS involves the epitaxial growing of silicon on a substrate of sapphire (Al_2O_3) and annealing the silicon film to improve film quality. Finally the film is LOCOS processed leaving islands of silicon in which to form transistors. The main advantage of SOS for electronic circuits is the highly insulating sapphire substrate. The benefit of the insulating substrate is very low parasitic capacitance, which provides increased speed, lower power consumption, better linearity, and substantially greater isolation than bulk silicon. The figure 2-1 below shows the SOS device.

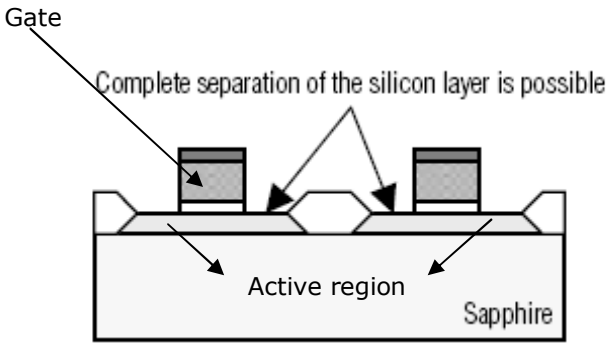


Figure 2-1 MOSFET cross-sectional structure of SOS device [18]

2.2 Bulk CMOS vs SOI device structures

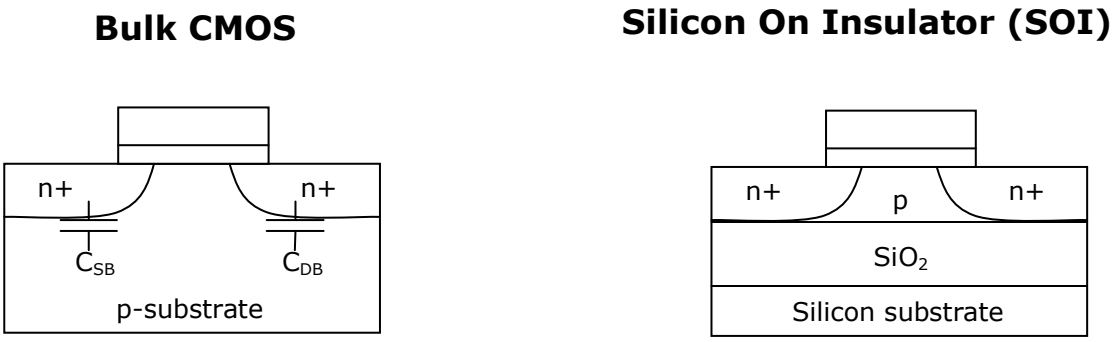


Figure 2-2 Device structures

The Processing techniques for the fabrication transistors in bulk and SOI CMOS are very similar. The basic difference between SOI and bulk CMOS technology is that the transistor source, drain and body are surrounded by insulating oxide rather than the semi-conductive substrate or well, Figure 2-2. In SOI technology the circuit elements are isolated dielectrically, which significantly reduce the junction capacitances and

allow the circuits to operate at high speed or substantially lower power at the same speed. The insulator layer in the SiMOX SOI devices is known as the buried oxide or BOX layer. This BOX layer provides isolation of transistors from silicon substrate underneath it, as shown in figure2-2.

2.2.1 S/D drain capacitance reduces:

In bulk CMOS device, the parasitic drain/source to substrate capacitance consists of two major components:

- The capacitance between the drain and the substrate
- The capacitance between the drain and the channel stop implant under the field oxide.

These capacitances increase with doping concentration.

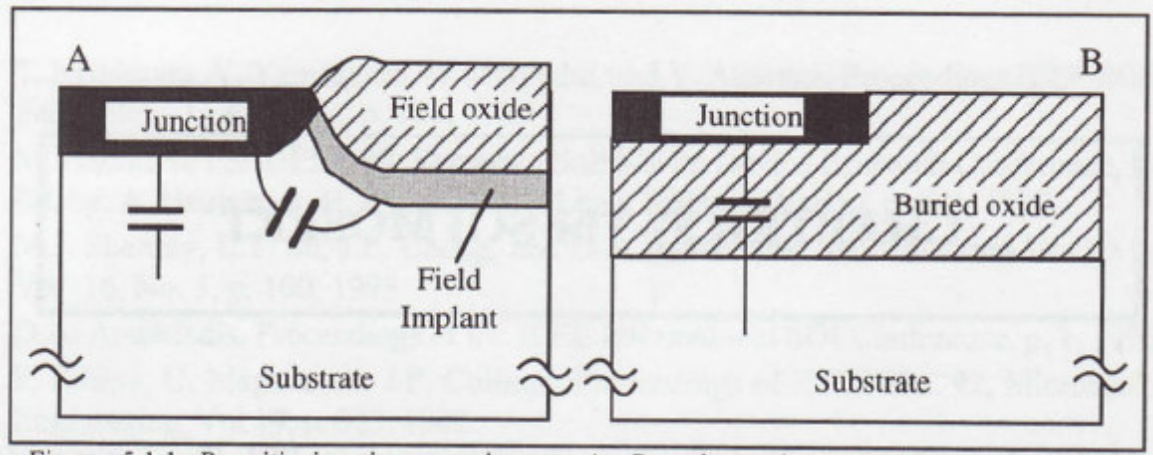


Figure 2-3 Parasitic junction capacitances

In SOI device the junction capacitance is reduced by eliminating the depletion region extending into the substrate. The value of source/drain capacitances is dictated by buried oxide layer capacitance which is much less as a result of the greater buried

oxide or sapphire BOX thickness. Note all depletion terms have been eliminated with the exception of the drain/sourced to channel. This reduction in parasitic capacitance gives the added advantage of increased speed [1].

Figure 2-3 shows the parasitic junction capacitances, with A.: Capacitance between a junction and the substrate and between the junction and the field (channel-stop) implant in a bulk device. B: Capacitance between a junction and the substrate, across the buried oxide, in an SOI device.

2.2.2 Short channel effects and Sub-threshold slope

In the case of short channel transistors, the channel is no longer under the control of just the gate but under the influence of both gate and drain. In a short channel device, the potential barrier is controlled by the electric fields due to the gate and the drain. As the drain voltage increases, the depletion region due to drain extends more into the channel reducing the gate voltage required to create an inversion layer of charge and hence leading to a reduction in threshold voltage. The reduced value of threshold voltage increases the off state leakage current. The short channel effect refers to the threshold voltage reduction with channel length for very short channel devices and the drain induced conductivity enhancement (DICE). Some other important short channel effects are velocity saturation, hot carriers, kink effect, DIBL (Drain Induced Barrier Lowering) and output impedance variation with drain voltage.

The short channel effects are smaller for SOI as compared to bulk CMOS due to the buried oxide layer in SOI devices. One of the major short channel effects observed is the variation in threshold voltage due to drain induced barrier leakage (DIBL). This effect is suppressed to a great degree in SOI by the thin-film structure of SOI [1]. The thin-film in SOI results in better control of the gate over the active region. The smaller equivalent capacitance of SOI results in better coupling of the gate voltage to the active region. This reduces the influence of DIBL and in addition decreases the sub-threshold slope. The combined effect of charge sharing and velocity saturation by lowering of depletion capacitance and saturation transconductance reduces the normalized kink effect ($\Delta I_D/I_D$) in short channel SOI MOS devices [33].

2.2.3 Latch up

In bulk CMOS, in the substrate, at the junctions of p and n material, parasitic pnp and npn bipolar transistors are formed. The cross-sectional view is as shown in the figure 2-4. Latchup can be caused by heavy ion strike in the bulk CMOS device where a parasitic n-p-n-p path. Latchup is triggered by excess current in the base of either of the parasitic transistors when a heavy-ion strikes i.e. an radiation environment. These bipolar transistors form a positive feedback path. Once triggered both the transistors conduct, and large amount of current flows through the device. This is due to a short between power and ground provided by the parasitic SCR.

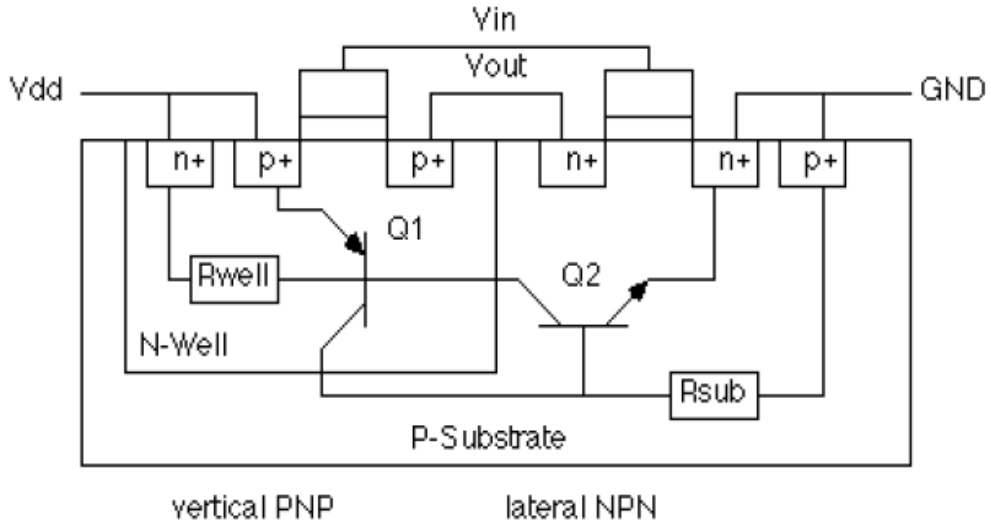


Figure 2-4 Latch up in bulk CMOS [27]

In SOI, a direct path between the various devices is eliminated by the presents of a layer of thick oxide which surrounds each device [1]. Alternately all potential DC paths are eliminated by combination of the BOX layer and a thin silicon film in which to form the devices. Hence latch-up never occurs in SOI. This is an advantage when using SOI for high temperature applications and in radiation environments.

2.2.4 Soft error rate (SER)

Soft errors are random nonrecurring transient single bit errors in memory devices. They are caused by a charged particle striking a semiconductor memory or a memory-type element. Specifically, the charge (electron-hole pairs) generated by the interaction of an energetic charged particle with the semiconductor atoms

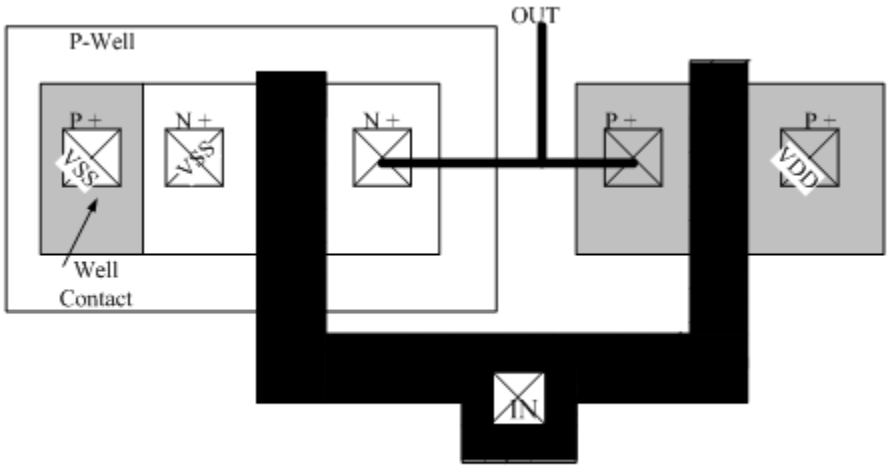
corrupts the stored information in the memory cell. These charged particles can come directly from radioactive materials, cosmic rays or indirectly as a result of high-energy particle interaction with the semiconductor itself. Alpha particles from radioactive elements in packaging are known to induce soft errors.

Due to the presence of buried oxide in SOI devices region through which alpha particles can pass is restricted to active silicon above the BOX layer. Therefore radiation events cause less charge generation and collection in SOI leading to lower soft error rate.

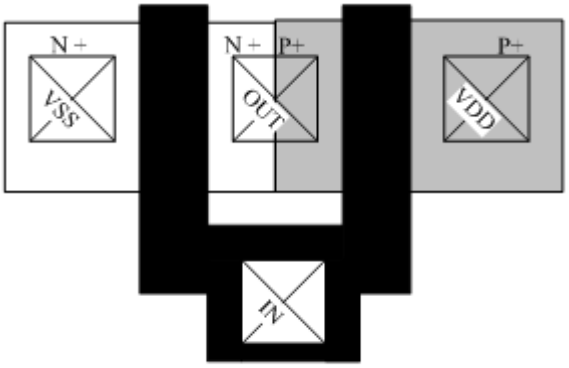
2.2.5 Device density

SOI CMOS devices offer greater device densities when compared to bulk CMOS. This is explained by figure 2-5 which shows the layout of and inverter using both the processes. The reason for higher device density of SOI devices are [1]:

- Absence of wells in SOI.
- Possibility of having direct contact between P+ and N+ junctions in SOI device, without concern for latch up.



(a) Layout of a bulk CMOS inverter



(b) Layout of an SOI CMOS Inverter

Figure 2-5 Device densities

2.2.6 Floating body effect

The MOS device always has a parasitic bipolar transistor between the source and drain terminals associated with it. This transistor is formed by back to back diodes between the source/body and drain/body junctions as shown in figure 2-7. In a bulk

CMOS device the base of this transistor is connected to ground through the substrate or the well contact. For the SOI device the base of the transistor is usually left floating. When the MOS transistor is biased in the saturation region and the drain voltage exceeds a specfic value when the source-body diode, in figure 2-7, turns on, the drain current suddenly rises with a discontinuity in the drain current on the IV curves. The bipolar device is turned on due to the impact ionization mechanism occurring as a result of the increased electric field near the drain. This discontinuity in the ID-VD curve is shown in figure 2-6.

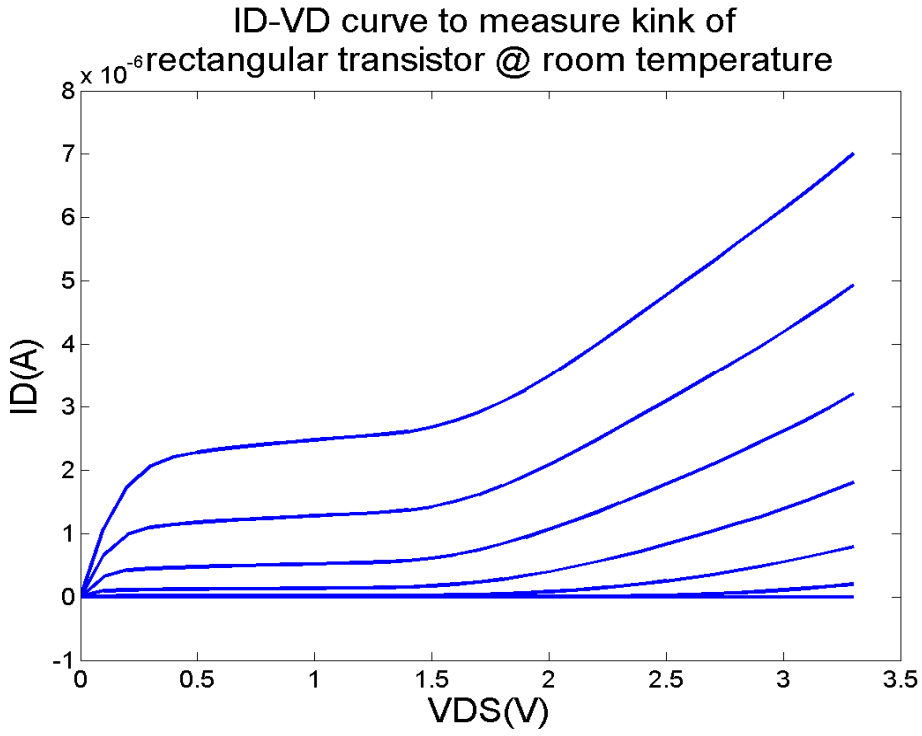


Figure 2-6 ID-VD displaying kink effect by varying VGS in steps of 0.1V from 0.3V to 0.9V, V_{TH}=0.268V

This effect is referred to as the kink effect. The kink effect adds to the standby leakage current and reducing the Ion/Ioff ratio.

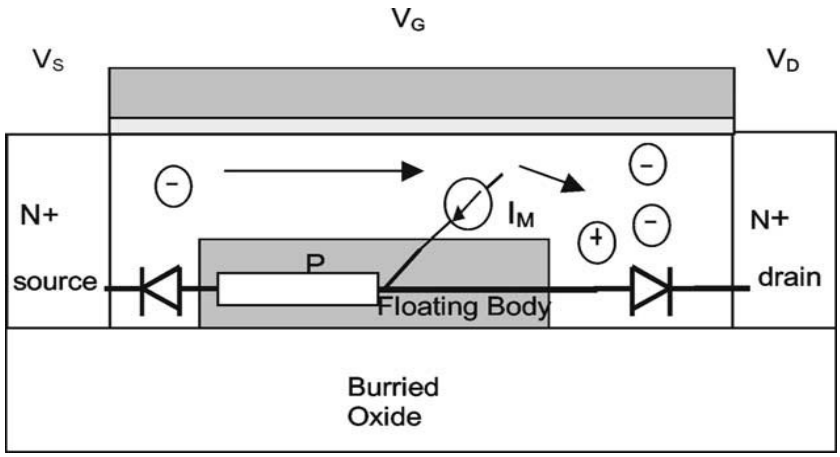


Figure 2-7 Occurrence of the kink effects in a PD NMOS device [23]

Kink effects are caused by impact ionization of the partially depleted (PD) SOI MOS devices and the parasitic BJT effect. As shown in figure 2-7 for a large drain voltage, the impact ionization caused by the mobile electrons with high energy within the high electric field region near the drain result in the generation of a large number of electron/hole pairs. The electrons move towards the positive drain in an NMOS device and the holes towards the more negative floating body and thus accumulate at the buried oxide (BOX) boundary near the source. Thus, the local body potential increases and the local threshold decreases, which triggers the rise in the drain current while the hole injected into the parasitic BJT via the BJT β trigger a sudden rise in collector current which is observed as MOS drain current. When the accumulation of holes and the related potential reach a certain extent, the

source/body diode turns on [23]. The injection current generated near the drain is given by:

$$Iholes,gen = Iso\ \left(exp\left(\frac{qVBS}{nkT}\right) - 1\right) \quad (2.1)$$

Where Iso is the saturation current source body diode, V_{BS} is the potential of the floating body and n is the ideality factor [1]. Based on equation 2.1 it is evident that with increase in temperature the kink current will reduce.

In case of FDSOI there is no significant potential barrier between the source and body, therefore holes can easily recombine in source without raising the body potential. Therefore V_{BS} in equation 2.1 does not change. As against this, in a PDSOI device, due to the presence of body current due to impact ionization is generated between drain and body. This current is collected through the source body diode, increasing the body potential. Therefore Kink effect is lower in FDSOI devices as compared to PDSOI devices. An approach to reducing or, minimizing or avoiding the kink effect is to connect a low impedance body contact to the source or the ground. However the body contact will increase the layout area and low impedance body ties are achieved with great difficult if at all in FD SOI.

2.2.7 Self Heating

SOI devices suffer from self heating. The oxide in the SOI device is a good thermal insulator along with being an electrical insulator. Thus the heat dissipated in switching transistors tends to accumulate in the transistor drain (or flow out the drain/source metal) rather than spreading into the substrate. The individual transistors with high current densities or dissipating large amounts of relative power may become substantially warmer than the die as a whole [4] in addition to warming their neighbor. The resulting higher temperatures reduce mobility and in turn reduce drain current resulting in slower switching speeds and a reduction in bandwidth.

2.2.8 Historic effect

PD SOI devices also suffer from hysteretic effects. Changes in the body voltage modulate the threshold voltage and adjust the gate delay. The body voltage depends on the device state, i.e. whether it has been idle or switching; therefore gate delay is a function of the switching history. An elevated or more positive (negative) body voltage reduces the NMOS (PMOS) threshold voltage and makes the gate faster. However, this associated with the uncertainty what the body voltage may be at any given instant previous results in switching and switching speeds that are a function of the presents state of the body. The history effect causes a mismatch between nominally identical transistors [4].The history effect can have

catastrophic effects with regard setup and hold in times regarding ms-D ff and state machines.

3 ANNULAR TRANSISTOR

3.1 Introduction

This chapter describes the radiation hardness and its effect on transistors. It also describes the uses of annular transistors and explains their geometry.

Annular transistors are mainly used in radiation hardened (Rad-hard) environments, such as, aerospace systems, military environment electronics and high energy physics measurement equipments. Annular transistors are used in these environments because they function more accurately and consistently in their environments which may be exposed to radiations. Complexity of specialized rad-hard technology, low volume demand, and area efficiency logic are some of the reasons this technology is not widely used. Accurate and complete models for annular devices typically do not exist as a part of the standard process design kit, therefore an entire remodeling for annular transistors must be completed, which is both expensive and time consuming considering the limited demand. In addition to the above reasons, these device structures are not very popular because some level of rad-hard tolerance is achieved in submicron processes without need for re-characterization. Submicron process achieve radiation hardness by using thinner oxides which provide fewer ionization charges, higher substrate doping and buried channel operation [28], i.e. 180nm 7RFSOI from IBM.

Annular MOSFETs have abnormal geometries and are studied since they have a high tolerance to radiation and total ionization dose. The annular MOSFET is radiation tolerant above 2Mrad, while the rectangular MOSFET is radiation tolerant to 50krad [20], a factor of 40 improvement. The reason for the great improvement in radiation tolerance is that the annular MOSFET has a drain or source, but not both, on the two sides of the bird's-beak region. Bird's beak region is the region that is formed on the edge of the device where the gate comes up over the field oxide, refer figure 3-1. The gate oxide of parasitic device is the bird's beak area at the ends of the drawn gate, where the holes can get trapped in a radiation environment. The trapped holes effectively bias the parasitic device and cause the threshold voltage to shift down and cause a significant current to leak from source to drain.

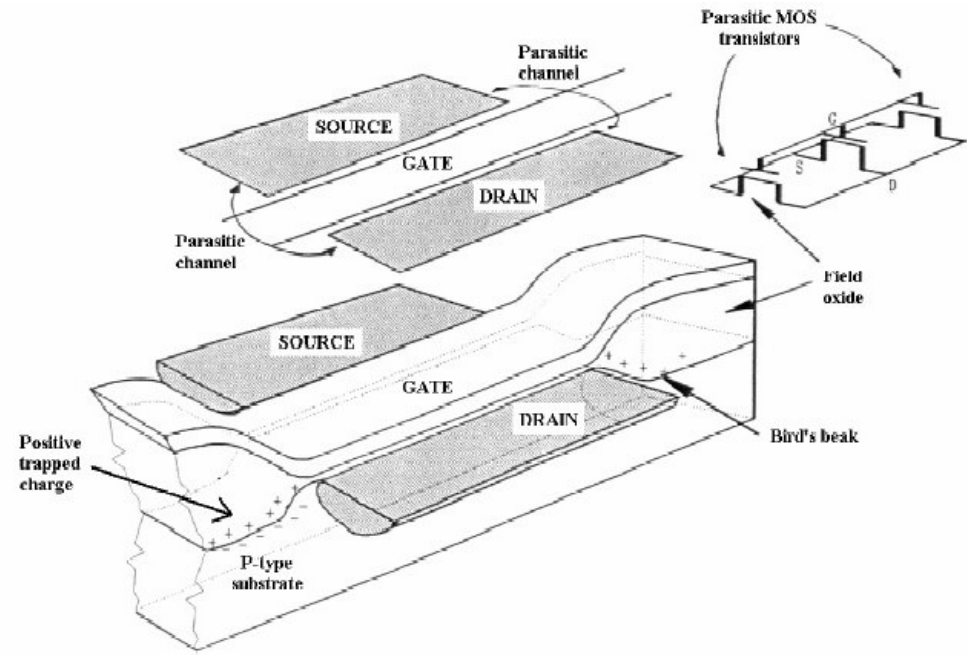


Figure 3-1 Illustration of Bird's Beak region with trapped holes [20]

Hence, even if there is a channel formed in that region, there is no potential across it to induce current flow. In addition an annular FET has a smaller gate to drain capacitance (Cgd) in the saturation region if the drain is on the inside of the gate than a standard MOSFET of equal Weff, the effective width of the gate, because the inner perimeter is smaller than Weff of the corresponding rectilinear transistor. This topic is covered in detail in the section 3.4

3.2 Radiation Hardening and Total Ionization Doze

To understand the purpose of annular transistors, which are used in radiation hardened environments, it is necessary to know what is meant by radiation hardness and the ionizing effect caused by the radiations. Radiation hardening is a method of designing and testing electronic components and systems to make them resistant to damage or malfunctions caused by high-energy subatomic particles and electromagnetic radiation. Rad-hard integrated circuits are manufactured to reduce the susceptibility to interference from high levels of electromagnetic radiation.

Due to radiation exposure, ionization effects occur as a result of exposure integrated circuit exposure to high energy particles (i.e. electrons and protons). These ionization effects are usually transient, creating glitches and soft errors (temporary memory loss), but can lead to destruction of the device if they trigger other damage mechanisms, for example, latchup or excessive leakage. Total ionization doze (TID) is the cumulative damage of the semiconductor lattice caused by ionizing radiation over the exposure time. TID is like sunburn to humans. Total dose is the cumulative

ionizing radiation that an electronic device receives over a specified interval of time. Like the sunburn, the damage is dependent on the intensity of the radiation and the length of exposure or in general the total dose. TID is measured in rads and causes slow gradual degradation of the device's performance; a total dose greater than 5000 rads delivered to silicon-based devices in seconds to minutes will cause long-term irreversible degradation [21].

3.2.1 Effects of radiation on regular CMOS device

In CMOS devices, the radiation creates electron–hole pairs in the gate insulation layers, which cause photocurrents during their recombination, and the holes trapped in the lattice defects in the insulator create a persistent gate bias and influence the transistors' threshold voltage, making the N-type MOSFET transistors easier and the P-type ones more difficult to switch on, a positive shift in threshold voltage. The accumulated charge can be high enough to keep the transistors permanently open (or closed), leading to device failure.

3.3 Annular transistors

Radiation hardened (Rad-hard) CMOS Bulk fabrication processes are rarely developed and would be expensive due to the small market size. Honeywell offers the only commercial radiation hard CMOS process. Radiation hardened By Design (RHBD) can be approached by using layout or circuit techniques. The majority of layout is frequently annular or other uses edgeless geometries, with drain/source

enclosing source/drain. In bulk annular CMOS device, the outer terminal needs to be source as explained in section 3.3.1. Such an approach is effective for the TID and the n-channel leakage effect is reduced through the use of an "enclosed" drain [5]. This is done by eliminating the leakage paths in the bird's beak region as discussed in section 3.1.

Annular transistors are an enclosed geometry transistor. The inner terminal, source/drain is fully surrounded by gate polysilicon. This eliminates the drain leakage through the ionized path produced by the charges trapped at the gate edges. By using the enclosed geometry, the channel electric field will be reduced by the curvature of gate poly and is modeled by the following equations [6].

$$V_{i+1} = A_i V + B_i V_{i-1} + C$$

Where,

$$A_i = \frac{\frac{2r_i}{\Delta r} + \frac{r_i \Delta r}{l^2}}{D_i}$$

$$B_i = \frac{0.5 - \frac{r_i}{\Delta r}}{D_i}$$

$$C_i = \frac{-I(r_i - r_0)\Delta r}{2\pi r_0 \varepsilon_{Si} z_j v_{sat} D_i}$$

$$D_i = 0.5 + \frac{r_i}{\Delta r}$$

$$l = \sqrt{\frac{\varepsilon_{Si} toxz_j}{\varepsilon_{ox}}} \,. \qquad (3.1)$$

In equation (3.1),

r_0 is the inner radius,

z_j is the junction depth,

Δr equals $\Delta L/n$,

ri equals r_0 plus $i\Delta r$.

vsat, ε_{ox}, and ε_{Si}, take on there usual meanings.

V_0 and V_1 are the initial conditions at the terminal edge of the poly.

Annular or edgeless transistors have the following useful properties:

1. Decreased inner diameter depletion capacitance [6]

Figure 3-2 above shows the annular transistor with inner/internal and outer/external drain. The inner and other terminals are not symmetric since they have different junction areas. The junction area determines the depletion region. A depletion region is an area depleted of mobile holes and electrons. The depletion layer of a PN junction is the interface of the junction, and (as the name implies) is depleted of charge carriers. The fixed atoms on each side of the junction within the depleted region exert a force on the electrons or holes that have crossed the junction. This equalizes the charge distribution in the diode, preventing further charges from the crossing the diode junction and gives rise to a parasitic capacitance. This parasitic capacitance is the depletion capacitance.

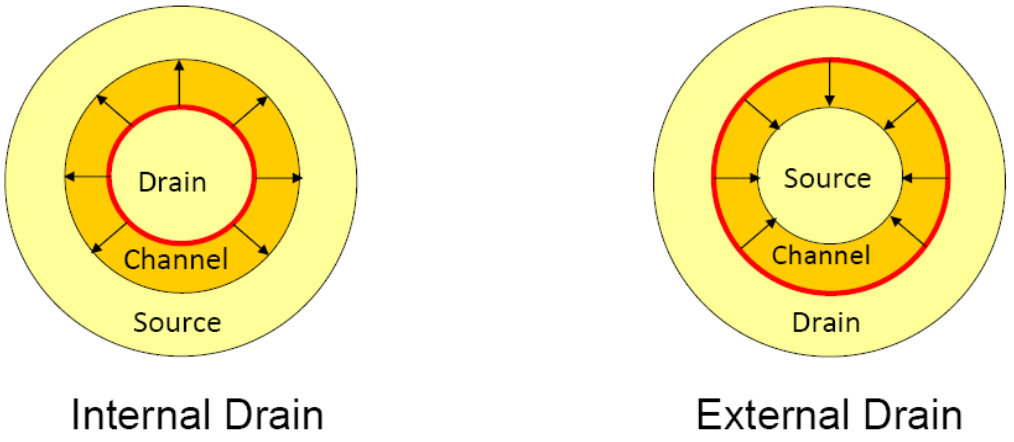


Figure 3-2 Annular transistor with inner drain terminal and outer drain terminal [15]

Under normal operating conditions this depletion layer of the semiconductor is capable of containing electrical charge carriers. The capacitance of the depletion layer is determined by it is the size (or width) by this equation,

$$Cpn = \frac{\varepsilon_o \varepsilon_r A}{Wd} \tag{3.2}$$

Where,

ε_o is the permittivity of free space

ε_r the relative permittivity of the semiconductor

W_d is the combined width of the depletion layers.

A is the junction area

From the above formula it can be observed that the depletion capacitance depends on the junction area. The inner terminal has a reduced area and therefore has lower depletion capacitance. This is at the expense of outer diameter capacitance.

2. Reduced electric field on the poly of outer annulus [6]. In annular transistors, the channel electric field changes by the curvature of the gate. However in regular rectilinear MOSFET it changes with an equivalent applied drain voltage. The equation shows that electric field intensity is inversely proportional to the drain area.

$$E = \frac{q}{\varepsilon A} \tag{3.3}$$

Where,

q is the charge

A is the area of the drain terminal

ε is the permittivity

Therefore the poly on the outer annulus has reduced electric field. A reduced electric field reduces the rate of depletion. This in turn decreases the output conductance. Therefore the output conductance is expected to increase with the inner drain terminal [5] [14].

Annular transistors have resulted in several unique applications to exploit the above mentioned properties;

- Low voltage differential signaling [7] (reduce inner drain C),

- Reduction of the drain (outer drain) electric field to improve radiation hardness and reliability [6].

3.3.1 Structure of Annular transistor

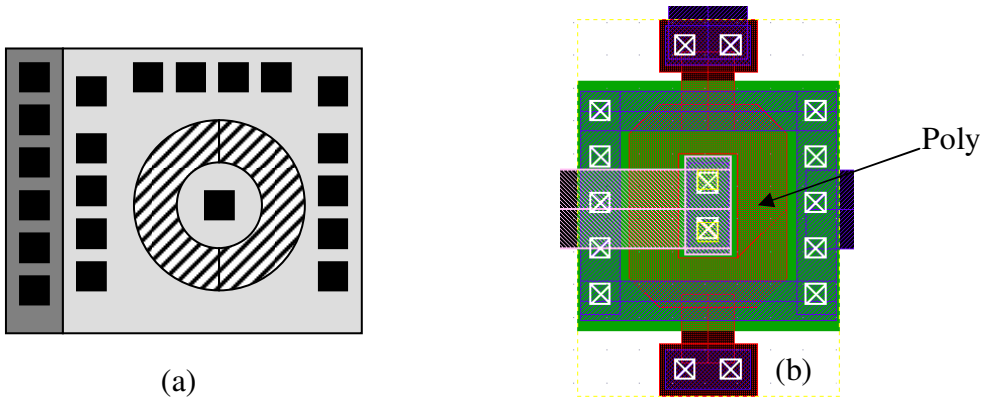


Figure 3-3 Structures of Annular transistor

Figure 3-3 (a) refers to an annular transistor for a bulk CMOS process and figure 3-3 (b) refers to annular transistor for a dielectrically isolated SOI process. In case of annular transistors using SOI process the source and the drain terminals can be used interchangeably. In case of bulk CMOS device, the source and the body need to be tied together. Therefore to keep the area small the source terminal needs to be the outer terminal. To use the inner terminal as source, the body contact needs to be at the inner terminal, which increases the size of the device. For the SOI annular transistor two contacts are used at the inner terminal to increase the reliability of the device.

By designing enclosed transistors, the channel electric field will change as per the curvature of the gate. As the electric field changes, the MOSFET reliability due to hot carrier generation at the drain gets affected. Reliability is increased by reducing hot carrier degradation, and reducing the injection of of hot channel electrons in into the gate oxide caused by impact ionization at the drain end of the channel where electric field achieves its maximum.

3.3.2 Disadvantages of annular transistor

The major disadvantages of these annular transistors are that:

1. The minimum size annular transistor which can be achieved is always larger than its corresponding rectilinear counterpart.
2. Inner source/drain terminal is less reliable due to fewer contacts, and two since it is maybe exposed to larger electric field when the inner contact is the drain.

3.4 Aspect ratio calculation

Figure 3-4 represents an elongated annular transistor. The shaded region is the gate polysilicon.

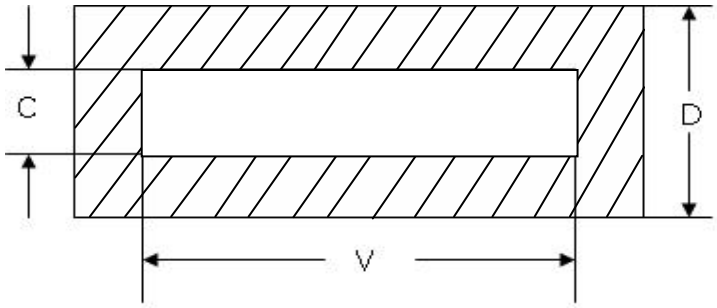


Figure 3-4 Elongated Square Annular transistor

The L and effective W of an annular transistor are calculated using the following estimation method [16]:

Elongated square annular transistor:

$$W_{eff} = 2V + C + D \quad (3.4)$$

$$L = (D-C)/2 \quad (3.5)$$

4 HYPOTHESIS

4.1 Early effect:

The Early effect is the variation in the width of the base in a BJT due to a variation in the applied base-to-collector voltage, named after its discoverer James M. Early [29]. A greater reverse bias across the collector–base junction, for example, increases the collector–base depletion width, decreasing the width of the charge neutral portion of the base at the expense of base width. Figure 4-1 shows how the ID-VD curve is extrapolated to determine the early voltage.

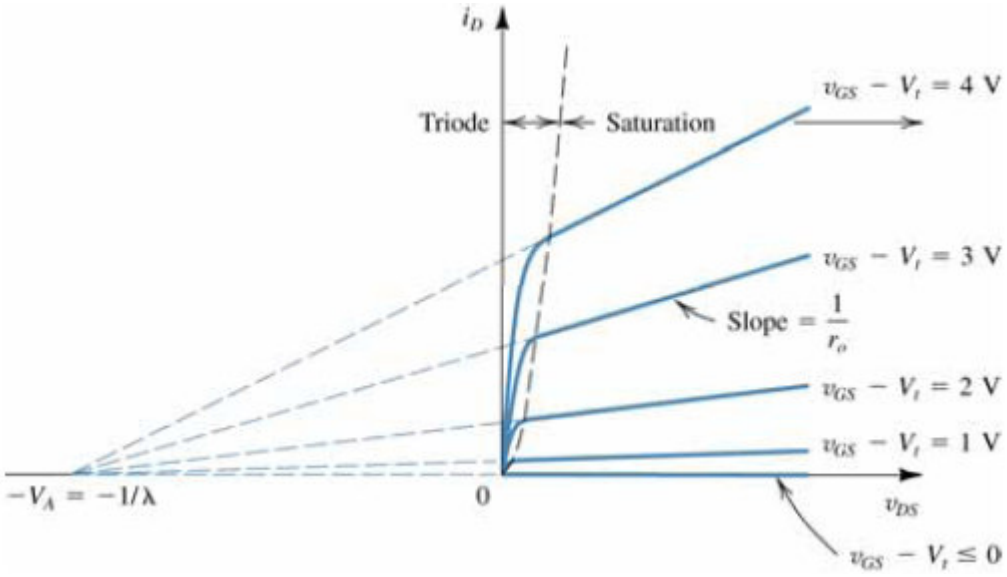


Figure 4-1 Early voltage [29]

At higher drain source voltages, junction depletion width grows, reducing the effective CMOS electrical channel length as it does in a bipolar device's base width. The reduction in effective channel length is due to an increase in reverse-bias voltage on the drain bulk junction. Because of the resemblance of the early effect results in bipolar and CMOS, the early effect extraction in BJTs is applied to MOSFETs as well.

$$R_O = \frac{1+\lambda V_{DS}}{\lambda I_D} = \frac{1/\lambda + V_{DS}}{I_D} \tag{4.1}$$

where V_{DS} = drain-to-source voltage, I_D = drain current and λ = channel-length (λ = $1/V_A$) modulation parameter, usually taken as inversely proportional to channel length *L*.

The early voltage depends on electric field intensity (V_{DS} and channel doping) and the effective channel length. When a strong electric field is applied, the effective channel length reduces and the early voltage is higher, as compared to when the lower electric field is applied. Therefore the annular transistor with inner drain terminal should have higher value of early voltage as against the outer drain.

4.2 Kink effect

The Kink voltage depends on elevating majority carriers past their ionization potential and electric field intensity at the drain terminal. The minimum VDS where

the slope of the IV curve breaks upward (sudden increase in drain current) is called the kink voltage. Note Figure 4-2. The kink effect worsens the differential drain conductance of the device. Again note the steep slope if in Figure 4-2. As discussed in chapter2, the kink occurs as a result of impact ionization which charges the body of the device and raises the body bias and increased drain electric field [19]. VDS voltage has a greater impact on the kink voltage as compared to VGS. Kink effect greatly worsens the performance of analog circuits whose region of interest is in moderate inversion or weak inversion (subthreshold region). In subthreshold region and or moderate inversion, beyond the kink voltage (between 1.5 and 2 V), the Ioff current is dominated by the kink current. This effect is shown in figure 4-2, for a annular transistor of L=1.6um and VGS=0.3V. *Note that in figure 4-2 there is essentially a total loss of control of the transistor current by VGS when VDS is above 2 to 2.5V!*

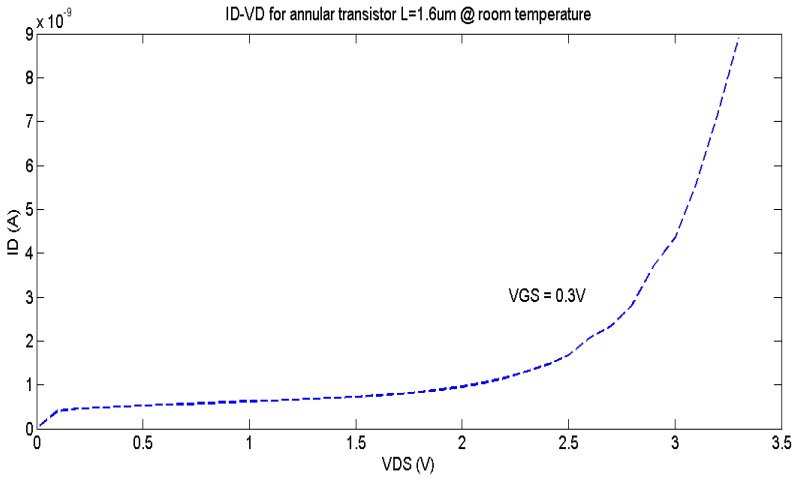


Figure 4-2 ID-VD for annular transistor of annular transistor with inner drain for VGS = 0.3V and V_{TH} = 0.33V

The derivation of the kink effect modeling is presented in [26]. Based on this model, the onset of kink effect at larger VDS can be achieved with lighter doping density in thin film. Equation 4.2 is used to determine Vkink [26]

$$V_{\text{kink}} = V_{\text{DSAT}} + \frac{-E_2 - \sqrt{E_2^2 - 4E_1E_3}}{2E_1}, \quad E_1 = \ln\left(\frac{I_{\text{reco}}}{I_{\text{CH1}}\frac{\alpha}{\beta}}\exp\left(\frac{V_{\text{BES}}}{2kT/q}\right)(e^{0.25}-1)\right) - 2,$$

$$E_2 = \ln\left(\frac{I_{\text{reco}}}{I_{\text{CH1}}\frac{\alpha}{\beta}}\exp\left(\frac{V_{\text{BES}}}{2kT/q}\right)(e^{0.25}-1)\right) + 2 + E_3, \quad E_3 = \frac{\beta}{\sqrt{\frac{\epsilon_{ox}/\epsilon_{si}}{t_{ox1}X_c}}}, \quad I_{\text{CH1}} = \frac{W}{L}\mu_{\text{eff}}C_{\text{ox}}V_{\text{DSAT}}$$

$$\times \frac{\left(\left(V_G - V_{fb} - 2\phi_f - \gamma\sqrt{2\phi_f - V_{BES} - \frac{1}{2}\frac{kT}{q}}\right) - \frac{1}{2}\left(1 + \frac{\gamma}{2\sqrt{\phi_s + 2\phi_f - V_{BES} - \frac{1}{2}\frac{kT}{q}}}\right)V_{DSAT}\right)}{1 + \theta\left(V_G - V_{fb} - 2\phi_f - \gamma\sqrt{2\phi_f - V_{BES} - \frac{1}{2}\frac{kT}{q}}\right) - \theta_B\left(V_{BES} + \frac{1}{2}\frac{kT}{q}\right)} \tag{4.2}$$

The kink voltage is expected to remain unchanged with inner drain or outer drain configuration of the annular device. As a result measured kink behavior should match with the corresponding rectilinear device.

4.3 Leakage current

Ion/Ioff ratio determines the effectiveness of the MOSFET as a switch. In SOI devices channel leakage is comprised of subthreshold currents, tunneling currents and side

wall interface currents. In SOI the OFF-state leakage currents are quite frequently dominated by the subthreshold currents. In bulk leakage is dominated by the thermal generation currents of the well diode junction along with the subthreshold currents. The thermally generated current of the well junction is large as a result of the larger junction area [32]. Ion is the on-current of the device and Ioff refers to the off-state leakage current. Excess leakage current i.e., greater Ioff results in higher power consumption and lower temperature isolation.

4.4 Effects of high temperature

There are four primary temperature dependent parameters of concern used in modeling CMOS devices: electron mobility, generation/recombination lifetimes and impact ionization. These physical parameters affect the threshold voltage, subthreshold slope, Ion/Ioff ratio, and the kink effect.

4.4.1 Mobility:

Electron mobility is dependent on the doping concentration and the operating temperature. Electrons and holes mobilities in a doped semiconductor decrease due to the increase of phonon effects with the temperature. This effect can be summarized by equation 4.3 [31].

$$\mu 0(T) = \mu(Tnom)\left(\frac{T}{Tnom}\right)^{\mu te} \qquad (4.3)$$

From equation 4.3 and figure 4.3 it is observed that mobility decreases with increase in temperature.

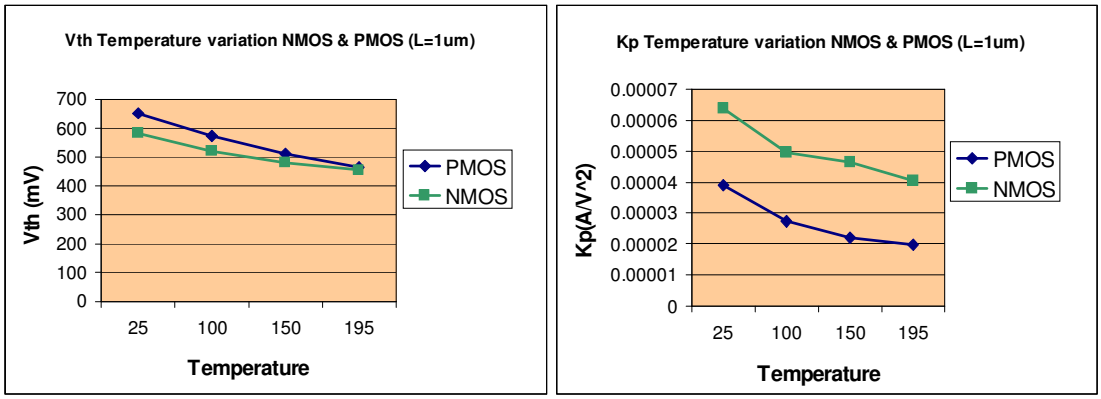


Figure 4-3 Variation of threshold voltage and current factor with temperature (25°C to 195°C) for NMOS and PMOS with L=1um. [32]

4.4.2 Threshold Voltage:

The threshold voltage V_{TH} is an important parameter for characterizing electrical MOSFET behavior. It corresponds to the onset of inversion channel build-up, and the conduction between the drain and the source can occur. Threshold voltage is used to control off state leakage, determine the noise margins and the switching speed of the circuit. . Hence it is a very useful parameter for digital circuits.

V_{TH} will change with a significant variation in channel length, but a minor change in channel length will a very limited effect on threshold voltage shift. Threshold voltage decreases with increase in temperature, due to Fermi level and bandgap energy shifts. V_{TH} depends approximately linearly on temperature as shown in figure 4-3 and

specified by equation 4.4 [32], over a wide range of temperature for devices with long channel lengths.

$$V_{th(T)} = V_{th(Tnom)} + (K_{T1} + K_{t1l}/L_{eff} + K_{T2}V_{bseff})(T/T_{nom} - 1) \quad (4.4)$$

Figure 4-3 shows the variation of threshold voltage with temperature. It is observed that with increase in with threshold voltage reduces. The threshold voltage temperature coefficients were found to be 0.75mV/^{o}C and 1.1mV/^{o}C for NMOS and PMOS respectively [32].

4.4.3 Subthreshold Slope:

Subthreshold slope, which may be defined by an amount of gate voltage increase required to produce a decade change in drain current. Reduced subthreshold slope may enable the formation of circuits with enhanced switching sensitivity; wherein small changes in gate voltage may control switching of the device from an off-state condition of very low leakage (Ioff) to an on-state condition of high drive (Ion). Equation 4.5 is used to determine subthreshold slope.

$$Subthreshold\ slope = \frac{\delta VGS}{\delta(\log_{10} Ioff)} = \frac{\eta V_T}{\log_{10} e} = 2.3\left(1 + \frac{Cf}{Cox}\right)\frac{kT}{q} \quad (4.5)$$

From equation 4.5 it can be observed that subthreshold slope has a direct relation with temperature. Therefore subthreshold slope increases with increase in temperature.

4.4.4 Leakage Current:

Leakage current is proportional to intrinsic carrier concentration. With the increase in temperature, n_i increases exponentially. Leakage current is defined using the Ion/Ioff ratio. For the SOS processes the greater the Ion/Ioff ratio, the lower is the leakage for any given device length. Ioff is typically dominated by the subthreshold current. Ion and Ioff can be determined using equation 4.5 and 4.6 respectively.

$$Ion = \mu\, Cox\, \frac{W}{L}\, (\Delta V)^2 \tag{4.7}$$

$$Ioff \approx I_t \left(\frac{W}{L}\right) e^{(q(V_{gs}-V_{TH})/nkT)} \tag{4.8}$$

$$\frac{1}{n} = \frac{Cox}{Cox+Cj} \tag{4.9}$$

$$I_t = 2n\mu Cox\, U_T^2 \tag{4.10}$$

Where W is the width of device, L is the length, ΔV is the effective voltage, μ is the mobility, Cox is the gate oxide capacitance, U_T is the thermal voltage, I_t is dependent on the process and channel length.

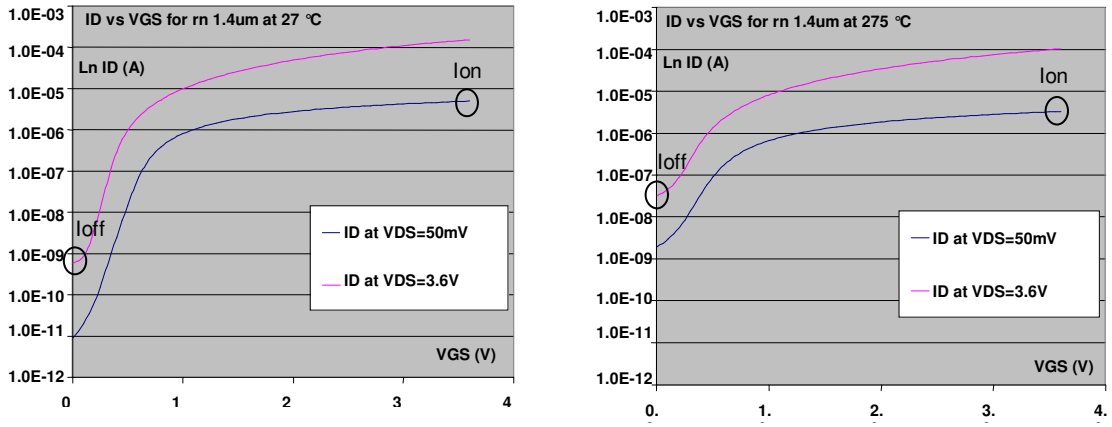


Figure 4-4 Logarithmic plots to measure Ion and Ioff at 27˚C and 275˚C for rectangular NMOS L=1.4um

Therefore, leakage current contributes to the total current at high temperature.

Figure 4-4 shows a graphical method to determine the Ion and Ioff currents. It can be observed that the Ion/Ioff ratio degrades with temperature as a result of the degradation in threshold and carrier mobility.

4.4.5 Kink effect:

At higher operating temperature and with a lighter thin-film doping density, the onset of kink effect occurs at a larger VDS [25].

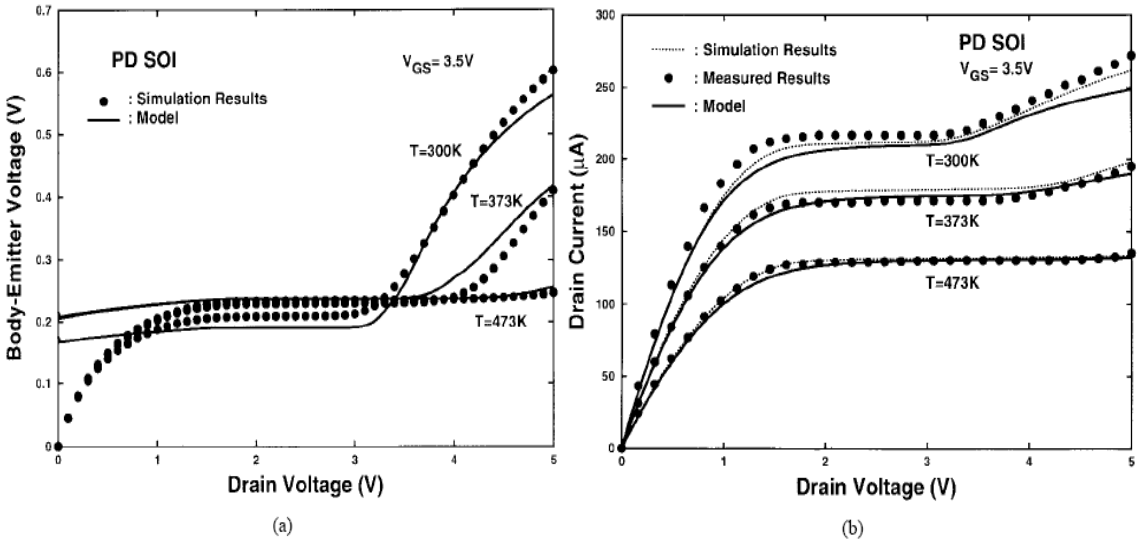


Figure 4-5 (a) VBE (b) ID versus VDS of the partially-depleted SOI NMOS device based on the analytical model, the experimental data [25]

Figure 4-5 (a) shows the variation in the VBE voltage of the parasitic bipolar transistor with respect to temperature. Figure 4-5 (b) shows how the VBE affects the kink voltage with change in temperature. With the increase in temperature the impact ionization current reduces and therefore the kink voltage increases.

4.5 Summary

Effect of temperature on threshold voltage, subthreshold slope, leakage current and output conductance can be summarized as shown in figure 4-6

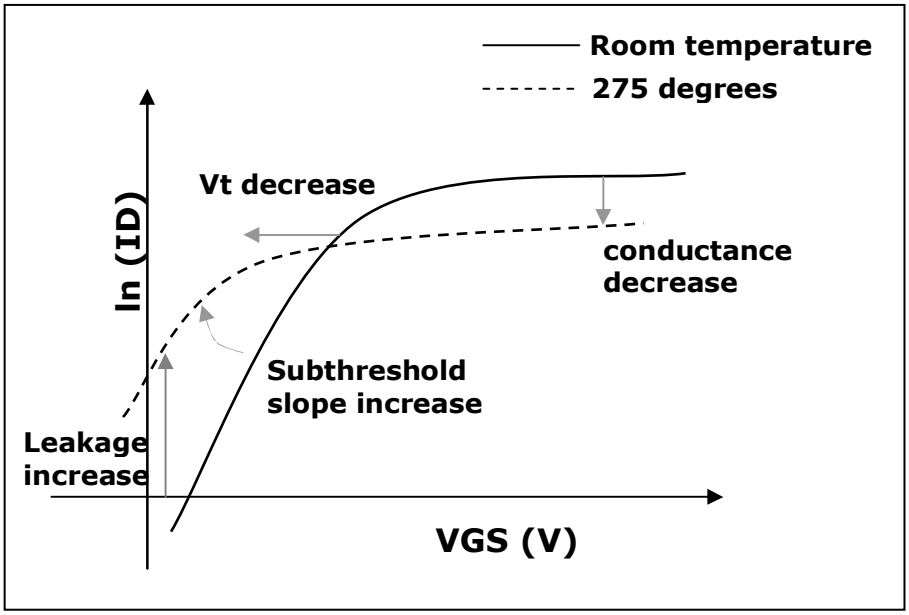


Figure 4-6 Temperature effects on device parameters

5 MEASUREMENTS

5.1 Experimental Setup

The experimental results are based on current and voltage measurement of the large signal drain versus gate characteristics of the transistors. A Keithley 4200 Semiconductor Characterization System was used to perform the measurements. Regular ID-VGS and ID-VDS curves are swept limited to 3.3V VDS with 0.1V stepping and VGS is set to 0.5V step. For analog applications higher resolution were used to investigate output resistance and kink effect, the VGS step size is reduced to 0.1V and limited to the maximum of 1V. To evaluate the thermal effects, the characterization procedures were repeated for room temperature and 275°C. For temperature settling accuracy of the test dies, a soak time of 5 minutes wait time was observed. The test structures of the conventional rectangular NMOS transistor and the annular NMOS transistor were fabricated using Peregrine 0.5um SOS process.

5.2 Extraction procedure

The drain current (ID) as a function of gate-source voltage (VGS) is shown in figure 5-1 The ID-VG curves were measured for VDS=50mV and VDS=3.6V. From these graphs, threshold voltage and Ion/Ioff ratio can be determined.

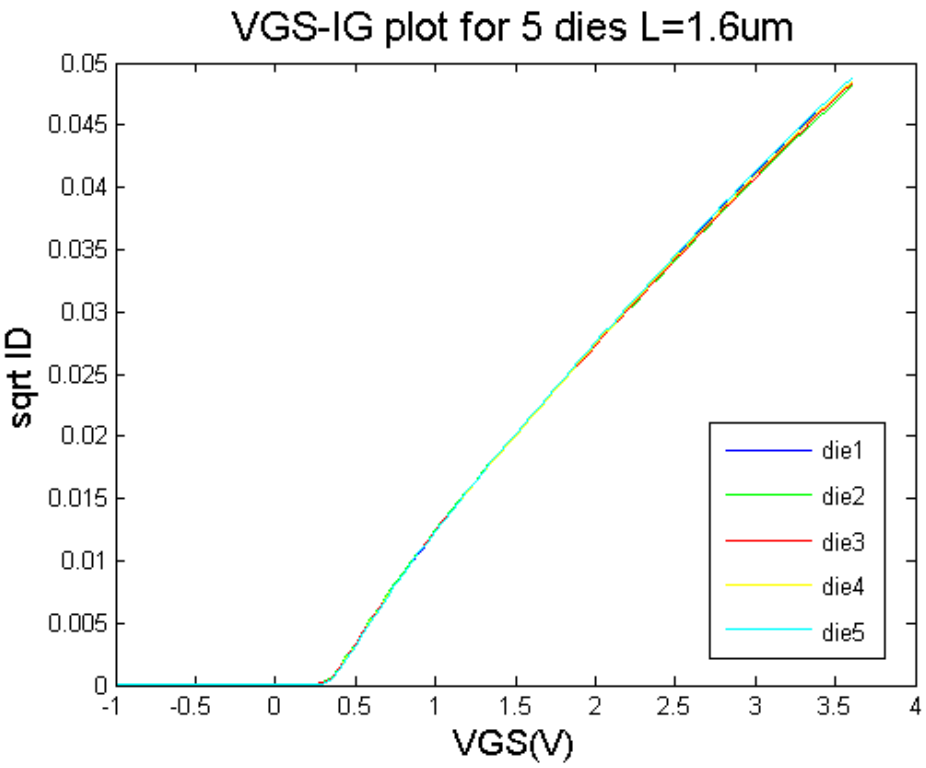


Figure 5-1 ID-VG curve for annular transistor with outer drain of L=1.6um

The figure 5-1 represents the ID-VG curve of five dies of L=1.6um. These curves are superimposed to bring out the characteristic that threshold voltage does not vary across the various dies on which measurements are taken.

This figure 5-2 illustrates the ID-VD characteristic of annular transistor with inner and outer drain. The VDS voltage is swept from 0V to 3.3V, and the VGS voltage is varied in the steps of 0.5V from 0.3V to 3.3V. The kink voltage and output resistance are determined using the same data used in generating this plot.

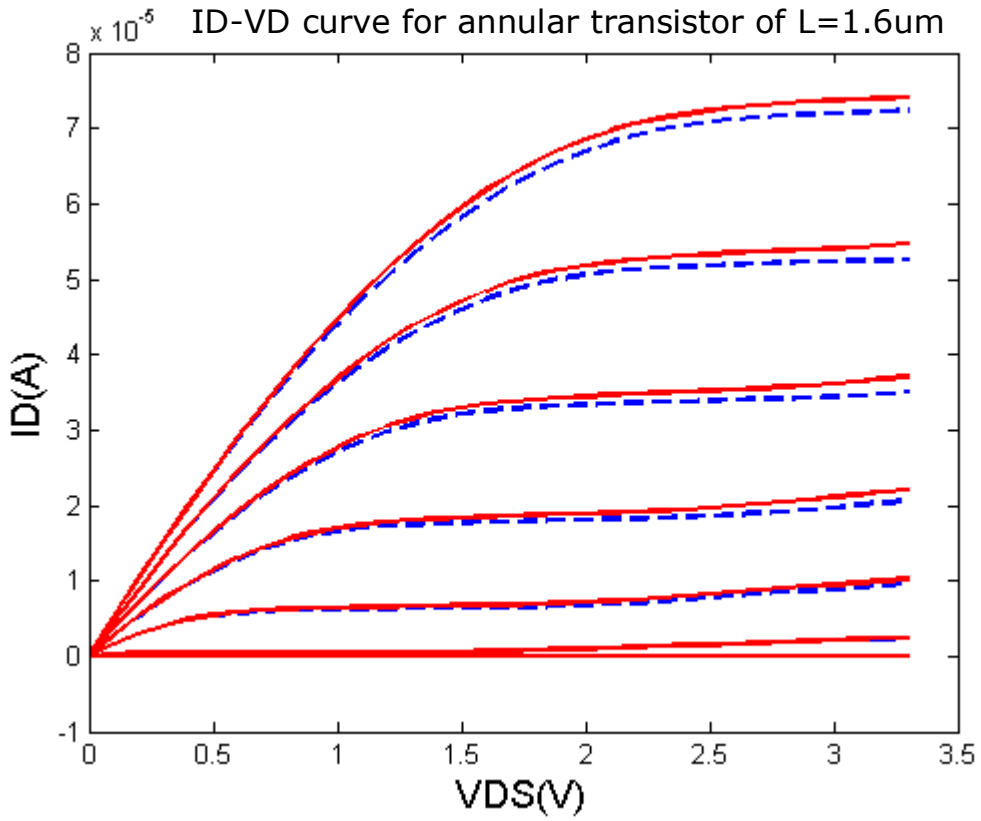


Figure 5-2 ID-VD curve for annular transistor of L=1.6um

The dotted line represents ID with outer drain terminal and the solid line represents the ID current with inner drain terminal. This observation is consistent with the literature [5]. From figure 5-2 it is evident that the drain current is with the inner drain terminal is greater than the outer drain terminal because of increased electric field intensity.

Annular transistors are not symmetric therefore we measure the characteristics for both the inner drain and outer drain terminal.

All measurements were taken for the following lengths of annular transistor, L=1.3um, 1.4um, 1.5um and 1.6um. The corresponding widths of these transistors

are: 12.4um, 12.8um, 13.2um and 13.6um. Ten dies of each length were measured. For comparison rectangular transistors for L=1.4um are also measured. The rectilinear transistor has 20fingers of width, W = 1.4um and a lenght, L = 1.4um. All measurements are taken at room temperature and 275°C.

5.3 Measurement of threshold voltage

5.3.1 Experimental Procedure

Threshold voltage is measured by plotting the ID-VG curve, in the saturation region. VGS-ID curve is obtained by keeping the VDS constant at 3.6V and sweeping VGS from -1V to 3.6V. V_{TH} is extracted by extrapolating the slope of the VG-ID curve to the point where it meets the x-axis.

The figure 5-3 shows the ID-VG curve for an annular transistor with inner drain terminal and outer drain terminal super imposed.

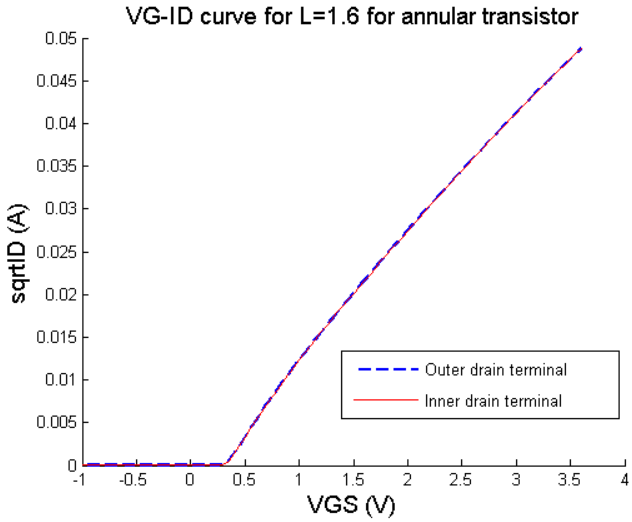
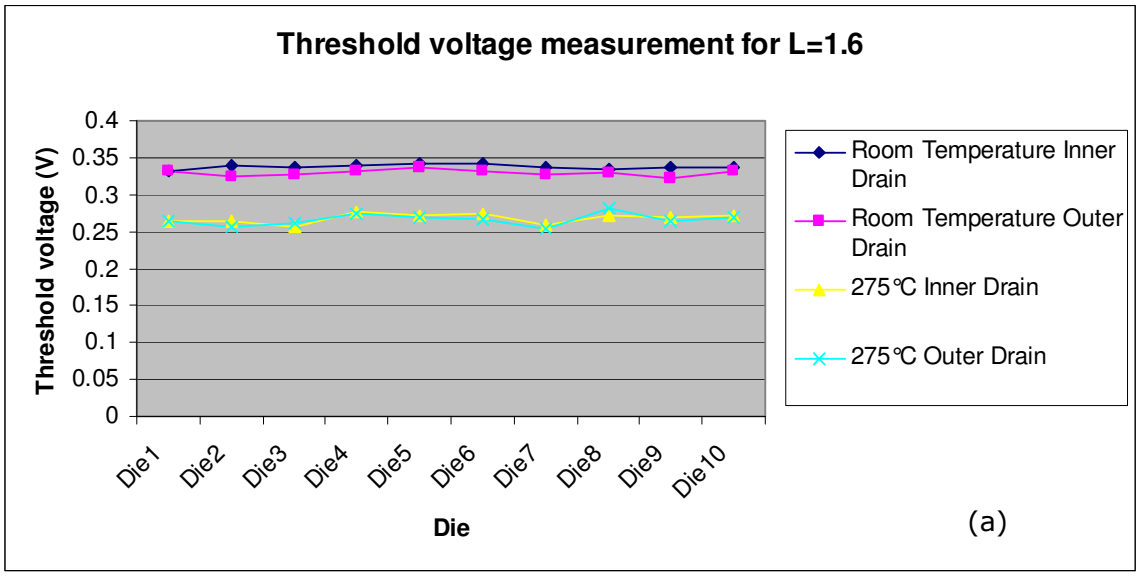
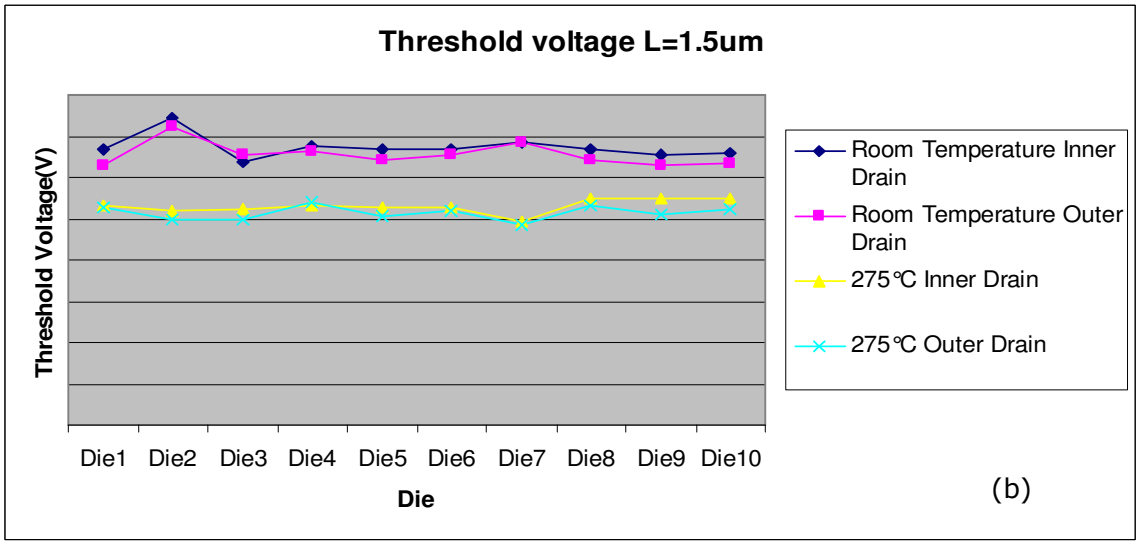


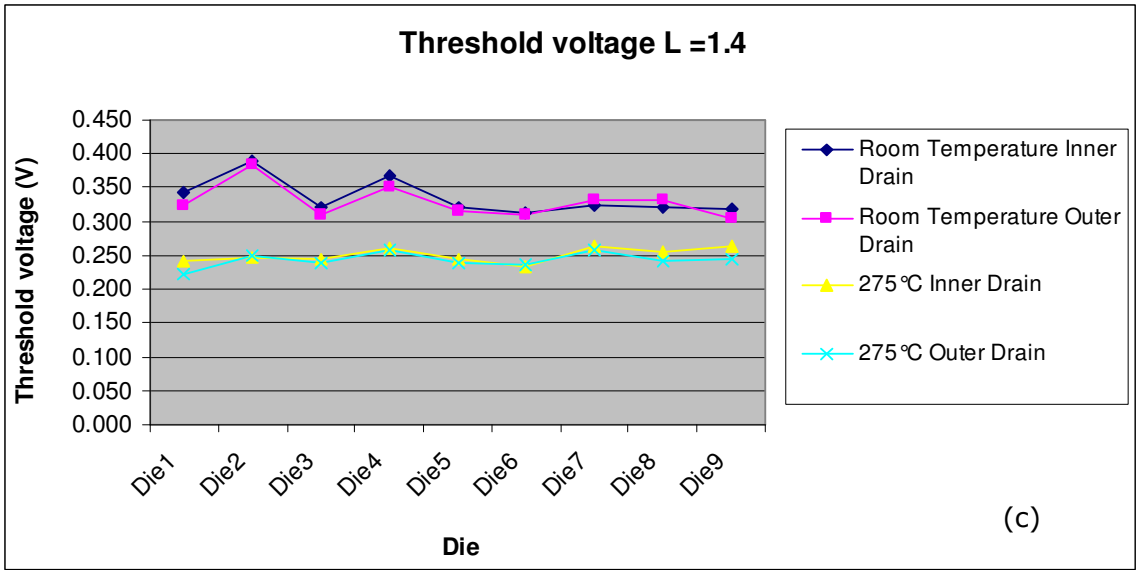
Figure 5-3 VG-ID curve for annular transistor of L=1.6um

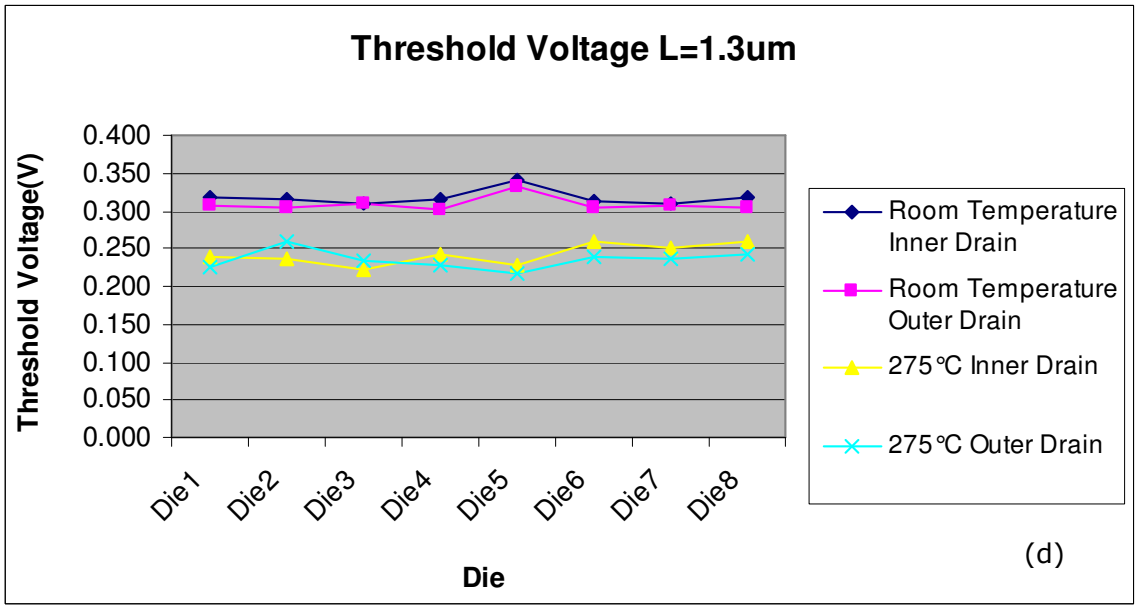
5.3.2 Observations

The figure 5-4 show the variation of threshold voltage across 10 dies of annular transistor with inner and outer drain terminals and rectilinear transistor. These graphs depict the values of V_{TH} at room temperature and at 275ºC.






Threshold voltage L =1.4
Threshold voltage (V)
0.450
0.400
0.350
0.300
0.250
0.200
0.150
0.100
0.050
0.000
Die1
Die2
Die3
Die4
Die5
Die6
Die7
Die8
Die9
Die
Room Temperature Inner Drain
Room Temperature Outer Drain
275℃ Inner Drain
275℃ Outer Drain
(c)


Threshold Voltage L=1.3um
Threshold Voltage(V)
0.400
0.350
0.300
0.250
0.200
0.150
0.100
0.050
0.000
Die1
Die2
Die3
Die4
Die5
Die6
Die7
Die8
Die
Room Temperature Inner Drain
Room Temperature Outer Drain
275℃ Inner Drain
275℃ Outer Drain
(d)

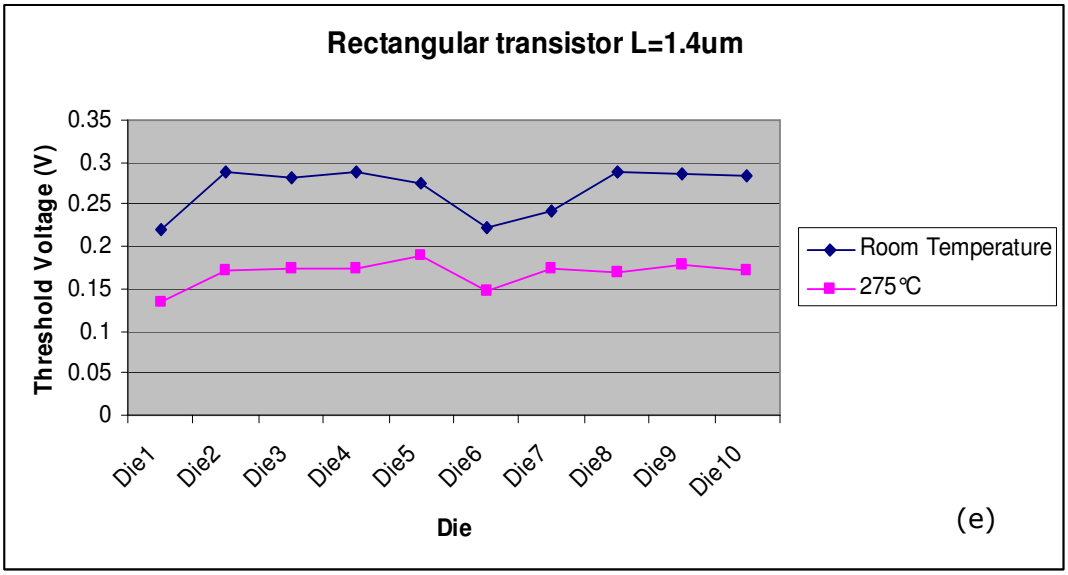


Figure 5-4 Threshold Voltage Measurements (Figures (a)-(d) refer to annular transistors (a) L=1.6um, (b) L=1.5um, (c) L=1.4um, (d) L=1.3um (e) Rectangular transistor L=1.4um)

5.3.3 Inference

The table 5-1 lists the mean and the standard deviation values of threshold voltage, measured across 10die of each length, at room temperature and 275°C.

Table 5-1 Threshold voltage comparison

Length(um)	Annular transistor	Mean V_{TH}		Standard deviation V_{TH}	
		Room Temperature	275°C	Room Temperature	275°C
1.3	Inner Drain	0.319	0.245	0.010	0.012
	Outer Drain	0.308	0.235	0.011	0.014

1.4	Inner Drain	0.335	0.250	0.027	0.011
	Outer Drain	0.329	0.243	0.025	0.011
1.5	Inner Drain	0.336	0.265	0.014	0.008
	Outer Drain	0.328	0.257	0.015	0.009
1.6	Inner Drain	0.338	0.268	0.003	0.007
	Outer Drain	0.330	0.266	0.004	0.008
1.4	Rectilinear transistor	0.268	0.168	0.028	0.016

It is observed that there is a slight increase in threshold voltage with the inner drain terminal as compared to outer drain terminal. There is a approximately 8% and 11% increase in V_{TH} for inner and outer drain terminal respectively, when channel length increases from 1.3um to 1.6um, at room temperature and 275°C. There is approximately 25% increase in threshold voltage from rectangular transistor to annular transistor with outer drain. Threshold voltage decreases with increase in temperature with a temperature coefficient is approximately 0.3mV/°C for annular transistor and 0.4mV/°C for rectangular transistor. Both the observations are in line with the hypothesis stated in section 4.4.2. The data as expected shows a reduction in Vos with increase in area consistent with a Pelgrom coefficient of AVT = 11.67mV-um [32].

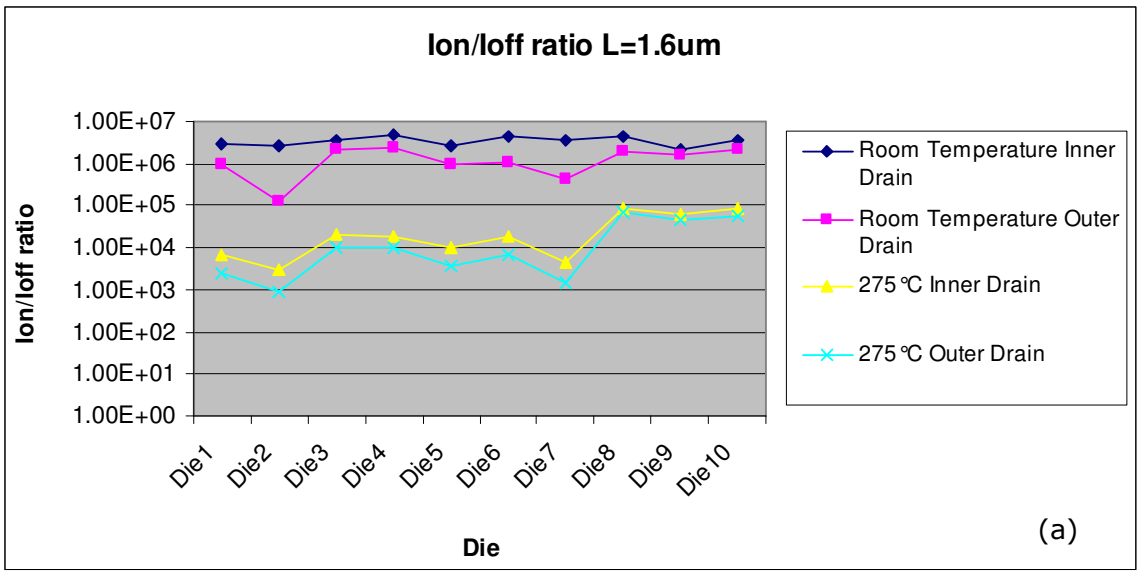
5.4 Measurement of Ion/Ioff ratio

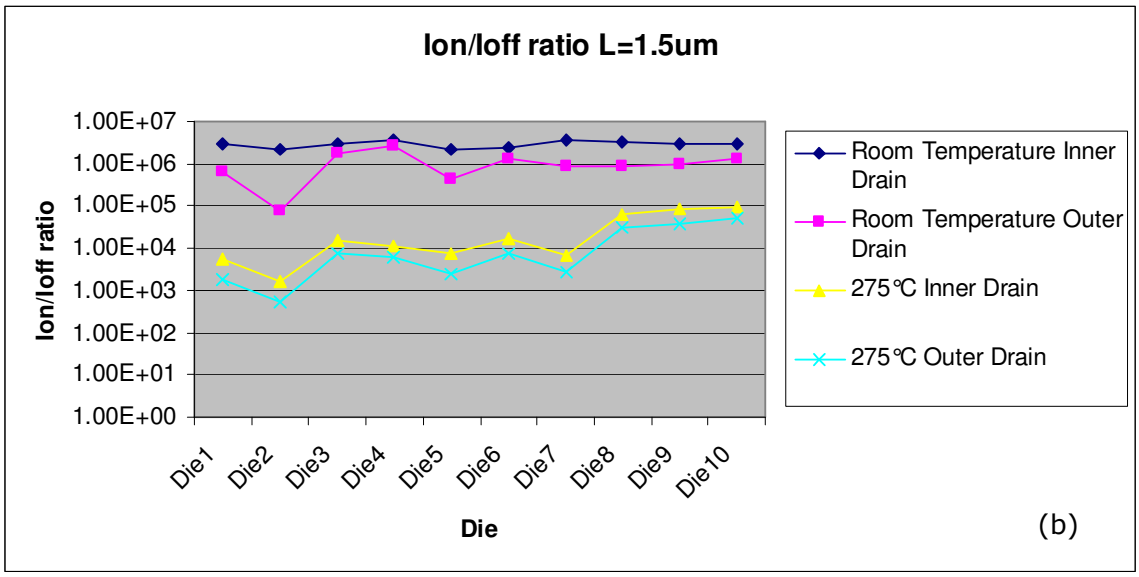
5.4.1 Experimental Procedure

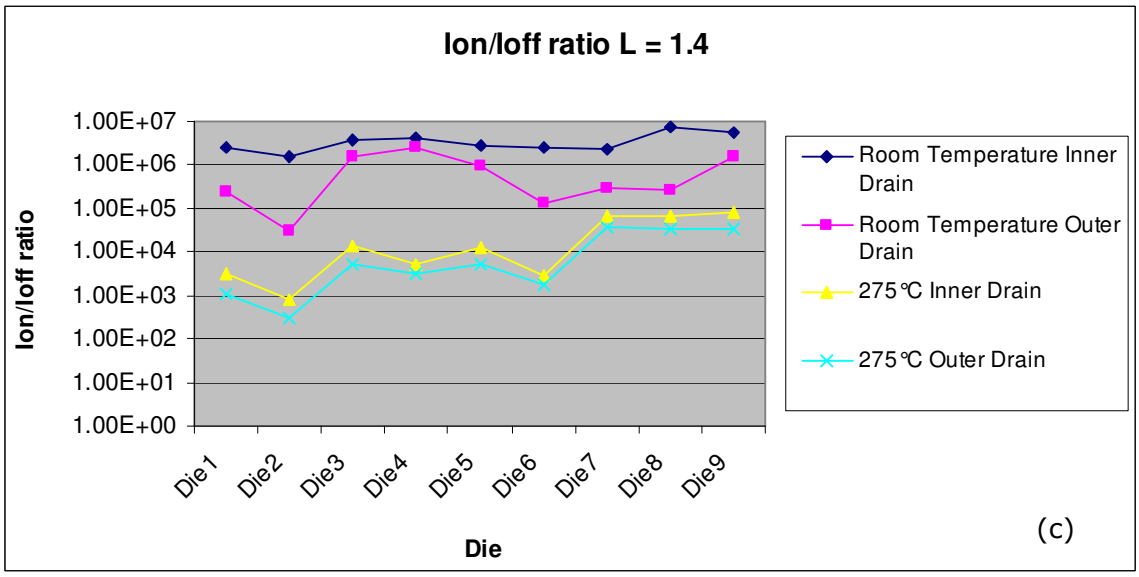
The 'ON' current is measured by setting the drain to source voltage VDS = 50mV and the 'OFF' current was measured by setting the value of VDS = 3.6V, while sweeping the gate to source voltage VGS from 0V to 3.6V in both cases. The 'ON' current is the current measured at VGS=3.6V when VDS=50mV. The 'OFF' current is the current measured at VGS=0V when VDS=3.6V.

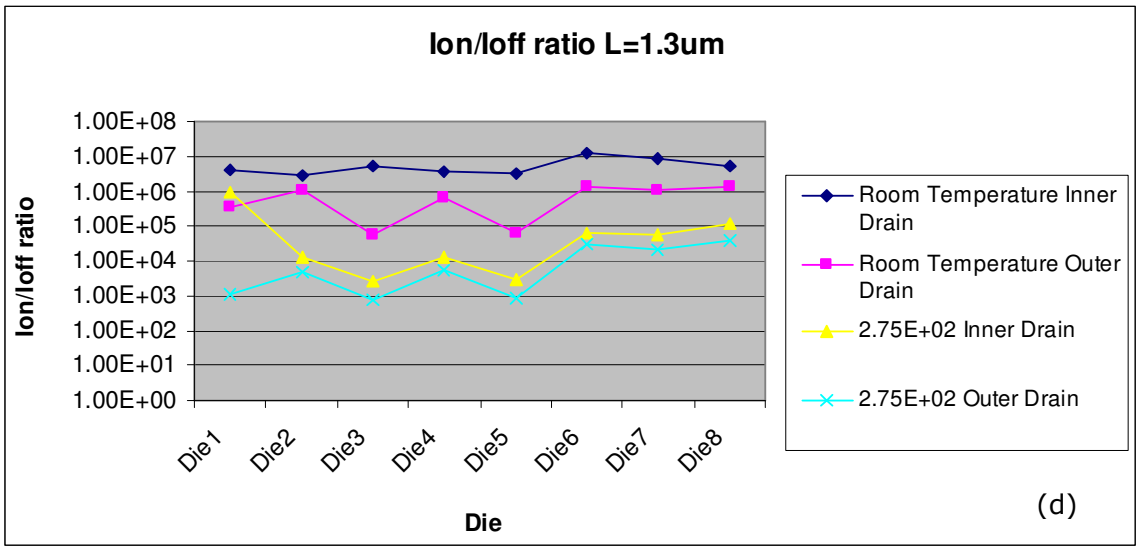
5.4.2 Observations

The leakage performance per um of width annular and rectangular NMOS devices are measured. The readings at room temperature and 275C are illustrated in figure 5-5. The following graphs show the variation of the Ion/Ioff ratios for these NMOS devices across 10 dies.




Ion/Ioff ratio L=1.5um
Ion/Ioff ratio
1.00E+07
1.00E+06
1.00E+05
1.00E+04
1.00E+03
1.00E+02
1.00E+01
1.00E+00
Die1
Die2
Die3
Die4
Die5
Die6
Die7
Die8
Die9
Die10
Die
Room Temperature Inner Drain
Room Temperature Outer Drain
275℃ Inner Drain
275℃ Outer Drain
(b)


Ion/Ioff ratio L = 1.4
Ion/Ioff ratio
1.00E+07
1.00E+06
1.00E+05
1.00E+04
1.00E+03
1.00E+02
1.00E+01
1.00E+00
Die1
Die2
Die3
Die4
Die5
Die6
Die7
Die8
Die9
Die
Room Temperature Inner Drain
Room Temperature Outer Drain
275℃ Inner Drain
275℃ Outer Drain
(c)



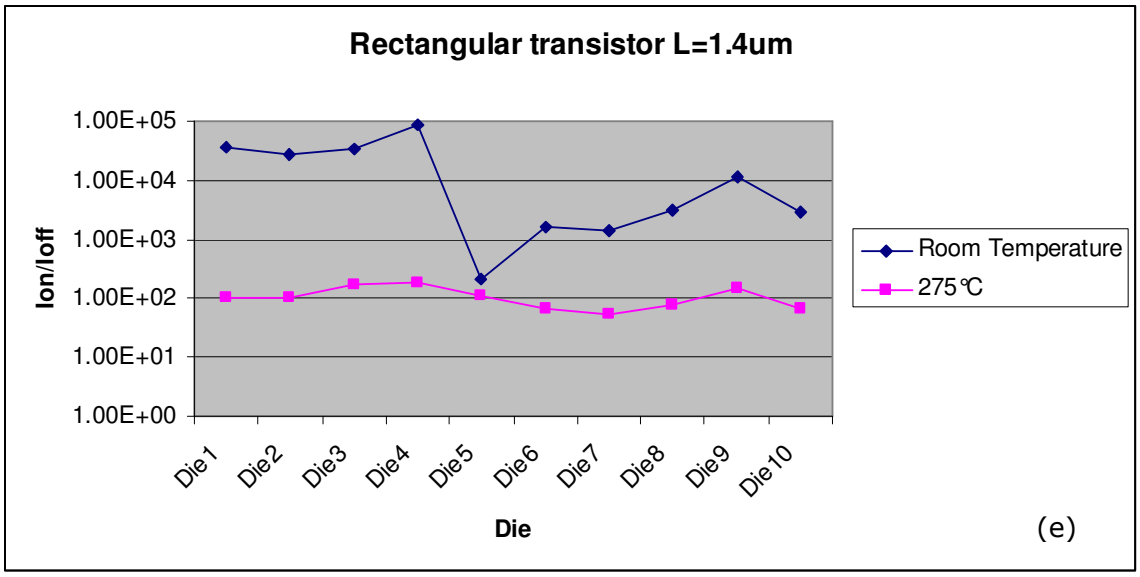


Figure 5-5 Ion/Ioff ratio Measurements (Figures (a)-(d) refer to annular transistors (a) L=1.6um, (b) L=1.5um, (c) L=1.4um, (d) L=1.3um (e) Rectangular transistor L=1.4um)

5.4.3 Inference

The table 5-2 below lists the mean and the standard deviation values of Ion/Ioff, measured across 10 die of each length, at room temperature and 275°C.

Table 5-2 Ion/Ioff ratio comparison

Length(um)	Annular transistor	Mean (Ion/Ioff)		Standard deviation (Ion/Ioff)	
		Room Temperature	275°C	Room Temperature	275°C
1.3	Inner Drain	5.70E+06	1.46E+05	3.32E+06	3.09E+05
	Outer Drain	7.47E+05	1.30E+04	5.47E+05	1.56E+04
1.4	Inner Drain	3.56E+06	2.75E+04	1.78E+06	3.22E+04
	Outer Drain	8.35E+05	1.34E+04	8.74E+05	1.60E+04
1.5	Inner Drain	2.96E+06	1.09E+06	3.07E+04	1.49E+04
	Outer Drain	5.65E+05	7.10E+05	3.57E+04	1.84E+04
1.6	Inner Drain	3.60E+06	3.12E+04	8.49E+05	3.27E+04
	Outer Drain	1.40E+06	2.12E+04	7.95E+05	2.69E+04
1.4	Rectilinear Transistor	2.05E+04	1.08E+02	2.77E+04	4.54E+01

It can be observed that the Ion/Ioff values increase by approximately 75.5% for the annular transistor with the inner drain and outer drain terminal configurations at room temperature and 51% at 275°C. Ion/Ioff ratio is greater by 97% for annular transistor with outer drain as compared to the rectilinear transistor of same dimensions. Annular transistors with either inner drain or outer drain configuration show a 98% decrease in Ion/Ioff ratio from room temperature to 275°C. This is consistent with the hypothesis which made in section 4.4.4 before conducting the experiments. Ion/Ioff ratio is increased by 99% for an annular transistor with inner drain to a rectangular transistor at room temperature. This increased Ion/Ioff ratio

indicates a significant reduction in the leakage current. This result can be very useful for analog circuit design in the subthreshold region.

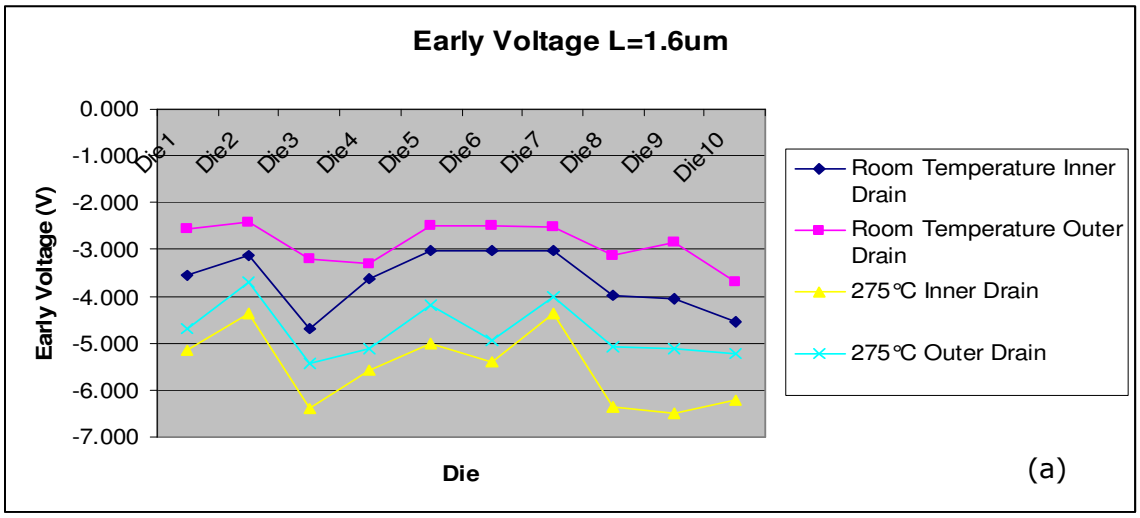
5.5 Measurement of Early Voltage (V_A)

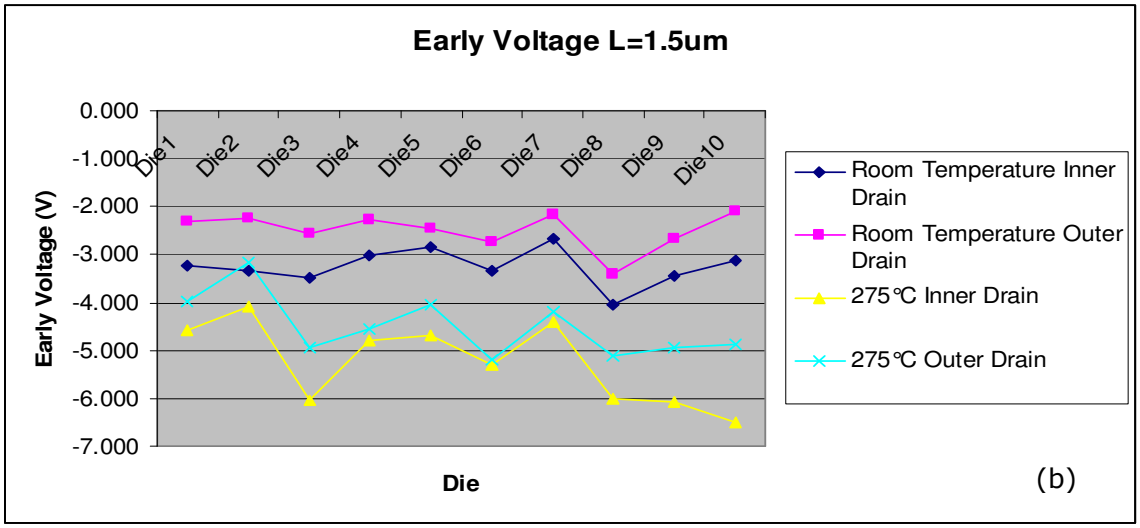
5.5.1 Experimental Procedure

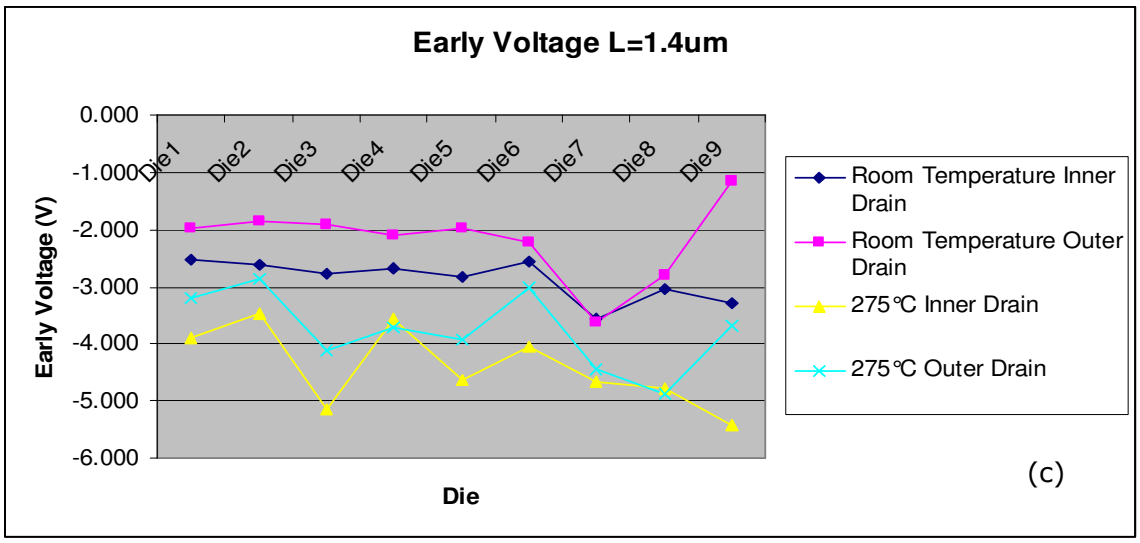
Early voltage is measured by plotting the ID-VD curve, in the saturation region. ID-VD curve is obtained by sweeping the VDS from 0V to 3.6V and changing VGS from 0.3V to 0.6V in steps of 0.1V. These curves below the kink voltage are extrapolated to the point where they meet the X-axis to determine the early voltage. The average of all four readings is taken for each device to give the final value of early voltage. The lower values of VGS are selected since early voltage is a significant parameter for analog designs and analog CMOS devices are typical biased at lower over drive voltages, -50mV to 300mV.

5.5.2 Observation

The early voltage of annular NMOS of length 1.6um, 1.5um, 1.4um and 1.3um are measured for inner and outer drain terminal configurations. The readings at room temperature and 275C are illustrated in the following graphs. These graphs show the variation of the early voltage for these NMOS devices across 10 dies. A similar graph is plotted for rectilinear transistor of length 1.4um.


Early Voltage L=1.6um
0.000
-1.000
-2.000
-3.000
-4.000
-5.000
-6.000
-7.000
Early Voltage (V)
Die1
Die2
Die3
Die4
Die5
Die6
Die7
Die8
Die9
Die10
Die
Room Temperature Inner Drain
Room Temperature Outer Drain
275℃ Inner Drain
275℃ Outer Drain
(a)


Early Voltage L=1.5um
0.000
-1.000
-2.000
-3.000
-4.000
-5.000
-6.000
-7.000
Early Voltage (V)
Die1
Die2
Die3
Die4
Die5
Die6
Die7
Die8
Die9
Die10
Die
Room Temperature Inner Drain
Room Temperature Outer Drain
275℃ Inner Drain
275℃ Outer Drain
(b)


Early Voltage L=1.4um
0.000
-1.000
-2.000
-3.000
-4.000
-5.000
-6.000
Early Voltage (V)
Die1
Die2
Die3
Die4
Die5
Die6
Die7
Die8
Die9
Die
Room Temperature Inner Drain
Room Temperature Outer Drain
275℃ Inner Drain
275℃ Outer Drain
(c)

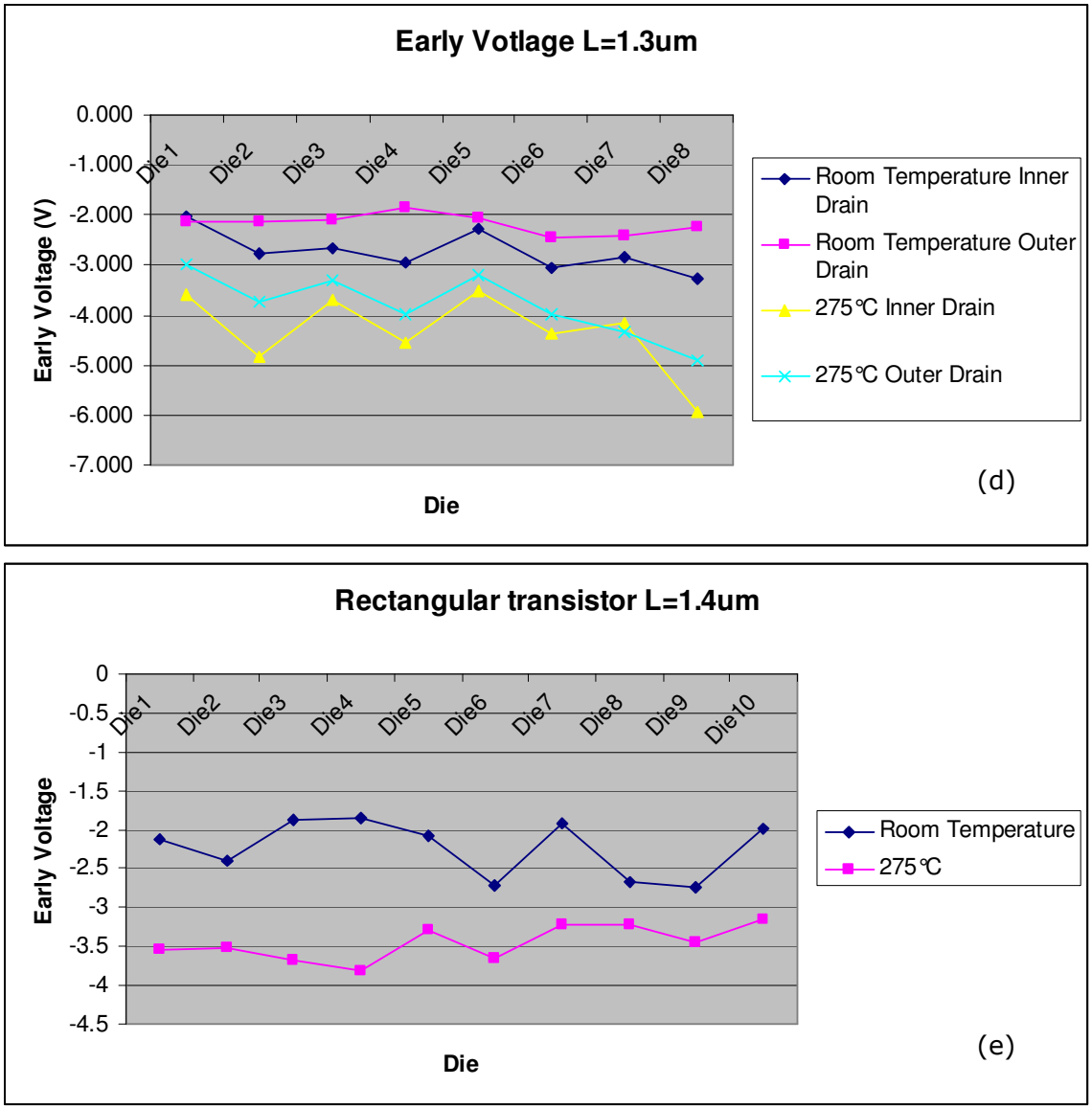


Figure 5-6 Early Voltage Measurements (Figures (a)-(d) refer to annular transistors (a) L=1.6um, (b) L=1.5um, (c) L=1.4um, (d) L=1.3um (e) Rectangular transistor L=1.4um)

5.5.3 Inference

The table 5-3 lists the mean and the standard deviation values of early voltage, measured across 10die of each length, at room temperature and 275°C.

Table 5-3 Early Voltage comparison

Length(um)	Annular transistor	Mean (VA)		Standard deviation (VA)	
		Room Temperature	275°C	Room Temperature	275°C
1.3	Inner Drain	-2.733	-4.333	0.399	0.803
	Outer Drain	-1.611	-3.803	1.566	0.631
1.4	Inner Drain	-2.876	-4.400	0.355	0.686
	Outer Drain	-2.181	-3.764	0.684	0.665
1.5	Inner Drain	-3.255	-5.249	0.390	0.848
	Outer Drain	-2.489	-4.503	0.387	0.646
1.6	Inner Drain	-2.937	-5.539	2.395	0.822
	Outer Drain	-2.862	-4.749	0.442	0.583
1.4	Rectilinear Transistor	-2.24	-3.45	3.62	2.26

Early voltage is based on electric field which is in turn dependent on the effective channel length. As electric field increases, the effective channel length decrease and therefore early voltage increases. Therefore it is expected and observed that early voltage is greater for annular transistor with inner drain and lower for annular transistor with outer drain terminal. Early voltage increases by 22.8% for annular transistor with inner drain and outer drain at room temperature and 13.7% at 275°C. Early voltage for annular transistor with inner drain is greater than rectilinear transistor by 22% at room temperature and 21.6% at 275°C. The observed data matches the hypothesis built in section 4.1.

5.6 Measurement of kink effect

5.6.1 Experimental Procedure

Kink effect is a key parameter in the analog circuit design. VGS values with Veff about 50mv to 300mV voltages are of interest in analog circuits. VGS<0.5V fall in subthreshold region and the current is mainly dominated by kink current as seen in section 4.2. Therefore kink voltage is determined at VGS = 0.8V using an ID-VD plot where VDS swept from 0V to 3.3V. The figure 5-7 shows the measurement of kink voltage at room temperature. The curve fit for each data set was taken such that the ID value for all the data points is approximately constant. The point at which ID increases by more than 5% from the fit is the kink voltage.

Kink effect is a key parameter in the analog circuit design. VGS values with Veff about 50mv to 300mV voltages are of interest in analog circuits. For VGS<0.5V device operation is in subthreshold region or moderate inversion and the drain currents above the kink voltage are dominated by kink currents as was observed in section 4.2. Therefore kink voltage is measured at VGS = 0.8V using an ID-VD plot where VDS is swept from 0V to 3.3V. The figure 5-7 shows the measurement of kink voltage at room temperature. In this figure, the curve fit for each data set was taken such that the ID value for all the data points is approximately constant. The point at which ID increases by more than 5% from the fit is the kink voltage.

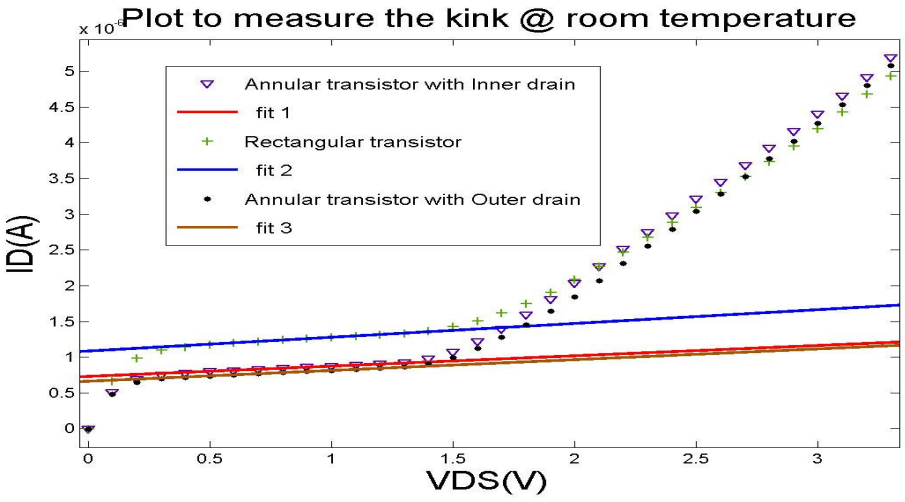
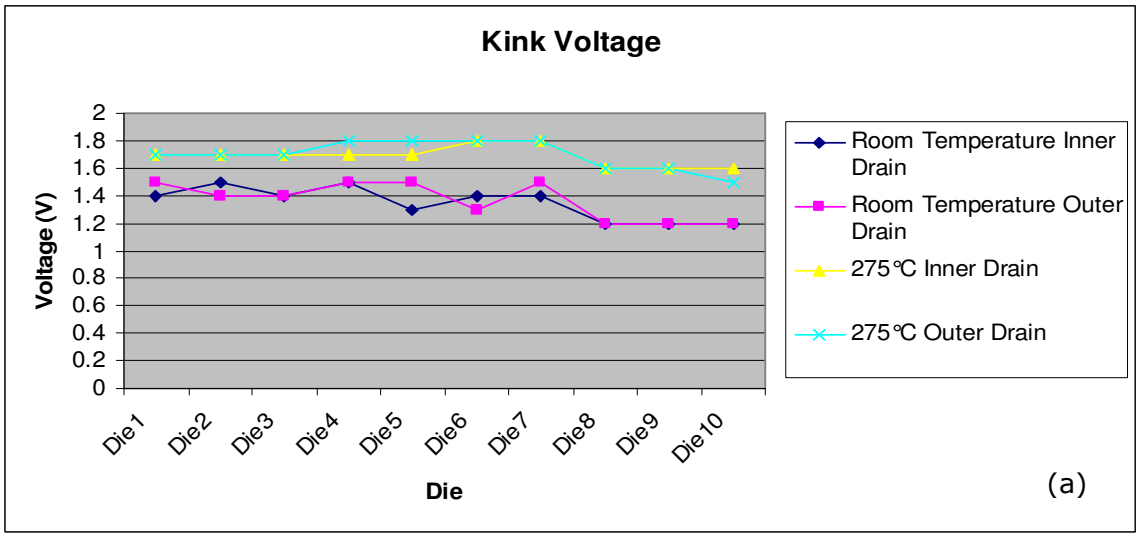
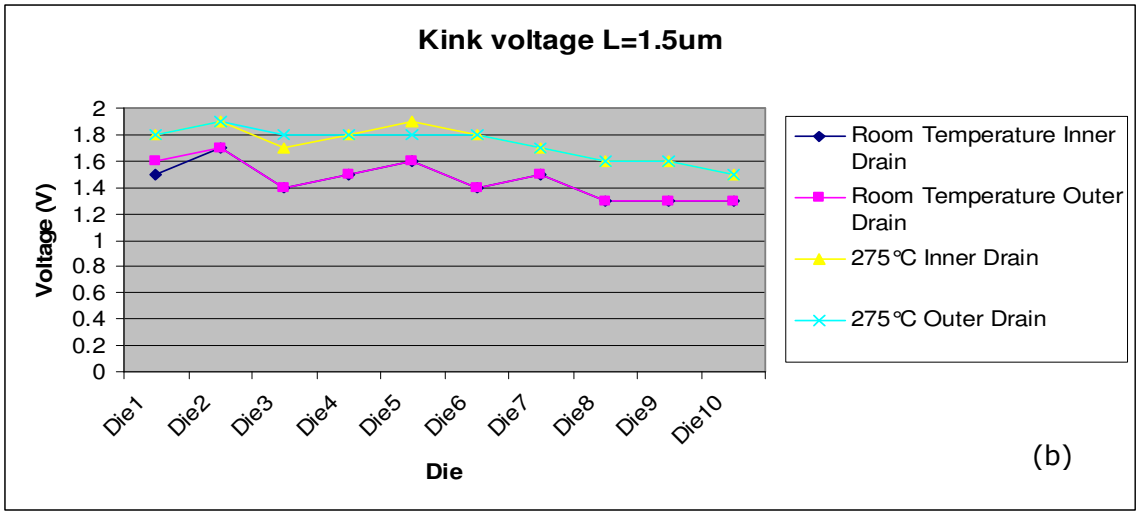


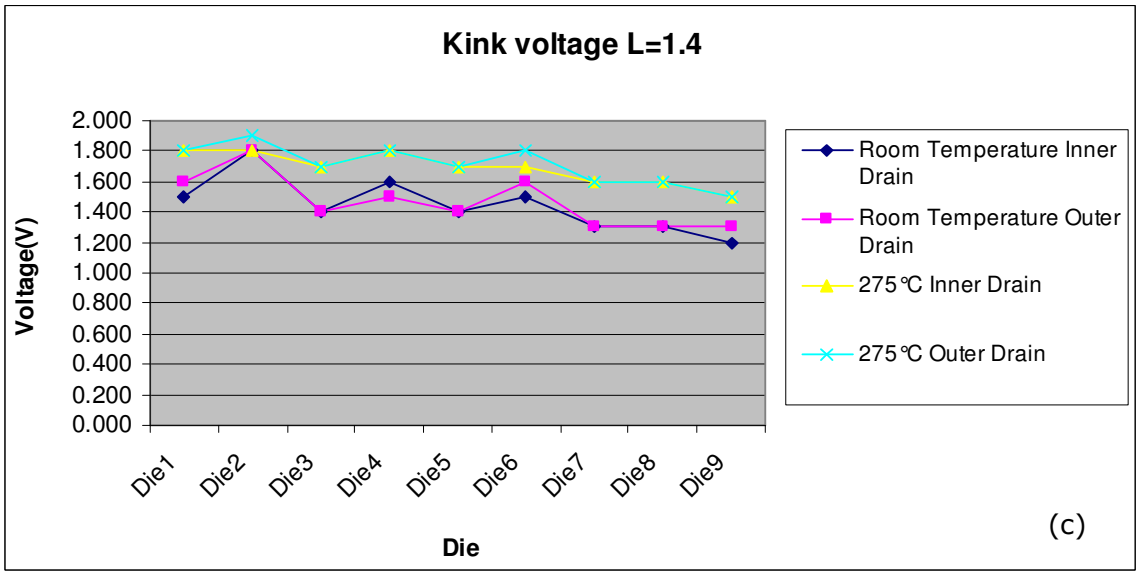
Figure 5-7 Kink voltage measurement setup

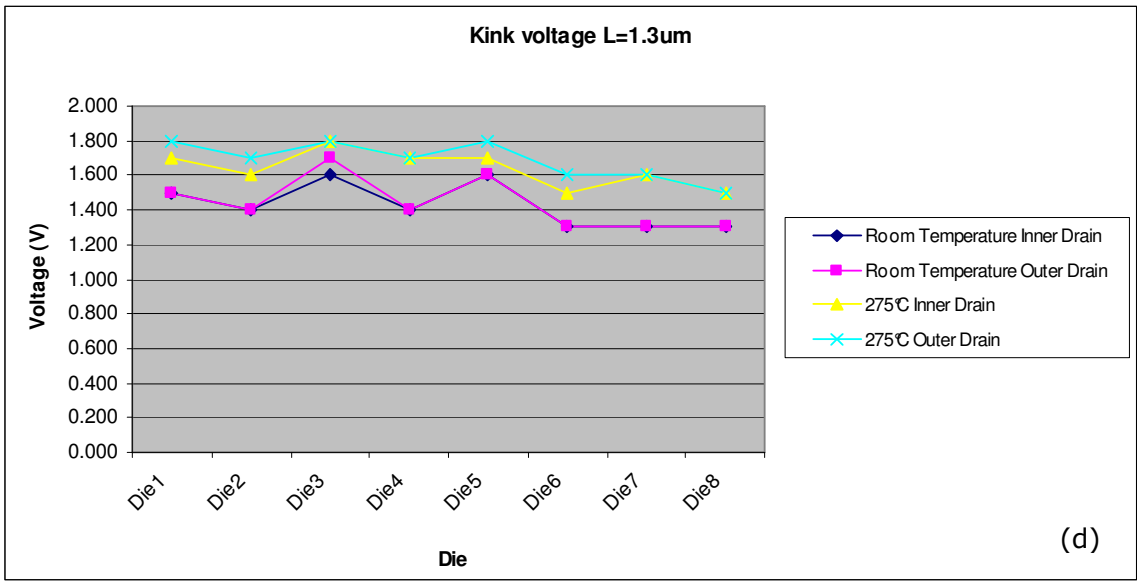
5.6.2 Observation

The figure 5-8 show the variation of kink voltage across 10 dies of annular transistor with L=1.6um, 1.5um, 1.4um and 1.3um respectively. This is followed by the plot showing the variation on kink voltage for the rectilinear transistor of L=1.4um.




Kink voltage L=1.5um
Voltage (V)
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
Die1
Die2
Die3
Die4
Die5
Die6
Die7
Die8
Die9
Die10
Die
Room Temperature Inner Drain
Room Temperature Outer Drain
275℃ Inner Drain
275℃ Outer Drain
(b)


Kink voltage L=1.4
Voltage(V)
2.000
1.800
1.600
1.400
1.200
1.000
0.800
0.600
0.400
0.200
0.000
Die1
Die2
Die3
Die4
Die5
Die6
Die7
Die8
Die9
Die
Room Temperature Inner Drain
Room Temperature Outer Drain
275℃ Inner Drain
275℃ Outer Drain
(c)



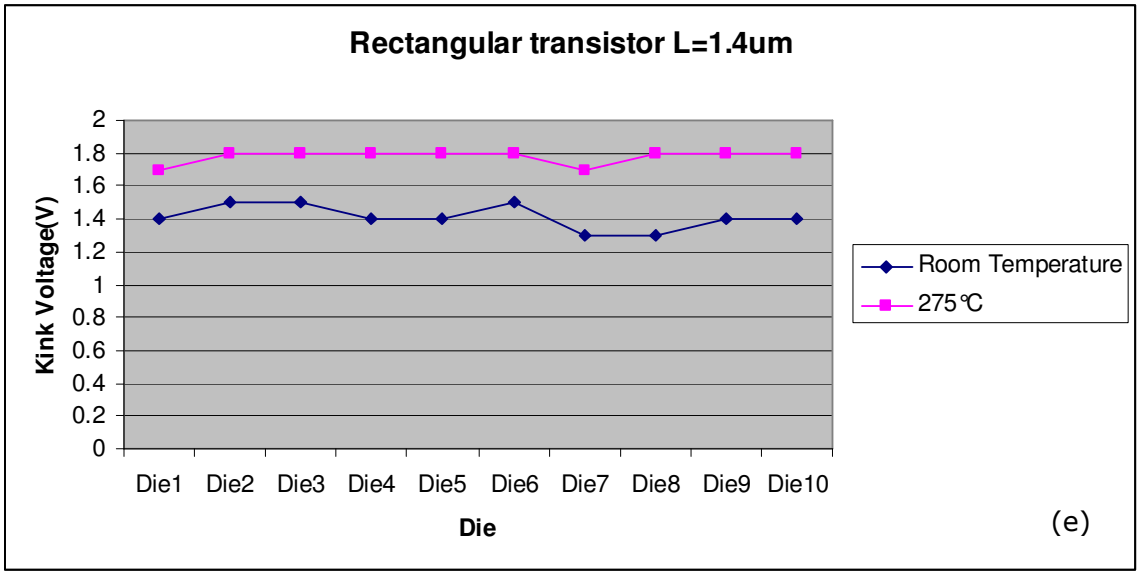


Figure 5-8 Kink Voltage Measurements (Figures (a)-(d) refer to annular transistors (a) L=1.6um, (b) L=1.5um, (c) L=1.4um, (d) L=1.3um (e) Rectangular transistor L=1.4um)

5.6.3 Inference

The table 5-4 shows the mean and standard deviation values of the kink voltage measured across 10dies of each length.

Table 5-4 Kink voltage comparison

Length(um)	Annular transistor	Mean Vkink		Standard deviation Vkink	
		Room Temperature	275°C	Room Temperature	275°C
1.3	Inner Drain	1.425	1.638	0.128	0.106
	Outer Drain	1.438	1.688	0.151	0.113
1.4	Inner Drain	1.444	1.689	0.181	0.105
	Outer Drain	1.467	1.711	0.173	0.127
1.5	Inner Drain	1.450	1.730	0.135	0.134
	Outer Drain	1.460	1.730	0.143	0.125
1.6	Inner Drain	1.350	1.690	0.118	0.074
	Outer Drain	1.370	1.700	0.134	0.105
1.4	Rectilinear transistor	1.41	1.78	0.07	0.04

We note that there is no real observable difference between kink voltage of annular transistor with inner drain and outer drain terminal. At room temperature the kink voltage for annular transistor is similar to that of rectilinear transistor. At 275°C we observe that kink voltage of rectangular transistor is greater than annular transistor with inner drain by 5% and 4% for annular transistor with outer drain. The observed data matches with the expectation built in section 4.4.5.

5.7 Measurement of output resistance

5.7.1 Experimental Procedure

Output resistance (Ro) is the inverse of transconductance (AC small signal parameter that relates the AC gate voltage to the AC drain current).

$$ro = \left[\frac{\partial ID}{\partial VDS}\right]^{-1}_{VGS=\ constant} \tag{5.1}$$

In the saturation region drain current is independent of VDS voltage. Thus ideally small change in drain to source voltage do not cause a change in the drain current; this implies that the incremental resistance looking into the drain of saturated MOSFET is infinite. More practically however the Early Voltage effect models the change in gds or id resulting from the electrical shortening of the channel length.

Output resistance is the ratio of the change in VDS to the change in drain current. The output resistance is measured by setting the VGS=0.8V and sweeping the VDS from 0V to 3.3V. Figure 5-9 shows the region in which the output resistance is measured; in the saturation region (VDS equal 0.6 to 1.2V) just before the kink occurs, approximately, 1.5V.

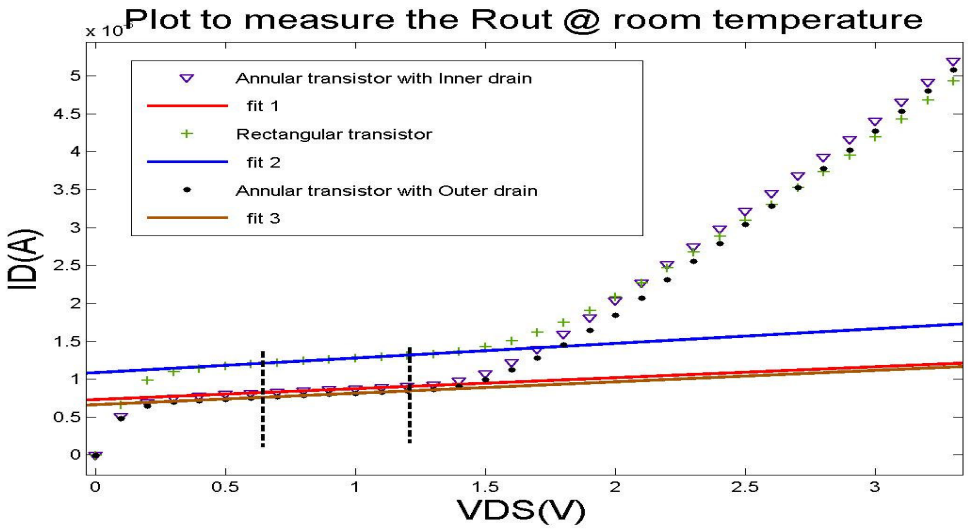
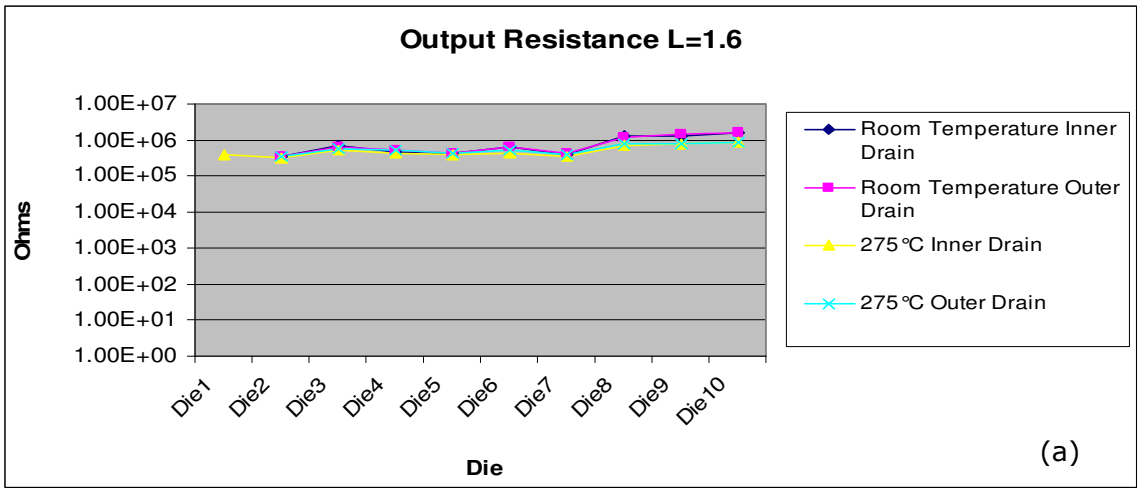
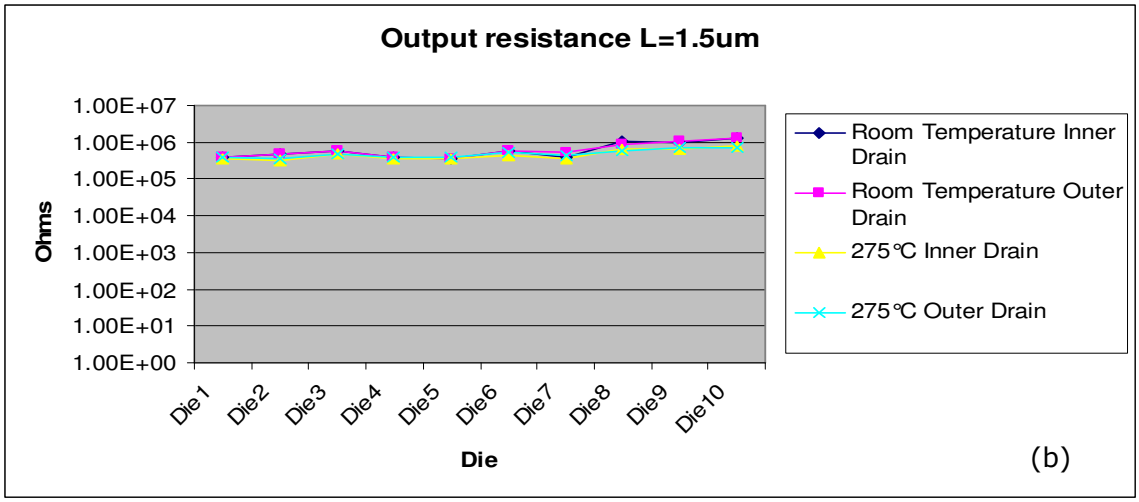


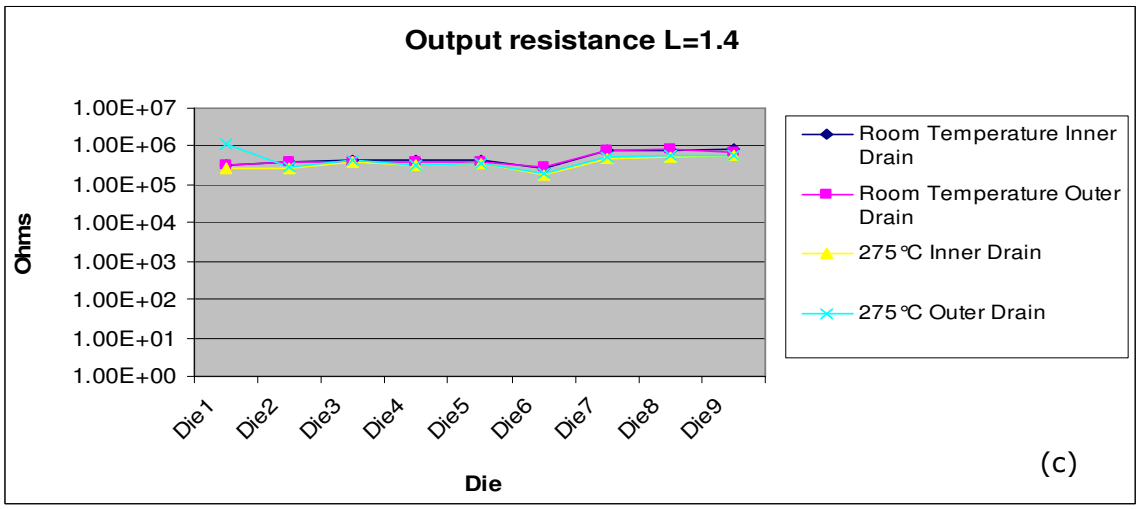
Figure 5-9 Output resistance measurement setup

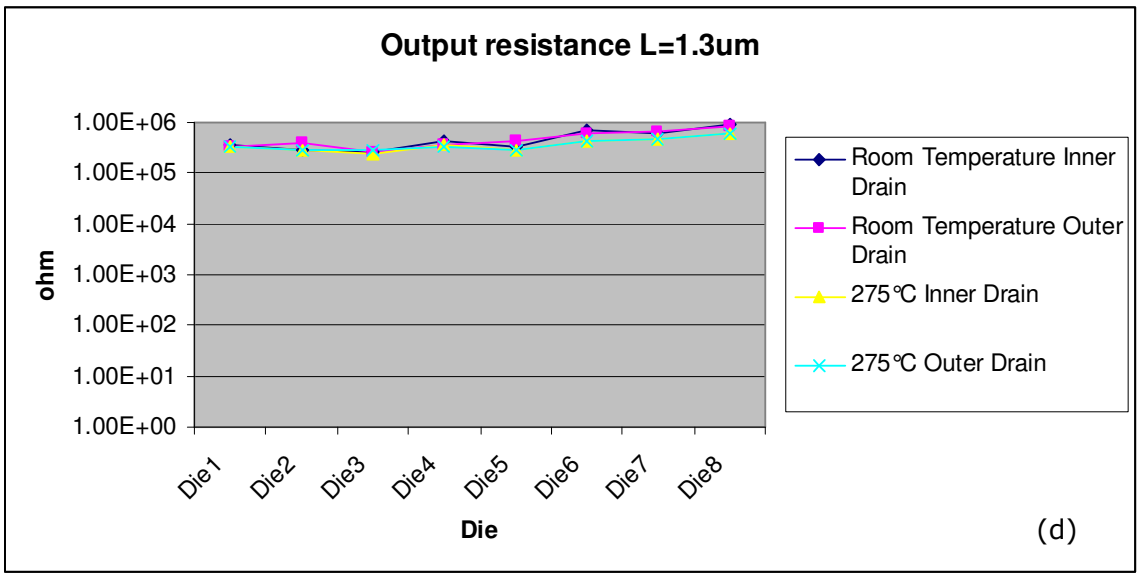
5.7.2 Observation

The following graphs illustrate the variation in the output resistance across 10 dies of lengths 1.6um, 1.5um, 1.4um, 1.3um respectively.




Output resistance L=1.5um
Ohms
1.00E+07
1.00E+06
1.00E+05
1.00E+04
1.00E+03
1.00E+02
1.00E+01
1.00E+00
Die1
Die2
Die3
Die4
Die5
Die6
Die7
Die8
Die9
Die10
Die
Room Temperature Inner Drain
Room Temperature Outer Drain
275°C Inner Drain
275°C Outer Drain
(b)


Output resistance L=1.4
Ohms
1.00E+07
1.00E+06
1.00E+05
1.00E+04
1.00E+03
1.00E+02
1.00E+01
1.00E+00
Die1
Die2
Die3
Die4
Die5
Die6
Die7
Die8
Die9
Die
Room Temperature Inner Drain
Room Temperature Outer Drain
275°C Inner Drain
275°C Outer Drain
(c)


Output resistance L=1.3um
ohm
1.00E+06
1.00E+05
1.00E+04
1.00E+03
1.00E+02
1.00E+01
1.00E+00
Die1
Die2
Die3
Die4
Die5
Die6
Die7
Die8
Die
Room Temperature Inner Drain
Room Temperature Outer Drain
275°C Inner Drain
275°C Outer Drain
(d)

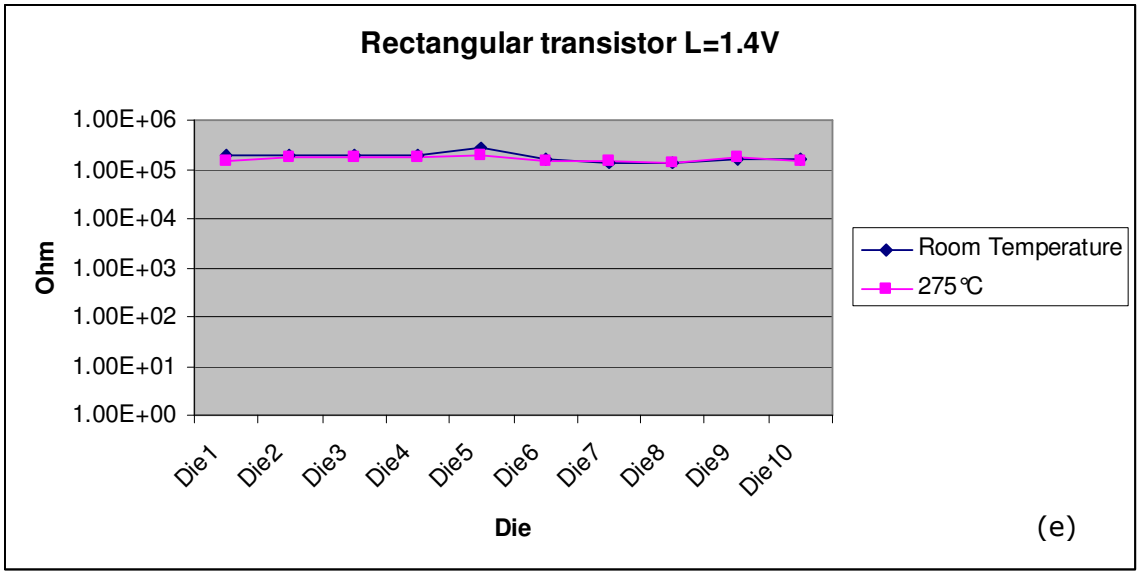


Figure 5-10 Output Resistance Measurements (Figures (a)-(d) refer to annular transistors (a) L=1.6um, (b) L=1.5um, (c) L=1.4um, (d) L=1.3um (e) Rectangular transistor L=1.4um)

5.7.3 Inference

The mean value and standard deviation of output resistance for the lengths of 1.3um, 1.4um, 1.5um and 1.6um are listed in table 5-5. This table mentions the readings for both annular transistor with inner drain terminal and outer drain terminal at room temperature and 275ºC.

Table 5-5 Output resistance comparison

Length(um)	Annular transistor	Mean Rout		Standard deviation Rout	
		Room Temperature	275°C	Room Temperature	275°C

1.3	Inner Drain	4.90E+05	3.75E+05	2.32E+05	1.13E+05
	Outer Drain	4.89E+05	3.80E+05	1.97E+05	1.14E+05
1.4	Inner Drain	5.23E+05	3.65E+05	2.22E+05	1.31E+05
	Outer Drain	5.03E+05	4.91E+05	2.17E+05	2.89E+05
1.5	Inner Drain	6.60E+05	4.66E+05	3.45E+05	1.58E+05
	Outer Drain	6.64E+05	5.00E+05	3.24E+05	1.40E+05
1.6	Inner Drain	8.05E+05	5.24E+05	4.73E+05	1.94E+05
	Outer Drain	7.99E+05	5.87E+05	4.61E+05	1.86E+05
1.4	Rectilinear transistor	1.82E+05	1.63E+05	3.76E+04	1.76E+04

We can infer that output resistance, rds, greater by 41% at room temperature as compared to 275°C for an annular transistor with inner drain and 32% greater for annular transistor with outer drain. There is no significant change between output resistance with annular transistor with inner drain terminal and outer drain terminal. Output resistance per unit width of annular transistor with inner drain is greater than rectilinear transistor by approximately 77% and 79%, at room temperature and 275°C. The improved output resistance is very useful for designing current sources in analog circuits.

6 CONCLUSION

6.1 Conclusion

Performance of annular transistor across four different transistor lengths (L= 1.3um, 1.4um 1.5um and 1.6um) was studied along with comparison to a rectilinear transistor (L=1.4um) at room temperature (RT) and 275°C.

The experimental results demonstrated a decrease in V_{TH} between the annular transistor with an inner drain compared to the rectilinear transistor by 20% at RT and 33% at 275°C. V_{TH} for an annular transistor with an inner drain is greater than the same transistor with an outer drain by 2% at RT and 3% at 275°C. The Ion/Ioff ratio for annular devices with an inner drain compared to a rectangular device shows an improvement of 99% at both RT and 275°C. The Ion/Ioff ratio for the same annular transistor with an inner drain verses an outer drain is greater by 75% at RT and 51% at 275°C. The Vkink voltage for an annular transistor with an inner drain is greater than rectangular transistor by 2% at RT while 5% lower at 275°C. Vkink for annular transistor with an outer drain is greater than the same transistor with an inner drain by 2% at RT and 1% at 275°C. Early voltage (V_A) for an annular transistor with an inner drain is greater than rectangular transistor by 22% at RT and 21% at 275°C. V_A for an annular transistor with an inner drain is greater than the same transistor with an outer drain by 22% at RT and 15% at 275°C. Output resistance (rds) per unit width of an annular transistor with an inner drain is greater than rectilinear transistor by 77% at RT and 79% at 275°C. rds for annular transistor with an inner drain is greater than that with an outer drain of the same device by 4% at RT and is lower by 25% at 275°C.

In conclusion when it is of the utmost importance to control leakage and device self gain annular transistors provide a significant improvement over the classical rectangular transistor. Some enhanced performance is observed when the inner contact is selected as the drain. It should also be noted that measurement accuracy precludes the taking of any conclusion where changes of less than 2% are observed.

6.2 Future work

There is lot of scope for the study which can be performed on annular transistors, in terms of the device sizes and the performance in circuits. For smaller device length there is a visible change in threshold voltage between the inner and outer drain terminals. These devices need can be fabricated and analyzed to get conclusive outcome. Layout of annular transistors for large transistors in analog circuits poses a challenge.

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ASIC technologies Application of hardness by- design methodology to radiation-tolerant ASIC technologies," Nuclear Science, IEEE Transactions on, vol. 47, pp. 2334-2341, 2000.

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VITA

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Scope and Method of Study:

Annular transistors are enclosed geometry transistors which reduce device leakage by eliminating diffusion edges. Due to the asymmetry of these devices with respect to inner and outer terminals; this study evaluates the behavior of the annular transistor with respect to both the inner and outer drain terminals. Along with this, the effects of geometry of the device on the leakage current and kink effects, related to the NMOS SOS devices at various temperatures are evaluated. Performance of NMOS annular transistor across four different transistor lengths (L= 1.3um, 1.4um 1.5um and 1.6um) are studied along with comparison to a NMOS rectilinear transistors (L=1.4um) at room temperature (RT) and 275°C.

Findings and Conclusions:

The experimental results demonstrated a decrease in V_{TH} between the annular transistor with an inner drain compared to the rectilinear transistor by 20% at RT and 33% at 275°C. V_{TH} for an annular transistor with an inner drain is greater than the same transistor with an outer drain by 2% at RT and 3% at 275°C. The Ion/Ioff ratio for annular devices with an inner drain compared to a rectangular device shows an improvement of 99% at both RT and 275°C. The Ion/Ioff ratio for the same annular transistor with an inner drain verses an outer drain is greater by 75% at RT and 51% at 275°C. The Vkink voltage for an annular transistor with an inner drain is greater than rectangular transistor by 2% at RT while 5% lower at 275°C. Vkink for annular transistor with an outer drain is greater than the same transistor with an inner drain by 2% at RT and 1% at 275°C. Early voltage (V_A) for an annular transistor with an inner drain is greater than rectangular transistor by 22% at RT and 21% at 275°C. V_A for an annular transistor with an inner drain is greater than the same transistor with an outer drain by 22% at RT and 15% at 275°C. Output resistance (rds) per unit width of an annular transistor with an inner drain is greater than rectilinear transistor by 77% at RT and 79% at 275°C. rds for annular transistor with an inner drain is greater than that with an outer drain of the same device by 4% at RT and is lower by 25% at 275°C.

In conclusion when it is of the utmost importance to control leakage and device self gain annular transistors provide a significant improvement over the classical rectangular transistor. Some enhanced performance is observed when the inner contact is selected as the drain. It should also be noted that measurement accuracy precludes the taking of any conclusion where changes of less than 2% are observed.

ADVISER'S APPROVAL: Dr. Chris Hutchens