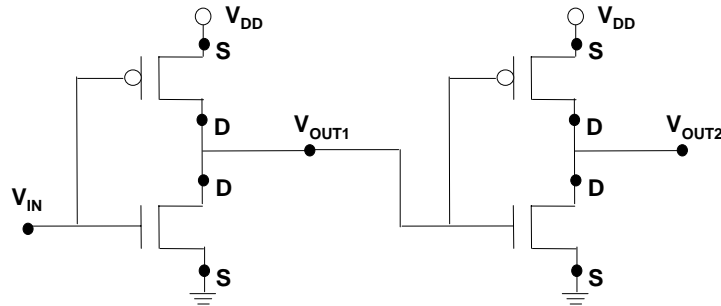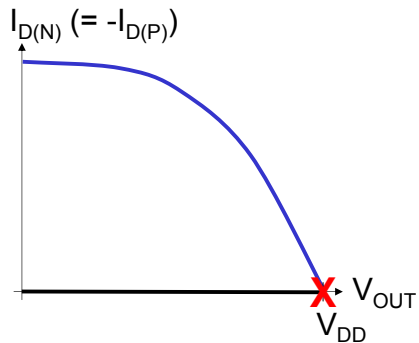# CMOS LOGIC

Inside the CMOS inverter, no I_D current flows through transistors when input is logic 1 or logic 0, because

- the NMOS transistor is cutoff for logic 0 (0 V) input
- the PMOS transistor is cutoff for logic 1 (V_{DD}) input
- current through the "turned on" transistor has nowhere to go if next stage consists of transistor gates
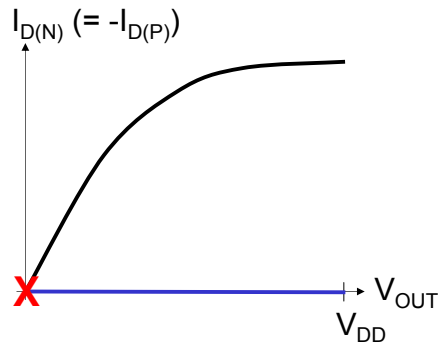
$V_{IN} = 0$ V

- NMOS transistor cutoff (since $V_{GS(N)} = V_{IN} = 0$ V) "acts as open circuit"
- PMOS transistor "on" ($V_{GS(P)} = V_{IN} - V_{DD} = -V_{DD}$) but $I_{D(P)} = 0$ A => $V_{DS(P)} = 0$ V

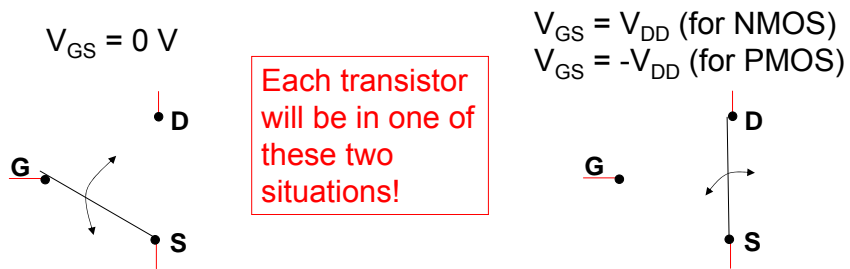## $V_{IN} = V_{DD}$

- PMOS transistor cutoff ($V_{GS(P)} = V_{IN} - V_{DD} = 0$ V) "acts as open circuit"
- NMOS transistor "on" ($V_{GS(N)} = V_{IN} = V_{DD}$) but $I_{D(N)} = 0$ A => $V_{DS(N)} = 0$ V
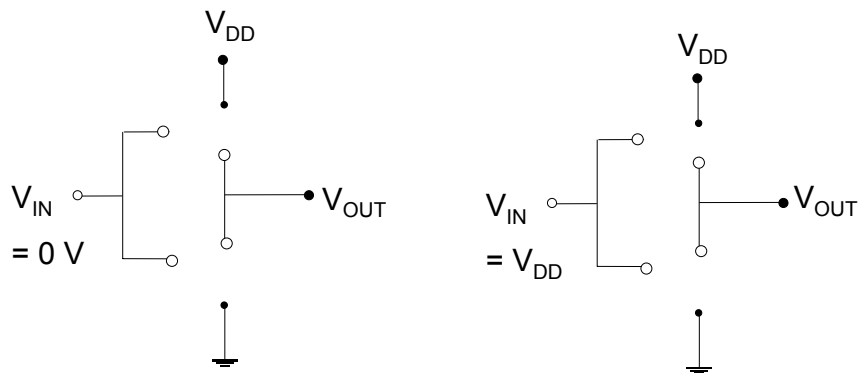
EASY MODEL FOR LOGIC ANALYSIS

There is a simpler model for the behavior of transistors in a CMOS
logic circuit, which applies when the input to the logic circuit is
fully logic 0 or **fully logic 1**.

$V_{GS} = 0$ V

Each transistor
will be in one of
these two
situations!

$V_{GS} = V_{DD}$ (for NMOS)
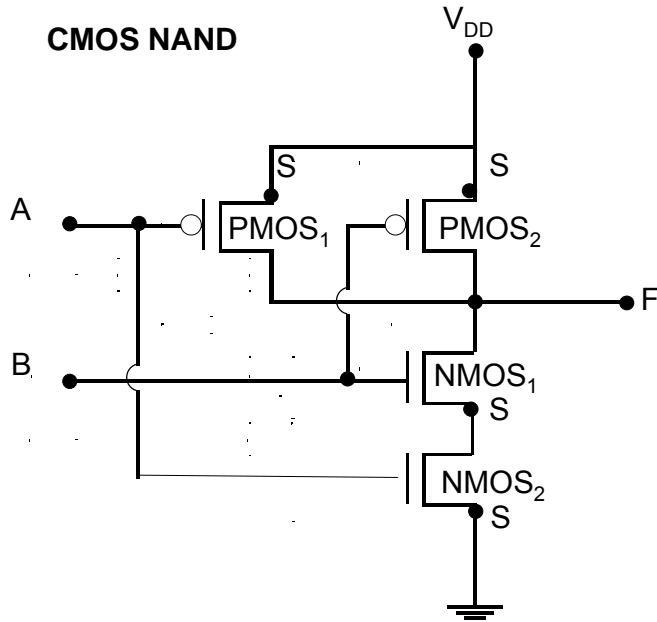$V_{GS} = -V_{DD}$ (for PMOS)

D

G

S

D

G

S

We can use the model to quickly determine the **logical**
operation of a CMOS circuit (but we cannot use it to find circuit
currents or voltages that will occur for mid-range input voltages).

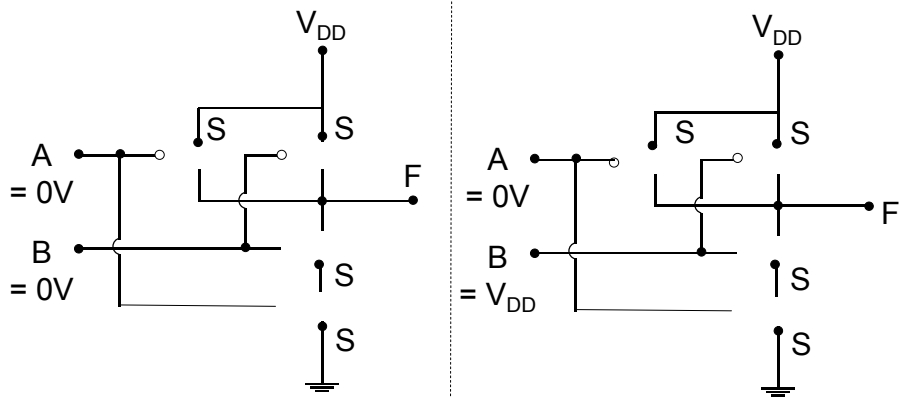## REVIEW: REVISIT CMOS INVERTER WITH SIMPLE LOGIC MODEL

Fill in the switch positions below…

V_{DD}

V_{IN}
= 0 V

V_{OUT}

V_{DD}

V_{IN}
= V_{DD}

V_{OUT}

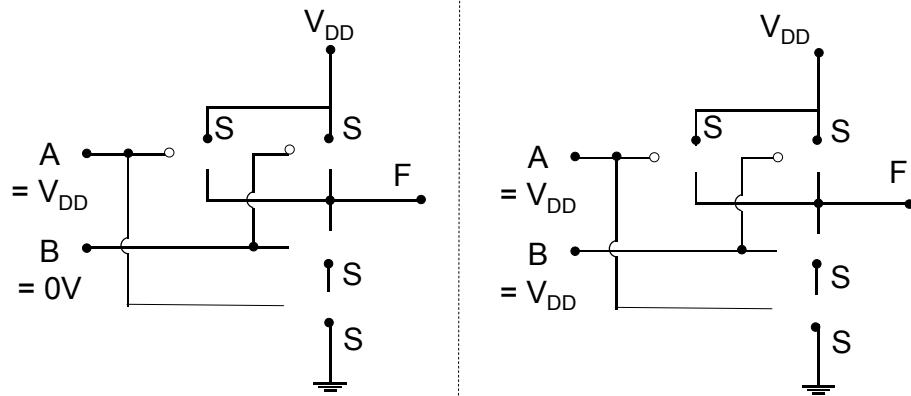**CMOS NAND**

V_{DD}

S S

A

$PMOS_1$ $PMOS_2$

F

B

$NMOS_1$

S

$NMOS_2$

S

Verify the logical operation of the CMOS NAND circuit:

V_{DD}

S S

A
= 0V

F

B
= 0V

S

S

V_{DD}
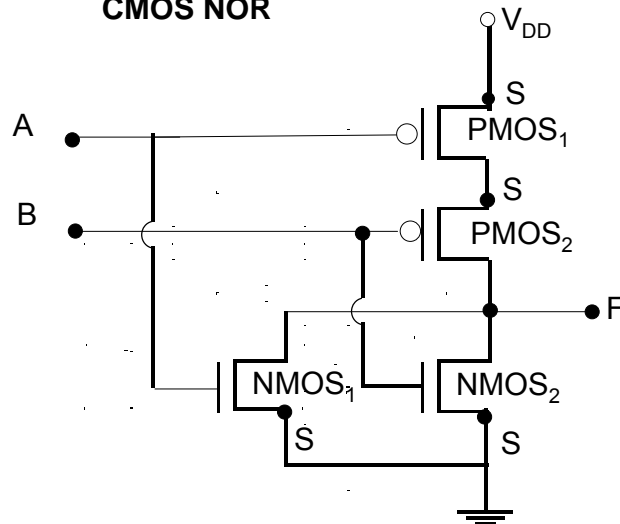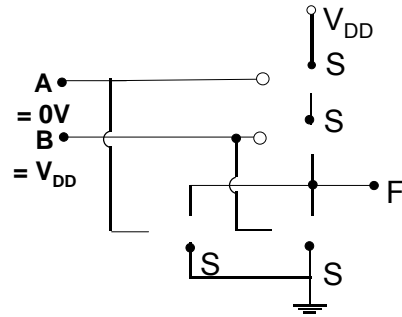
S S

A
= 0V

F

B
= V_{DD}

S

S

Verify the logical operation of the CMOS NAND circuit:

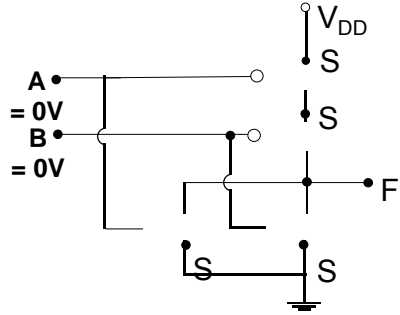**CMOS NOR**

Verify the logical operation of the CMOS NOR circuit:

A
= 0V
B
= 0V

V_{DD}
S
S
F
S   S

A
= 0V
B
= V_{DD}

V_{DD}
S
S
F
S   S

Verify the logical operation of the CMOS NOR circuit:

A
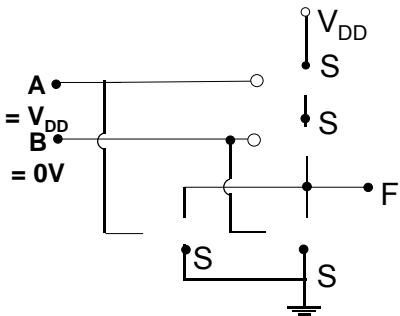= V_{DD}
B
= 0V

V_{DD}
S
S
F
S   S

A
= V_{DD}
B
= V_{DD}

V_{DD}
S
S
F
S   S
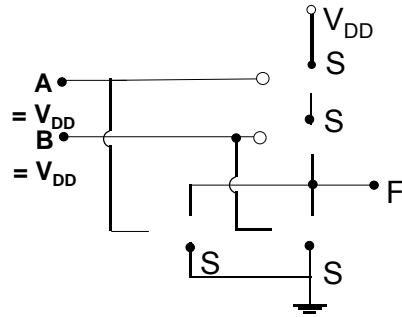
PULL-UP AND PULL-DOWN DEVICES

In our logic circuits, the NMOS transistor sources are connected to ground, and the PMOS sources are connected to V_{DD}.

Notice that when NMOS transistors are "on" (when $V_{GSN} = V_{DD}$) V_{DSN} is shorted by switch, helping connect output to ground.
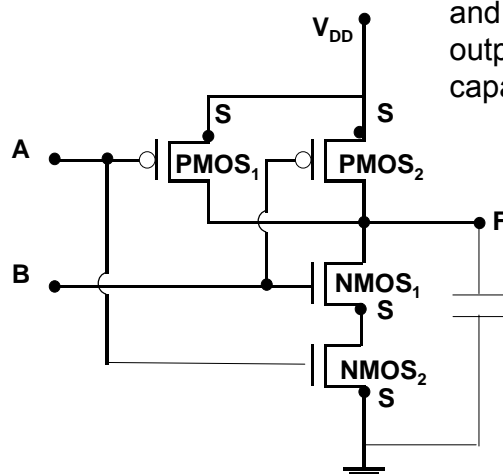
The NMOS transistor functions as a **pull-down** device; when active, it brings the output to 0 V.

When PMOS transistors are "on" (when $V_{GSP} = -V_{DD}$) V_{DSP} is shorted by switch, helping connect output to V_{DD}.

The PMOS transistor functions as a **pull-up** device; when active, it brings the output to V_{DD}.

LIMITATIONS OF SWITCH MODEL
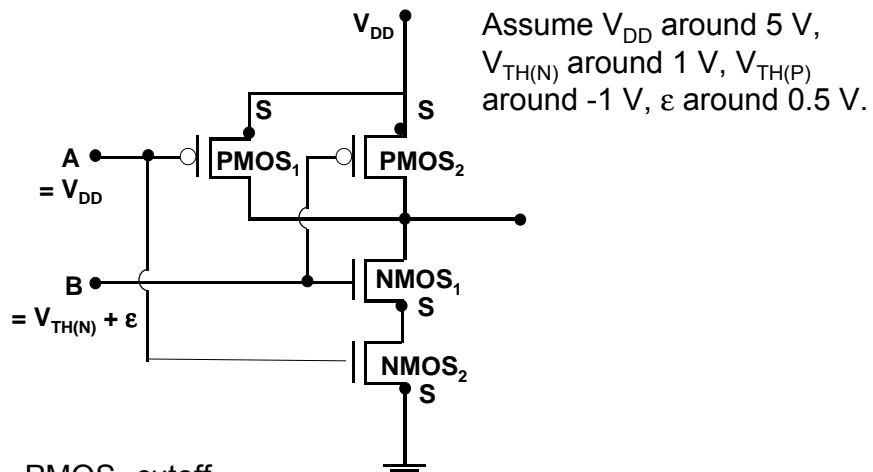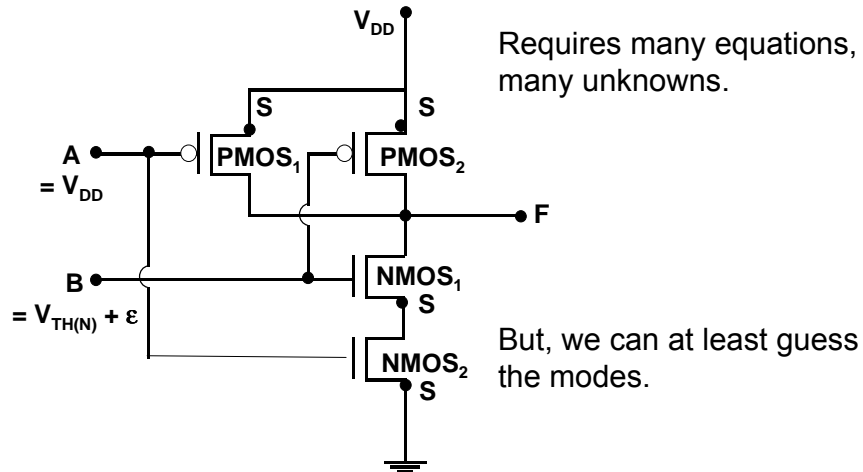
Preview of next class:

In reality, the pull-up devices must have some V_{DS} voltage and current flow to bring the output high since natural capacitance must be charged.

Similarly, the pull-down devices must have some V_{DS} voltage and current flow to bring the output to ground since natural capacitance must be discharged.

This is GATE DELAY.

LIMITATIONS OF SWITCH MODEL

Suppose one needed to fully analyze the circuit for intermediate input voltages.

Requires many equations, many unknowns.

But, we can at least guess the modes.

Assume V_{DD} around 5 V, $V_{TH(N)}$ around 1 V, $V_{TH(P)}$ around -1 V, ε around 0.5 V.

- PMOS$_1$ cutoff
- NMOS$_1$ barely on ($V_{DS(N2)} \geq 0$) => saturation
- NMOS$_2$ fully on, but NMOS$_1$ limits I_D to small value => triode
- PMOS$_2$ on, but NMOS$_1$ and PMOS$_1$ make I_D small => triode

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